Data Sheet
May 2012

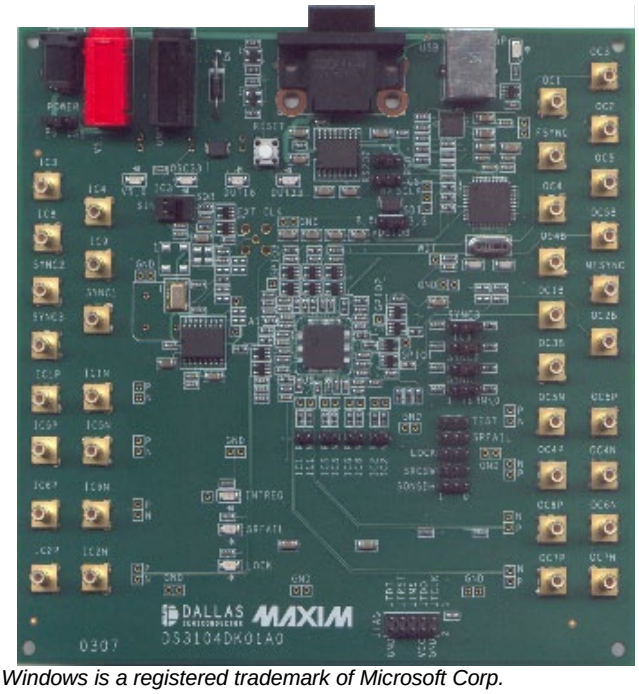
DS3106DK Demo Kit
Evaluates: DS3106 Timing IC

General Description

The DS3106DK is an easy-to-use demo and evaluation kit for the DS3106 line card timing IC. A surface-mounted DS3106 and careful layout provide maximum signal integrity. An on-board 8051-compatible microcontroller and included software give point-and-click access to configuration and status registers from a Windows®-based PC. LEDs on the board indicate interrupt, power-supply function, and lock status. Single-ended and differential clocks are accessed via SMB connectors. All LEDs and connectors are clearly labeled with silkscreening to identify associated signals.

Demo Kit Contents

DS3106DK Board
CD-ROM Includes:
- DS3106 Software
- DS3106 Initialization File
- DS3106DK Data Sheet
- DS3106 Data Sheet/Errata Sheet



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Features

- **Soldered DS3106 for Best Signal Integrity**
- **SMB Connectors and Termination Ease Connectivity**
- **Careful Layout for Analog Signal Paths**
- **On-Board Stratum 3 Oscillator with Footprints for Stratum 3E and Stratum 4 Oscillators**
- **On-Board Microcontroller and Included Software Provide Point-and-Click Access to the DS3106 Register Set**
- **LEDs for Interrupt, Power Supplies, and Lock Status**
- **Banana Jack VDD and GND Connectors Support Use of Lab Power Supplies**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**
- **Software Provides GUI Fields for Most Commonly Used Features Plus Full Read/Write Access to the Entire Register Set**
- **Software Support for Creating and Running Configuration Scripts Saves Time During Evaluation**

Minimum System Requirements

- **PC Running Windows XP or Windows 2000**
- **Display with 1024 x 768 Resolution or Higher**
- **Available USB or Serial (COM) Port**
- **USB Cable or DB-9 Serial Cable**

Ordering Information

PART	DESCRIPTION
DS3106DK	Demo kit for DS3106

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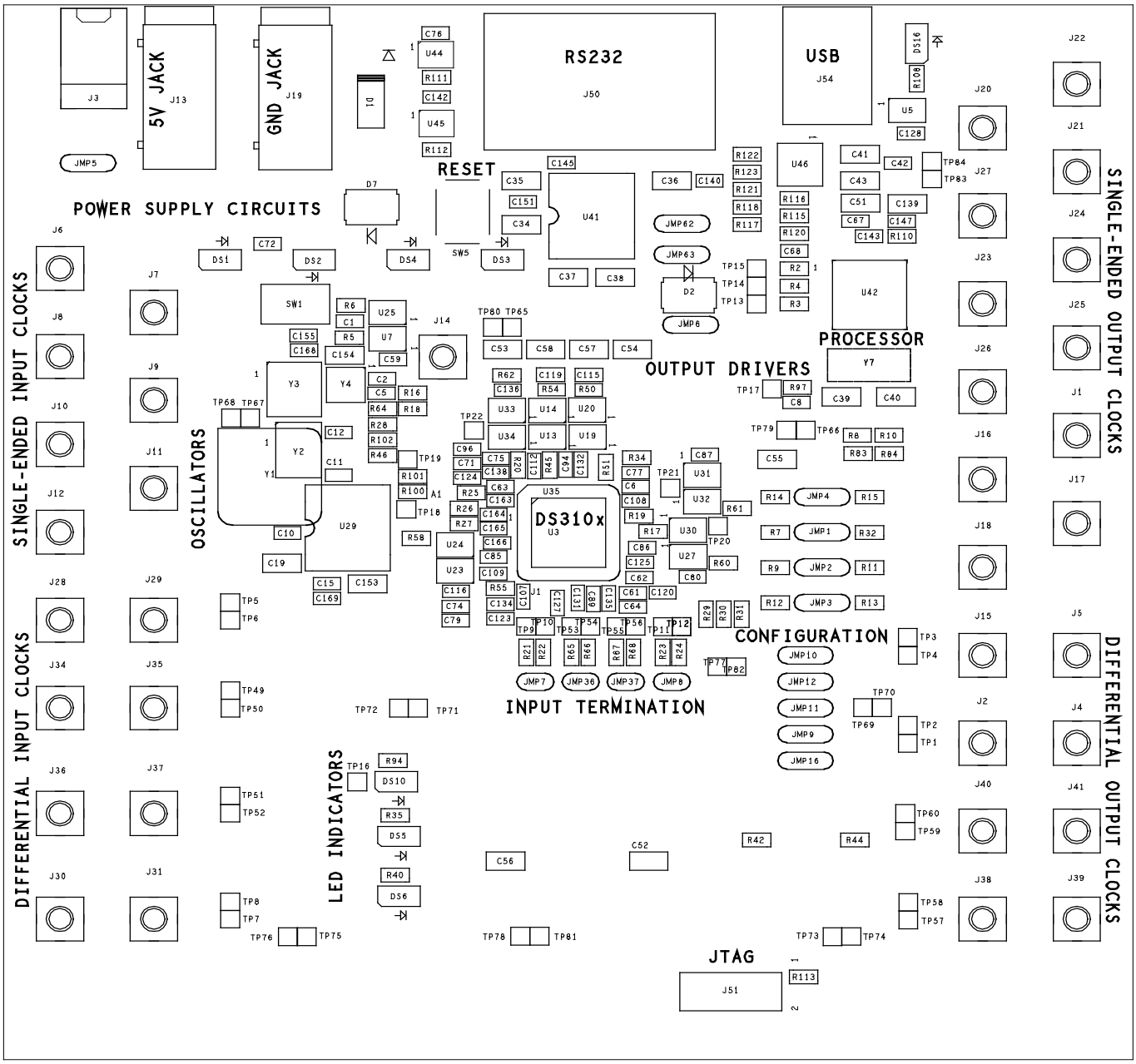
1. Board Floorplan

Figure 1-1 shows the DS3106DK floorplan. The DS3106 is in the center of the board, input clock SMB connectors are along the left edge of the board, and output clock connectors are on the right edge. Between the input clock connectors and the DS3106, land patterns are provided for several different types of local oscillators, ranging from inexpensive XOs to higher performance TCXOs. The top edge contains, from left to right, power-supply connectors, DC-DC converters and power-indicator LEDs, reset pushbutton, serial connector, and USB connector. An on-board DS87C520 microcontroller is located near the USB connector. The bottom edge of the board is occupied by a JTAG connector and LED indicators. The DS3106DK has the same PCB design as demo kits for timing ICs with more clock I/Os. As a result, many of the connectors are not populated in the DS3106DK. See Appendix 1: Hardware Components for a complete component list. Complete board schematics follow in Section 7.

Figure 1-1. DS3106DK Board Floorplan



1.1 Input and Output Clocks

There are two SMB connectors at the left of the board labeled IC3 and IC4 that provide a single-ended clock input to the DS3106. These clock inputs are connected to the DS3106 with a 50Ω characteristic impedance trace and terminated with 50Ω at the device.

On the other side of the PCB are three SMB clock output connectors labeled OC3, FSYNC, and MFSYNC. All single-ended clock outputs are buffered at the DS3106 and connected to the SMB connector via a 50Ω characteristic impedance trace. Two additional SMB connectors labeled OC6P and OC6N provide connections to the OC6 differential output from the DS3106.

1.2 Jumpers, Headers, and Switch Settings

Jumpers JMP9 to JMP12 and JMP16 (lower right of board) provide the means to pull up or pull down the O3F1/SRFAIL, O3F2/LOCK, SRCSW, SONSDH, and TEST pins of the DS3106. Labels specify which position is used to pull each pin to a 1 or a 0 (if jumper is not installed pin is left to float to accommodate a pin's output function). Jumpers JMP1 to JMP4 (middle right of board) provide access to the IPF0/SYNC1, IPF1/SYNC2, IPF2/IC9, and O3F0/SYNC3 pins of the DS3106. Labels specify the position to install the jumper to pull the pin up (signified by "1") or pull it down through a 50Ω resistor (signified by "TERM\0"). The 50Ω resistor is used as a termination resistor when the pin is used as a input clock signal. Jumper JMP6 (labeled VDDIOB) is not used in the DS3106DK. Jumpers JMP62 and JMP63 select the computer interface to be USB or RS232. Jumper JMP5 (upper left) selects whether the board should be powered from the USB connector or from the power-supply jacks (J3 or J13/J19). LEDs DS1–DS4 (upper left) indicate the labeled power supply is operational. LED DS16 (upper right) indicates the microprocessor is operational. LEDs DS5, DS6, and DS10 (lower middle) indicate the status of SRFAIL, LOCK, and INTREQ pins, respectively. Switch SW1 is used to select a squaring circuit to accommodate a sinusoidal input on IC3. Header J51 provides access to the JTAG port of the DS3106. Test points are provided for differential the differential output (OC6), SPI port pins, ground plane connection, and pings O6F0/GPIO1, O6F1/GPIO2, O6F2/GPIO3.

1.3 Microcontroller

The DS87C520 microcontroller has factory-installed firmware in on-chip nonvolatile memory. This firmware translates memory access requests from the RS232 serial port or USB port into register accesses on the DS3106. When the microcontroller starts up it turns on DS16 to indicate that the controller is working correctly. A pushbutton switch labeled RESET near the RS232 connector resets the microcontroller as well as the DS3106.

1.4 Power-Supply Connectors

A 5V lab power supply can be connected across the red (J13) and black (J19) banana jacks. Optionally the board can be powered from the USB connector by placing jumper JMP5 in the USB position. The 5V input from any of these sources is then regulated to 3.3V, 2.5V, and 1.8V and distributed to board components.

Note that the board cannot be USB powered through some USB hubs. Before trying to power the board through a USB hub, check the voltage at JMP5 to ensure the board is getting 5V from the hub.

2. Basic Hardware Setup

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the demo kit (DK) software. Text in **bold and underlined** refers to items from the Windows operating system.

The following steps provide a quick start to using the DS3106DK.

1) Place the POWER jumper (JMP5) in the PS position.
2) To communicate with the board using a USB cable:
   a) Configure the board for USB communication by placing jumpers to connect the middle and right pins of JMP62 and JMP63 (i.e., place the jumpers toward the “USB” silkscreen).
   b) Connect a USB cable between the USB connector on the DS3106DK and an available USB port on the host computer.
3) To communicate with the board using a serial (RS232) cable:
   a) Configure the board for serial communication by placing jumpers to connect the left and middle pins of JMP62 and JMP63 (i.e., place the jumpers toward the “RS232” silkscreen).
   b) Connect a standard DB-9 serial cable between the serial port connector on the DS3106DK and an available serial port on the host computer. (Be sure the cable is a standard straight-through cable rather than a null-modem cable. Null-modem cables prevent proper operation.)
4) Attach the appropriate AC power-supply prongs to the included international power supply.
5) Plug the power supply into an AC power outlet and connect the DC output of the supply to connector J3 (upper-left corner in Figure 1-1).

At this point the power indicator LEDs DS1–DS4 should be lit. Microcontroller status LED DS16 (to the right of the USB connector) should also be lit.

2.1 USB Driver Installation

When the DS3106DK is first connected to the PC using a USB cable, an on-board USB-to-serial converter IC is automatically detected by Windows and the **Found New Hardware Wizard** is automatically started. Follow these steps to install the drivers:

1) In the first screen of this wizard, select **Install from a list or specific location** and click **Next**.
2) In the second screen, select **Search for the best driver in these locations**, check **Include this location in the search**, and browse to the **USB** directory in the DS3106DK CD-ROM or downloaded ZIP file. Click **Next**.
3) Click **Finished**.
4) Repeats steps 1 to 3 the second time the **Found New Hardware Wizard** starts.

After the drivers are installed, whenever the DS3106DK board is connected to a USB port on the PC, the Windows operating system will see the USB-to-serial converter IC as an additional COM port. The DS3106DK software will automatically list the additional COM port in the **PORT** selection combo box in the upper-left corner of the main window.

3. Installing and Running the Software

At this time the DS3106 demo kit software only runs on Windows 2000 or Windows XP operating systems.

To install the demo kit software, run SETUP.EXE from the disk included in the DS3106DK box or from the zip file available on the Microsemi website or from Microsemi timing products technical support.

After software installation is complete, set up the hardware as described above and run the software by double-clicking the **DS3106 Demo Kit** icon on the Windows desktop or by selecting **Start**→**Programs**→**Microsemi**→ **DS3106 Demo Kit**. When the main window appears, select the correct serial port in the box in the upper-left corner. When communication has been properly established between the software and the hardware, the ID field in the upper-left corner should indicate **3106 rev x**, where x = 0 for a revision A1 device, and x = 1 for a revision A2 device.

The demo kit software always starts in demo mode (with the **DEMO MODE** checkbox in the upper-left corner checked) to allow a user to look at the software without having the DK hardware connected to the PC. To connect the software with the demo kit hardware, uncheck the **DEMO MODE** box. The software optionally initializes the DS3106 device and then reads the state of the device to get ready for use.

3.1 Command Line Options

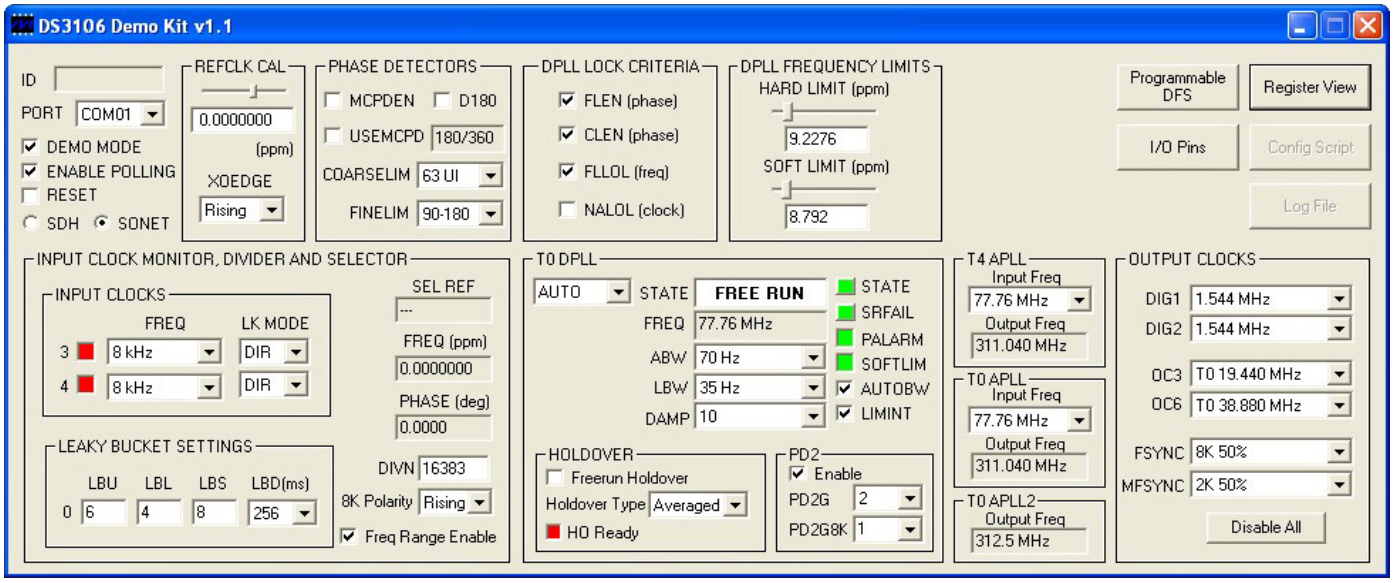
The demo kit software has these command line options:

-l <filepath>	specifies an alternate log file	example: “DS3106DK.exe –l mylog.mfg
-p[port#]	sets the serial (COM) port number	example: “DS3106DK.exe –p2” sets COM2

To add command line options to the DS3106 demo kit shortcut that the installer adds to the desktop, right-click on the shortcut and select **Properties**. In the **Shortcut** tab, at the end of the text in the **Target** text box, add a space followed by the command line option.

4. Overview of the Software Interface

Figure 4-1. Software Main Screen



4.1 Global Configuration

In the upper-left corner of the main window are several global status and configuration fields. The **ID** field displays the device part number and revision. The **PORT** field shows the COM port to which the DK board is connected. The **DEMO MODE** checkbox, which is checked by default, must be unchecked to enable the software to communicate with the DK board. The **ENABLE POLLING** checkbox, also checked by default, controls software polling of the device. The **RESET** checkbox controls MCR1:RESET in the device. Finally, the **SDH** and **SONET** radio buttons (which control device register field MCR3:SONSDH) specify whether 1.544MHz (SON) or 2.048MHz (SDH) is an available frequency option for input clocks IC3 and IC4.

4.2 Input Clock Monitor, Divider, and Selector

This box occupying the lower left section of the main window contains the configuration and status associated with input clocks IC3 and IC4.

Just to the right of the input clock numbers 3 and 4 are software LEDs that indicate the state of each input as reported by its input monitor. These LEDs are red in the absence of any other condition. When a clock of the correct frequency is applied to an input, the associated LED turns green when activity is detected. If an input is disqualified by one of the DPLLs because the DPLL could not lock to it, the LED turns magenta.

In the middle of the box, the **FREQ** and **LK MODE** fields configure the frequency and lock mode (direct-lock, DIVN, LOCK8K, or alternate direct-lock) for each input clock. Near the lower right corner is a field to configure the DIVN divider used for inputs configured for DIVN mode.

The **SEL REF** field shows the selected reference for the DPLL. (Reminder: The DS3106 only supports manual switching between IC3 and IC4, controlled by the SRCSW pin.) The **FREQ** and **PHASE** fields show the real-time frequency and phase reported by the DPLL.

The field labeled **8K Polarity** specifies the significant edge that the DS3106 will lock to when the input clock is 8kHz. The **Freq Range Enable** checkbox controls whether the DS3106 checks the input clocks for frequency accuracy (within 10,000ppm).

Table 4-1. Mapping Between Input Clock Software Fields and DS3106 Register Fields

SOFTWARE FIELD	DS3106 REGISTER FIELDS
Input Clock Status LEDs 3 and 4	ISR2 register LED red when ACT = 1, LOCK = 0 LED green when ACT = 0, LOCK = 0 LED magenta when LOCK = 1
FREQ 3 and 4	ICR3 and ICR4:FREQ[3:0]
LK MODE 3 and 4	ICR3 and ICR4:LOCK8K, and DIVN
SEL REF	PTAB1:SELREF
FREQ (ppm)	FREQ1, FREQ2, and FREQ3 registers concatenated
PHASE (deg)	PHASE1 and PHASE2 register concatenated
LEAKY BUCKET SETTINGS	LBxU, LBxL, BLxS, LBxD (x = 1 to 4)
DIVN	DIVN1, DIVN2
8K Polarity	TEST1:8KPOL
Freq Range Enable	MCR1:FREN

4.3 T0 DPLL

The state of the T0 DPLL (free-run, locked, holdover, etc.) is shown in the **STATE** text box. The **STATE** and **SRFAIL** buttons represent latched status bits in the device. When the button is red, the corresponding latched status bit has been set in the DS3106. Pressing the button clears the latched status bit and changes the color of the button back to green. The **STATE** button indicates that the state of the T0 DPLL has changed since the last time the button was pressed. **SRFAIL** indicates that the selected reference has failed since the last time the button was pressed. The state of the T0 DPLL can be forced using the combo box to the left of the **STATE** text box.

The frequency of the T0 DPLL is displayed in the **FREQ** field (fixed at 77.76MHz for the DS3106 T0 DPLL). The acquisition and locked bandwidths are set by the **ABW** and **LBW** fields, respectively, and the damping factor is set by the **DAMP** field. The acquisition bandwidth is only used if **AUTOBW** is checked. If the frequency of the T0 DPLL's selected reference exceeds the **SOFT LIMIT** setting (in the **DPLL FREQUENCY LIMITS** box at the top of the main window), the **SOFTLIM** LED turns red.

When the **Freerun Holdover** box is checked, the T0 DPLL will holdover at 0ppm with respect to the REFCLK oscillator rather than at the long-term frequency average of the last valid input clock. When the **Freerun Holdover** box is not checked, holdover type can be set to instant or averaged. The **PALARM** status LED and the phase detector 2 (**PD2**) fields are advanced topics. See Table 4-2 and the DS3106 data sheet for more details.

Table 4-2. Mapping Between T0 DPLL Software Fields and DS3106 Register Fields

SOFTWARE FIELD	DS3106 REGISTER FIELDS
STATE combo box	MCR1:T0STATE
STATE status box	OPSTATE:T0STATE
FREQ	Fixed by T0 DPLL architecture
ABW	T0ABW
LBW	T0LBW
DAMP	T0CR2:DAMP
STATE latched status button	MSR2:STATE
SRFAIL	MSR2:SRFAIL
PALARM	TEST1:PALARM
SOFTLIM	OPSTATE:T0SOFT
AUTOBW	MCR9:AUTOBW
LIMINT	MCR9:LIMINT
Freerun Holdover	MCR3:FRUNHO
Holdover Type	HOCR3:AVG
HO Ready	VALSR2:HORDY
PD2 Enable	T0CR3:PD2EN
PD2G	T0CR3:PD2G
PD2G8K	T0CR2:PD2G8K

4.4 T0 APLL and T0 APLL2

The **Input Freq** field configures the frequency of the T0 APLL DFS (refer to the DS3106 data sheet for details). The APLL output frequency is always four times the input frequency. When the **Input Freq** field is changed, the **Output Freq** field changes to match, and all the T0 options in the OC3 and OC6 output clock combo boxes also change to frequencies derived from the new T0 APLL frequency. These changes match what happens in the DS3106.

In normal operation the T0 APLL2 has a fixed output frequency of 312.5MHz (twice the standard XGMII clock rate). The rate is displayed in the **T0 APLL2 Output Freq** text box.

Whenever the T0 APLL DFS or the T0 APLL2 DFS are configured for programmable DFS operation (see Section 4.9), their respective **Input Freq** and **Output Freq** fields specify their frequencies with a "P" prefix to indicate that programmable DFS mode is enabled.

Table 4-3. Mapping Between T0 APLL Software Fields and DS3106 Register Fields

SOFTWARE FIELD	DS3106 REGISTER FIELDS
Input Freq	T0CR1:T0FREQ
Output Freq	Derived by software from Input Freq

4.5 T4 APLL

The **Input Freq** field in the **T4 APLL** box configures the frequency of the T4 APLL DFS (refer to the DS3106 data sheet for details). The APLL output frequency is always four times the input frequency. When the **Input Freq** field is changed, the **Output Freq** field changes to match, and all the T4 options in the OC3 and OC6 output clock combo boxes also change to frequencies derived from the new T4 APLL frequency. These changes match what happens in the DS3106.

Whenever the T4 APLL DFS is configured for programmable DFS operation (see Section 4.9), the **Input Freq** and **Output Freq** fields specify their frequencies with a "P" prefix to indicate that programmable DFS mode is enabled for the T4 APLL DFS.

Table 4-4. Mapping Between T4 APLL Software Fields and DS3106 Register Fields

SOFTWARE FIELD	DS3106 REGISTER FIELDS
Input Freq	T0CR1:T0FT4
Output Freq	Derived by software from Input Freq

4.6 Output Clocks

The fields in the **OUTPUT CLOCKS** box configure the DS3106's output clocks. The **DIG1** and **DIG2** fields configure the Digital1 and Digital2 frequency options for OC3 and OC6 (refer to the DS3106 data sheet for details).

The **OC3** and **OC6** fields specify the output frequencies for outputs OC3 and OC6. Note that when the T0 APLL setting is changed, the frequencies of all the T0 options in the **OC3** and **OC6** fields automatically change to frequencies derived from the new T0 APLL frequency. Similarly, when the T4 APLL setting is changed, the frequencies of all the T4 options in the **OC3** and **OC6** fields automatically change to frequencies derived from the new T4 APLL frequency. These changes match what happens in the DS3106.

Whenever the T0 APLL DFS, T4 APLL DFS, or T0 APLL2 DFS are configured for programmable DFS operation (see Section 4.9), the T0, T4, and T02 options, respectively, in the **OC3** and **OC6** fields change to frequencies derived from the programmable DFS settings. These options all have a "P" prefix, for example, "PT0" or "PT4" to indicate that they are controlled by the programmable DFS mode. Similarly, whenever the DIG1 DFS or the DIG2

DFS are configured for programmable DFS operation, the **DIG1** and **DIG2** fields change to display the programmable DFS frequency with a “P” prefix.

FSYNC is an 8kHz output that can be configured as a 50% duty cycle clock or a frame pulse and can optionally be inverted. **MFSYNC** is a 2kHz output that can be similarly configured.

Table 4-5. Mapping Between Output Clock Software Fields and DS3106 Register Fields

SOFTWARE FIELD	DS3106 REGISTER FIELDS
DIG1	MCR6:DIG1SS, MCR7:DIG1F
DIG2	MCR6:DIG2SS, MCR7:DIG2F, MCR7:DIG2AF
OC3 and OC6	OCR2 and OCR3
FSYNC	OCR4:FSEN, FSCR1:8KPUL, FSCR1:8KINV
MFSYNC	OCR4:MFSEN, FSCR1:2KPUL, FSCR1:2KINV

4.7 DPLL Frequency Limits, Phase Detectors, DPLL Lock Criteria

The DPLL frequency limits specify the hard and soft limits of the T0 DPLL frequency range. When the selected reference exceeds the soft limit, the **SOFTLIM** LED turns red but the selected reference is not disqualified. If the **FLLOL** (frequency limit loss of lock) box is checked in the **DPLL LOCK CRITERIA** box, when the selected reference exceeds the hard limit the DPLL will lose lock (transition to LOL state).

The remaining fields are advanced topics. See Table 4-6 and the DS3106 data sheet for more details.

Table 4-6. Mapping Between DPLL Software Fields and DS3106 Register Fields

SOFTWARE FIELD	DS3106 REGISTER FIELDS
MCPDEN	PHLIM2:MCPDEN
USEMCPD	PHLIM2:USEMCPD
D180	TEST1:D180
COARSELIM	PHLIM2:COARSELIM
FINELIM	PHLIM1:FINELIM
FLEN	PHLIM1:FLEN
CLEN	PHLIM2:CLEN
FLLOL	DLIMIT3:FLLOL
NALOL	PHLIM1:NALOL
HARD LIMIT	HARDLIM[9:0] in DLIMIT1 and DLIMIT2
SOFT LIMIT	DLIMIT3:SOFTLIM

4.8 REFCLK Calibration

Any known frequency error in the local oscillator can be calibrated out inside the DS3106 by setting the ppm value in the **REFCLK CAL** box. Also, the significant edge of the REFCLK signal can be selected in **XOEDGE** field.

Table 4-7. Mapping Between REFCLK Software Fields and DS3106 Register Fields

SOFTWARE FIELD	DS3106 REGISTER FIELDS
REFCLK slider/text box	MCLKFREQ[15:0] in MCLK1 and MCLK2
XOEDGE	MCR3:XOEDGE

4.9 Programmable DFS

When the **Programmable DFS** button in the upper-right corner of the main window is pressed, the **Programmable DFS** window appears (Figure 4-2). In this window one or more of the output DFS engines in the DS3106 can be configured to synthesize a custom frequency that is a multiple of 2kHz (f < 77.76MHz) or a multiple of 8kHz (f ≤ 311.04MHz). The desired frequency can be entered in the **Target Output Clock Frequency (MHz)** box at the top of the window, and the software will perform the necessary computations to fill in the other numerical fields in window.

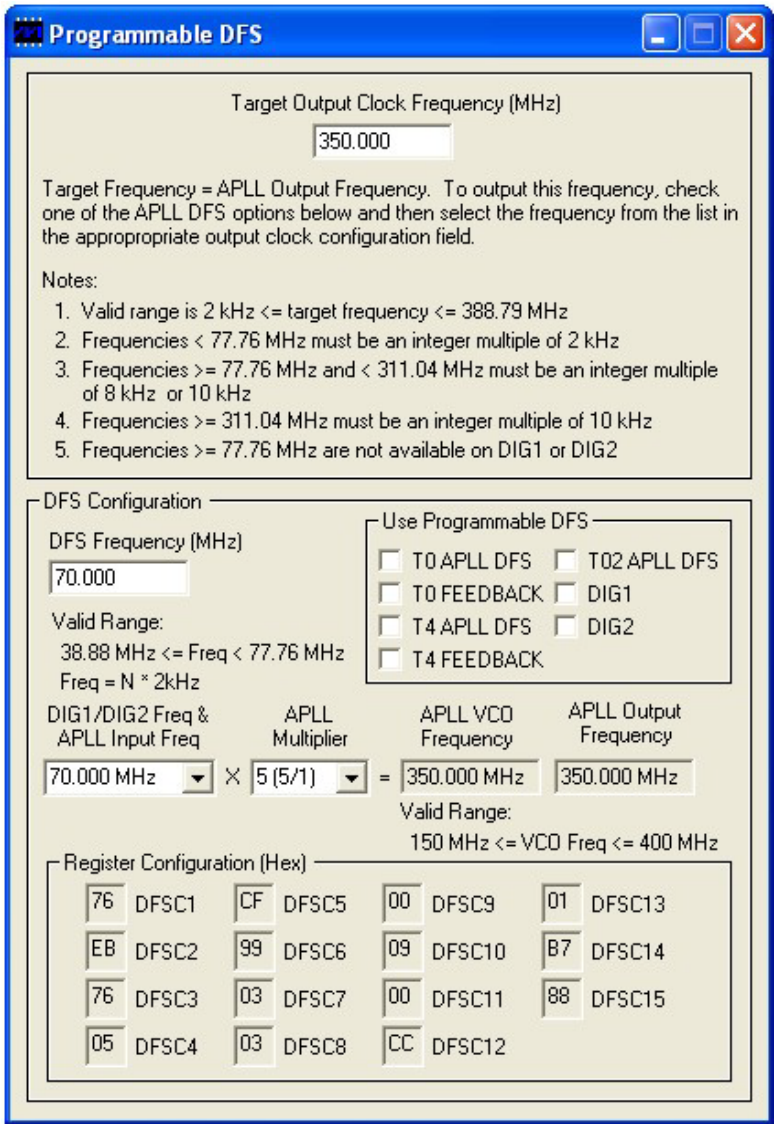
The programmable DFS configuration can be applied to one or more DFS engines as specified in the **Use Programmable DFS** box. Frequencies below 77.76MHz are typically synthesized by the DIG1 or DIG2 DFS engine and brought out on CMOS/TTL output clock pin(s) by selecting **DIG1** or **DIG2** in the appropriate output clock configuration field in the main window of the software. Frequencies of 77.76MHz or above must be synthesized using an APLL DFS and its associated APLL, and are typically brought out on differential output clock pin(s).

If a group of custom clock rates that are related to one another by factors of 1, 2, 4, 6, 8, 10, 12, 16, 20, 48, or 64 are needed, often the highest frequency clock can be produced through one of the APLL DFS blocks and then various lower rate clocks can be selected on one or more of the output pins. Refer to the OCR2 and OCR3 registers in the DS3106 data sheet for details.

If the software-computed values for **DFS Frequency (MHz)**, **DIG1/DIG2 Freq & APLL Input Freq**, or **APLL Multiplier** are manually overridden, the user must manually ensure that the **DFS Frequency (MHz)** falls within its allowed range and that the **APLL VCO Frequency** falls within its allowed range. Note that the **APL VCO Frequency** does not need to be within its allowed range if none of the APLL DFS blocks are selected for use.

The **Register Configuration** section of the **Programmable DFS** window shows the values that are written to the DFSC1–DFSC15 registers to get the configuration specified in the upper part of the window. DFSC1–DFSC15 are located at device addresses 1E0h–1EEh, respectively.

Figure 4-2. Software-Programmable DFS Window



4.10 I/O Pins

The fields in this window configure the general-purpose I/O available on the DS3106. See Figure 4-3, Table 4-8, and the DS3106 data sheet for details.

Figure 4-3. Software I/O Pins Window

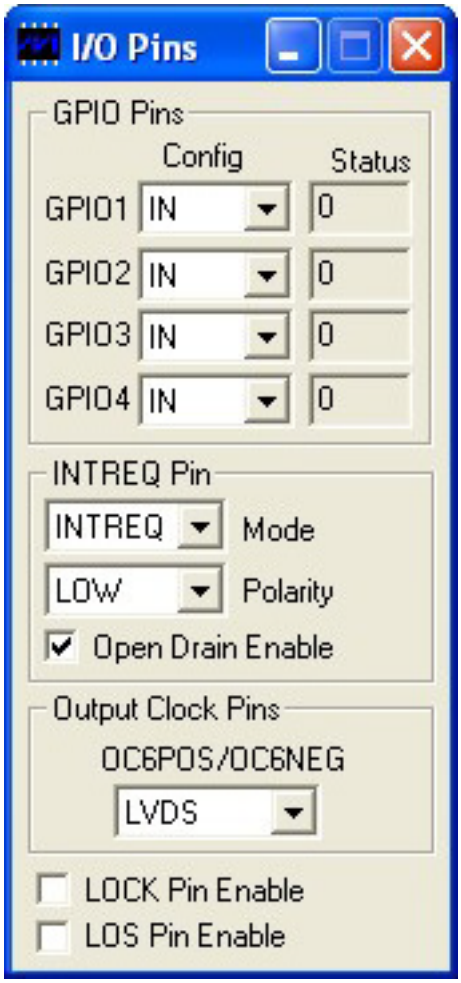


Table 4-8. Mapping Between I/O Pins Software Fields and DS3106 Register Fields

SOFTWARE FIELD	DS3106 REGISTER FIELDS
GPIO1 to GPIO4 Config	GPCR:GPIOxD and GPIOxO
GPIO1 to GPIO4 Status	GPSR:GPIOx
INTREQ Mode	INTCR:LOS, GPO
INTREQ Polarity	INTCR:POL
INTREQ Open Drain Enable	INTCR:OD
LOCK Pin Enable	MCR1:LOCKPIN
LOS Pin Enable	MCR10:SRFPIN
OC6POS/OC6NEG Format	MCR8:OC6SF

4.11 Register View Window

When the **Register View** button in the upper-right corner of the main window is pressed, the **Register View** window appears (Figure 4-4). In this window the DS3106's entire register set can be viewed and manually written as needed.

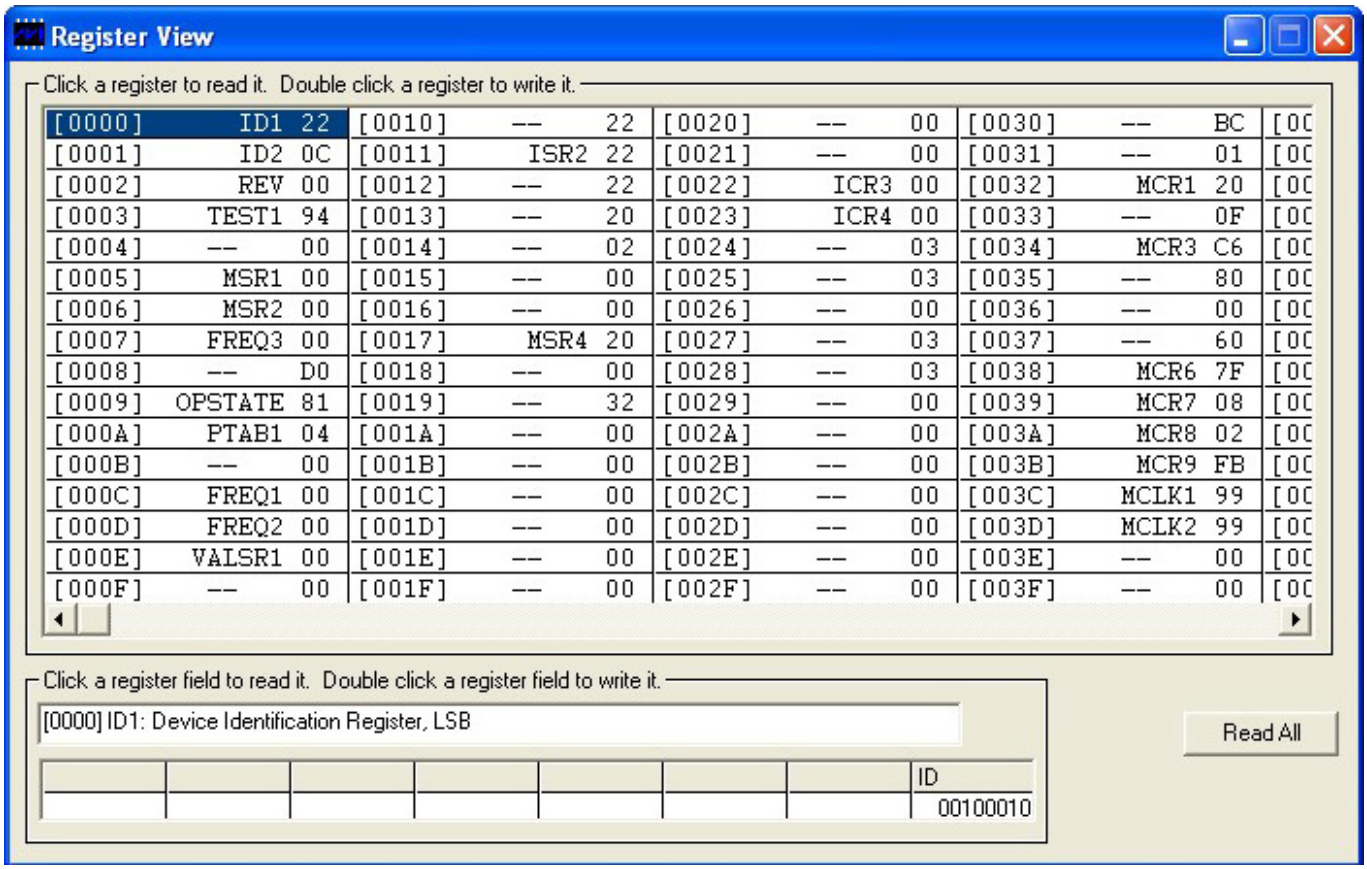
The large grid that takes up most of the window displays the DS3106 register map. For each register, its hexadecimal address in square brackets is followed by its register name and its contents in two-digit hex format.

When a register is clicked in the main register grid, its register description and fields are displayed at the bottom of the window. Due to the limited speed of the serial port, the demo kit software does not continually poll every register and does not make real-time updates to the data displayed on the **Register View** screen. Registers can be manually read as described below.

The **Register View** window supports the following actions:

- **Read a register.** Select the register in the register map.
- **Read a register field.** Select the register in the map or the register field at the bottom of the window.
- **Read all registers.** Press the **Read All** button.
- **Write a register.** Double-click the register name in the register map and enter the value to be written.
- **Write a register field.** Select the register, double-click the field, and enter the value to be written.
- **Write a multiregister field.** Double-click one of the register names and enter the value for the field.

Figure 4-4. Software Register View Window



4.12 Configuration Scripts and Log File

4.12.1 Configuration Log File

Every write command issued by the software to the DS3106DK board is logged in file DS3106DKLog.mfg located in the same directory as the software executable. This file can be viewed in Notepad by pressing the **Log File** button in the upper-right corner of the main window. Command line option "-l <filepath>" can be used to cause the software to write to a file other than DS3106DKLog.mfg.

4.12.2 Configuration Scripts

All or part of the text in the configuration log file can be copied to a text file with a .mfg file extension for use as a configuration script. Configuration scripts are useful for quickly configuring the DS3106 without having to remember all the required settings.

Two types of configuration scripts are possible: full and partial. A full configuration script can start with the DS3106 in its power-on default state and configure every aspect of the device to bring it to a desired state. To make a full configuration script, run the software, uncheck the **Demo Mode** checkbox, initialize the device, configure the device using the DK software fields, press the **Log File** button, and use **File→Save As** in Notepad to save a copy of the entire log file to a different file name.

A partial configuration file only affects a subset of the DS3106 device settings. To make a partial configuration script, press the **Log File** button to view the log file, press **Ctrl-End** to jump to the end of the file, and add to the end of the file a carriage return or comment line (starting with a semicolon) to delimit the start of the desired configuration. Then save and exit the log file. Next, configure the device using the DK software fields. Finally, view the log file again, jump to the end, and copy everything from the delimiter to the end of the file into a new .mfg file.

To run a configuration script, press the **Config Script** button in the upper-right corner of the main window. In the script window, type the path to the file or press the **Browse** button to navigate to the file.

Note that when the **Demo Mode** checkbox is unchecked, during the **Initializing the DS3106** step, the software runs configuration script startup.mfg located in the same directory as the software executable. The startup.mfg file can be edited or replaced as needed to change the initial configuration of the device. Be aware, however, that the section of the startup.mfg file labeled **Required Initialization** must be executed after device power-up or reset for the DS3106 to operate correctly.

5. Appendix 1: Hardware Components

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1, C2, C5, C6, C9–C12, C15, C42, C59–C138, C140, C142, C143, C145, C147, C151, C155, C163–C166, C168, C169	103	0.1µF ±20% 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
C3, C13 ,C14, C16, C41	5	4.7µF ±10%, 25V X5R ceramic capacitors (1206)	PAN	ECJ-3YB1E475K
C4, C17, C18, C20	4	6.8µF ±10%, 6.3V X5R ceramic capacitors (1206)	PAN	ECJ-3YB0J685K
C7	1	68µF ±20%, 16V tantalum capacitor (D case)	PAN	ECS-T1CD686R
C8	1	0.01µF ±10%, 50V X7R ceramic capacitor (0603)	AVX	06035C103KAT
C19	1	100µF ±20%, 4V ceramic capacitor (1206)	TAI	AMK316BJ107ML-T
C34–C38, C51–C58, C139, C141, C153, C154	17	10µF ±20%, 10V ceramic capacitors (1206)	PAN	ECJ-3YB1A106M
C39, C40	2	22pF ±10%, 100V ceramic capacitors (1206)	AVX	12061A220KAT2A
C43	1	1µF ±10%, 16V ceramic capacitor (1206)	PAN	ECJ-3YB1C105K
D1	1	DIODE 1A 50V GEN PURPOSE SILICON	GEN	1N4001
D2, D7	2	SCHOTTKY DIODE, 1 AMP 40 VOLT	IRF	10BQ040
DS1–DS4, DS6	5	SMD green LEDs	PAN	LN1351C
DS5, DS10	2	SMD red LEDs	PAN	LN1251C
DS16	1	SMD green LED	PAN	LN1351C
J1, J6, J7, J22, J27, J40, J41	7	CONNECTOR, SMB, 50 OHM VERTICAL, 5PIN	AMP	413990-1
J3	1	CONN 2.1MM/5.5MM PWRJACK RT ANGLE PCB, closed frame, high current 24VDC@5A	CUI, INC	PJ-002AH
J13	1	SOCKET, BANANA PLUG, HORIZONTAL, RED	MSR	164-6219
J14	1	CONNECTOR, SMB, 50 OHM VERTICAL, 5PIN, DO NOT POPULATE	AMP	413990-1
J19	1	SOCKET, BANANA PLUG, HORIZONTAL, BLACK	MSR	164-6218
J50	1	CONN, DB9 RA, LONG CASE	AMP	747459-1
J51	1	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	NA	NA
J54	1	CONN, USB, TYPE B SINGLE RT ANGLE, BLACK	MOL	67068-0000
JMP1–JMP6, JMP9–JMP12, JMP16	11	L_HEADER, 3-PIN, .100 CENTERS, VERTICAL	STC	TSW-103-07-T-S
JMP7, JMP8, JMP36, JMP37	4	L_2 PIN HEADER, .100 CENTERS, VERTICAL	STC	TSW-102-07-T-S
JMP13, JMP14, JMP15	3	DO NOT PLACE, SHORTED 2PIN TH JUMPER	NA	NA
JMP62, JMP63	2	L_3 PIN HEADER, .100 CENTERS, VERTICAL	STC	TSW-103-07-T-S
R1–R4, R17, R19, R20, R25–R27, R33, R34, R41, R43, R45, R47–R63, R111, R112, R117, R118	36	L_RES 0603 0 Ohm 1/16W 1%	AVX	CJ10-000F

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R5, R11, R13, R15, R21–R24, R29–R32, R65–R68	16	L_RES 0603 51.1 Ohm 1/16W 1%	PAN	ERJ-3EKF51R1V
R6	1	RES 0603 100K Ohm 1/16W 5%	PAN	ERJ-3GEYJ104V
R7, R9, R10, R12, R14, R84, R110, R113, R115, R116, R120–R123	14	L_RES 0603 10K Ohm 1/16W 5%	PAN	ERJ-3GEYJ103V
R8, R16, R18, R46, R64, R83, R100, R101, R102	9	RES 0603 DO NOT POPULATE	NA	NA
R28	1	RES 0603 33.2 Ohm 1/16W 1%	PAN	ERJ-3EKF33R2V
R35–R40, R42, R44, R94, R108	10	L_RES 0603 330 Ohm 1/16W 5%	PAN	ERJ-3GEYJ331V
R97	1	RES 0603 20K Ohm 1/16W 5%	PAN	ERJ-3GEYJ203V
SW1	1	SWITCH DPDT SLIDE 6PIN TH	TYC	SSA22
SW5	1	SWITCH MOM 4PIN SINGLE POLE	PAN	EVQPAE04M
TP1–TP22, TP49–TP60, TP65–TP84	54	Test Points, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U1, U2, U5, U13, U14, U23, U24, U28	8	L_TINYLOGIC HIGH SPEED 2-INPUT OR GATE, 5 PIN SOT23	FAI	NC7SZ32M5
U3	1	IC, LINE CARD TIMING, -40°C to +85°C, 64 PIN QFP	DAL	DS3106
U4, U6	2	LINEAR REGULATOR, 3.3V, 16 PIN TSSOP-EP	MAX	MAX1793EUE-33
U7, U25	2	L_TINYLOGIC HIGH SPEED 2-INPUT XOR GATE, 5 PIN SOT23	FAI	NC7SZ86M5
U8	1	LINEAR REGULATOR, 1.8V, 16 PIN TSSOP-EP	MAX	MAX1793EUE-18
U26	1	IC, LINEAR REGULATOR, 1.5W, 2.5V OR ADJ, 1A, 16 PIN TSSOP-EP	MAX	MAX1793EUE-25
U29	1	IC, TCXO, 12.8MHz, 0°C to +70°C, 16-PIN SOIC, DO NOT POPULATE	DAL	DS4026+BCC
U35	1	IC, LINE CARD TIMING WITH SYNCHRONOUS ETHERNET SUPPORT, -40 TO 85C, 81 PIN BGA, DO NOT POPULATE	DAL	NOT POPULATED
U41	1	DUAL RS232 XMITR/RCVR 16 PIN SOIC (300 MIL)	DAL	DS232AS
U42	1	HIGH SPEED MICRO 44-PIN TQFP 0°C to +70°C	DAL	DS87C520-ECL
U44	1	MICROPROCESSOR VOLTAGE MONITOR, 3.08V RESET, 4PIN SOT143	MAX	MAX811TEUS-T
U45	1	MICROPROCESSOR VOLTAGE MONITOR, 4.38V RESET, 4PIN SOT143	MAX	MAX812MEUS-T
U46	1	IC, SINGLE-CHIP USB TO UART BRIDGE, 28 PIN QFN	SIL	CP2101

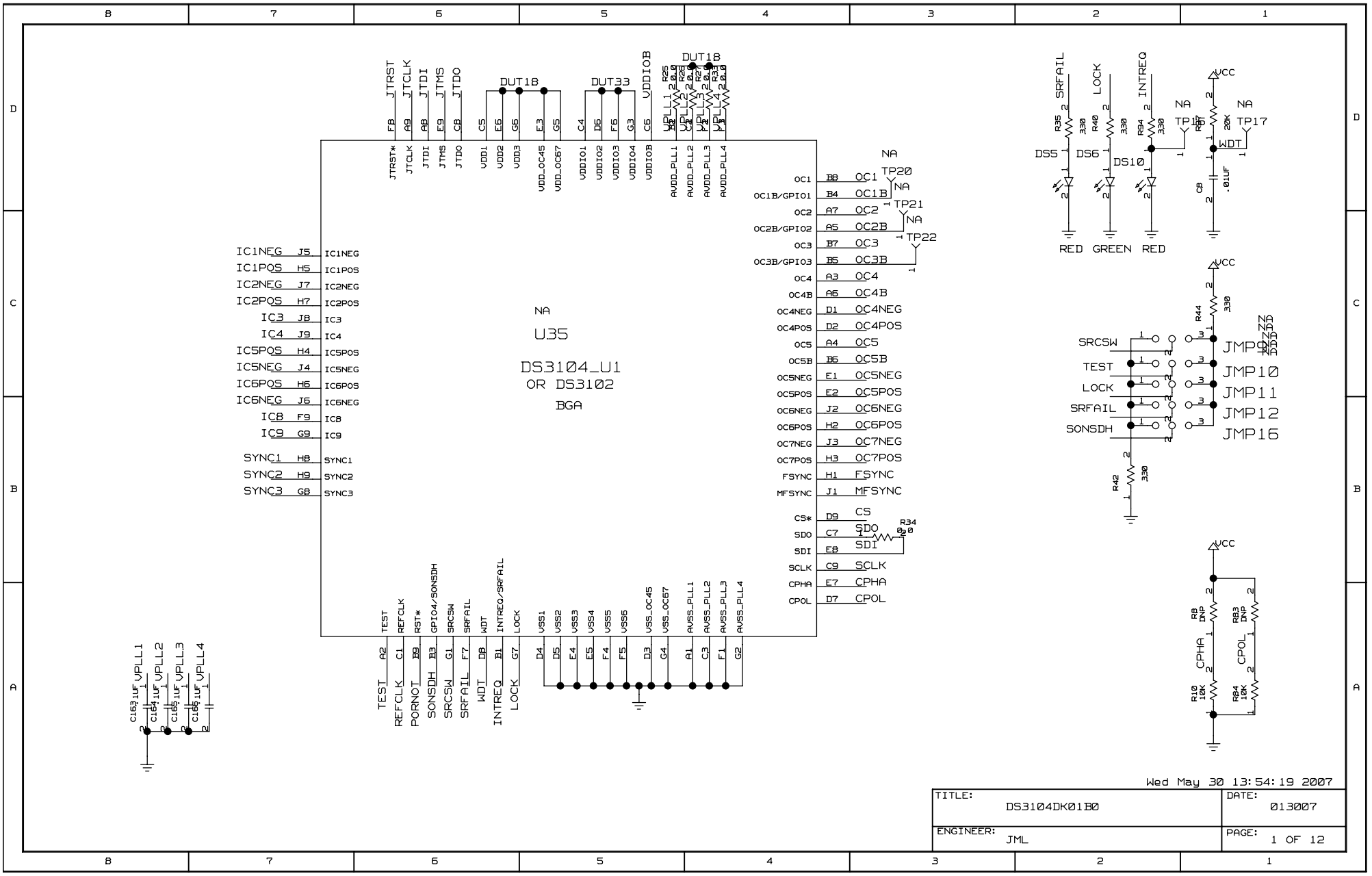
DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
Y1	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 12.8MHz, DO NOT POPULATE	SAR	NTH069A3-12.8
Y2	1	OSCILLATOR, RAKON TCXO, 3.3V, 12.8MHz, 4 PIN SMD	RAK	E4837LF
Y3	1	OSCILLATOR, CRYSTAL CLOCK XO 1613, 3.3V CMOS, LOW JITTER-12.8MHz, 4-PIN SMD, DO NOT POPULATE	SAR	S1613A-12.8000
Y4	1	OSCILLATOR, CRYSTAL CLOCK XO 1633, 3.3V CMOS, LOW JITTER-12.8MHz, 4-PIN SMD, DO NOT POPULATE	SAR	S1633A-12.8000
Y7	1	XTAL, LOW PROFILE, 11.0592MHz	PLE	LP49-33-11.0592M

6. Appendix 2: Schematics

The schematics are featured in the following pages.

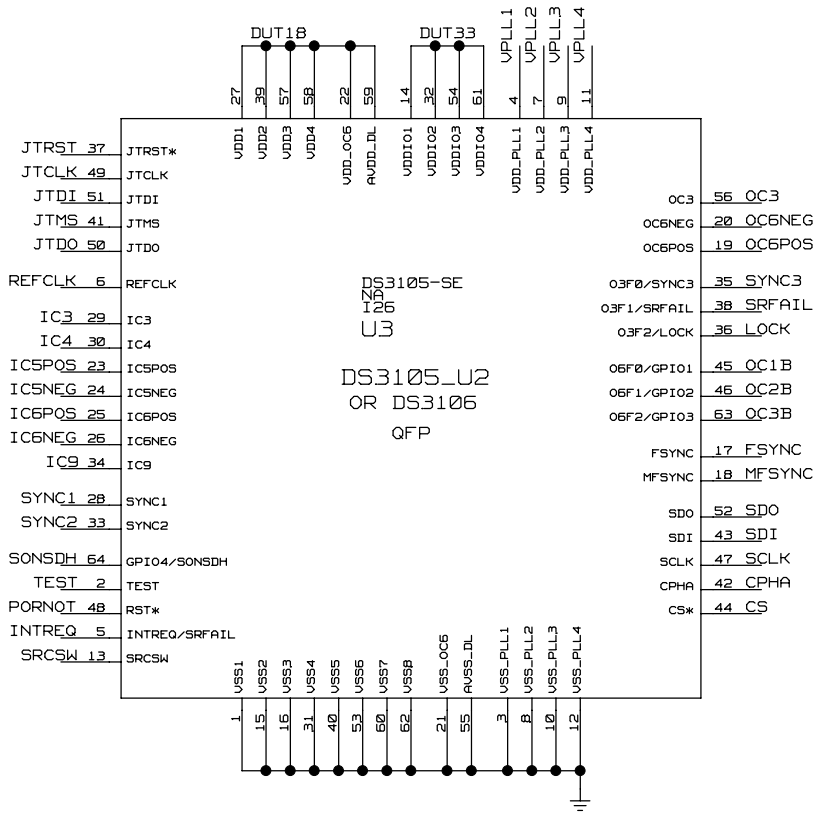
7. Document Revision History

REVISION DATE	DESCRIPTION
012208	Initial release.
2012-05	Reformatted for Microsemi. No content change.



Wed May 30 13:54:19 2007

TITLE: DS3104DK01B0	DATE: 013007
ENGINEER: JML	PAGE: 1 OF 12

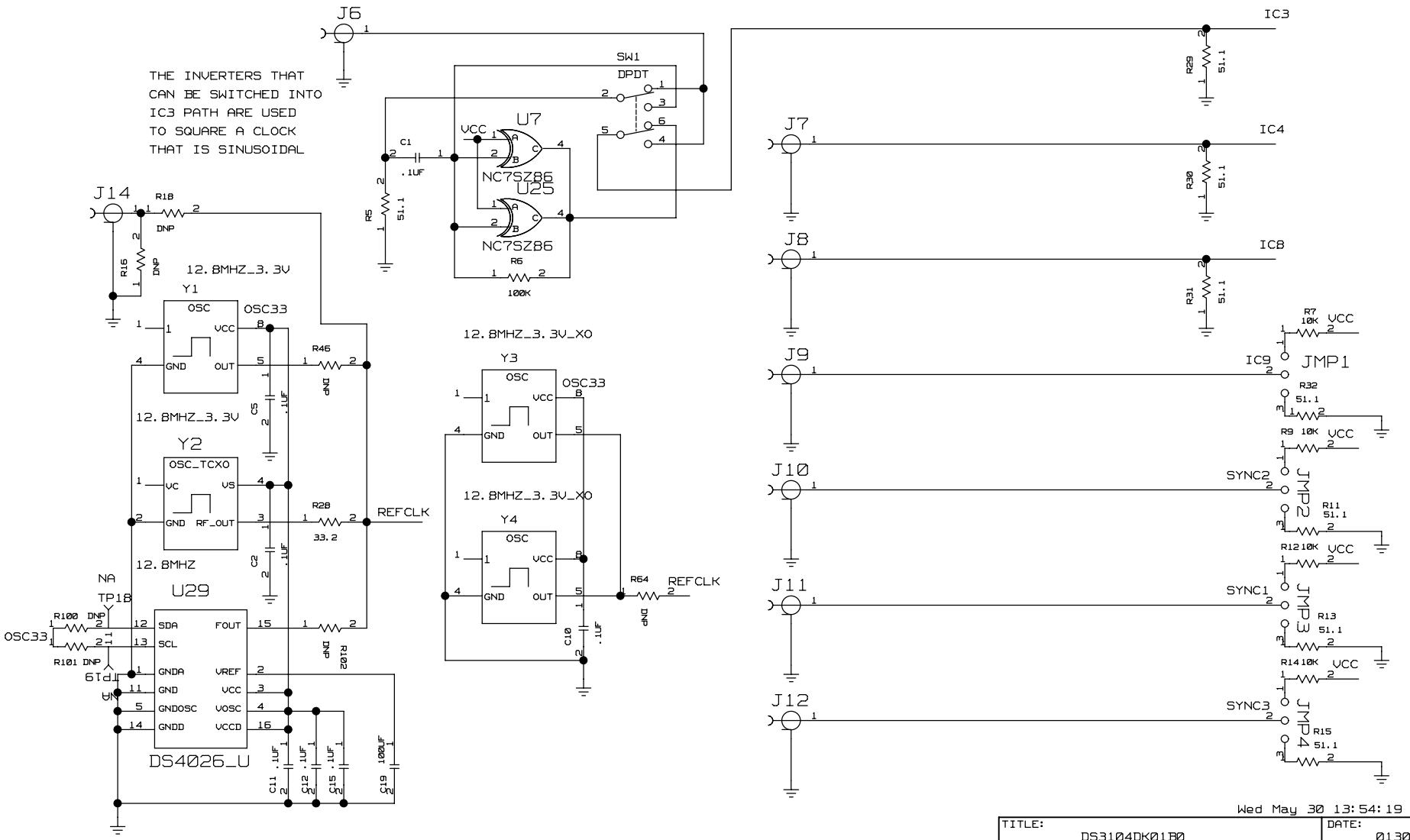


Wed May 30 13:54:21 2007

TITLE: DS3104DK01B0	DATE: 013007
ENGINEER: JML	PAGE: 2 OF 12

ALL SIGNAL TRACKS ARE 50 OHM WITH RESPECT TO PLANE

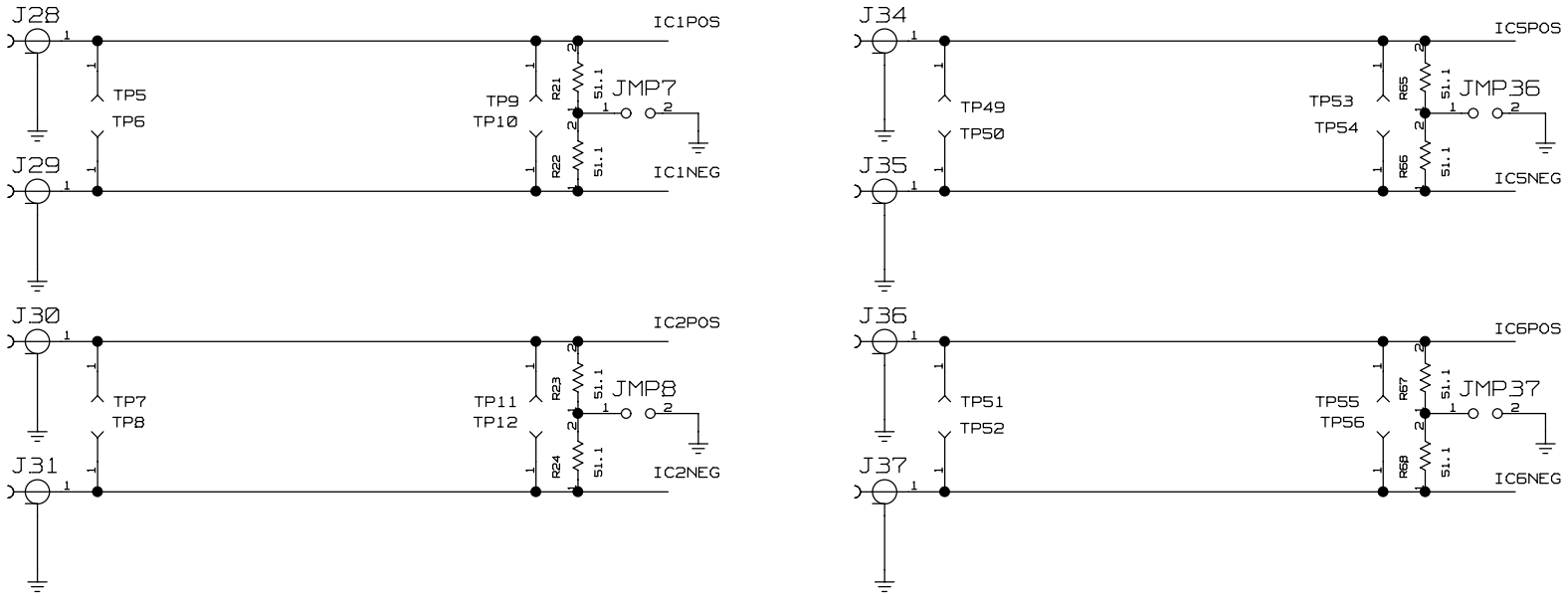
THE INVERTERS THAT CAN BE SWITCHED INTO IC3 PATH ARE USED TO SQUARE A CLOCK THAT IS SINUSOIDAL



Wed May 30 13:54:19 2007

TITLE: DS3104DK01B0	DATE: 013007
ENGINEER: JML	PAGE: 3 OF 12

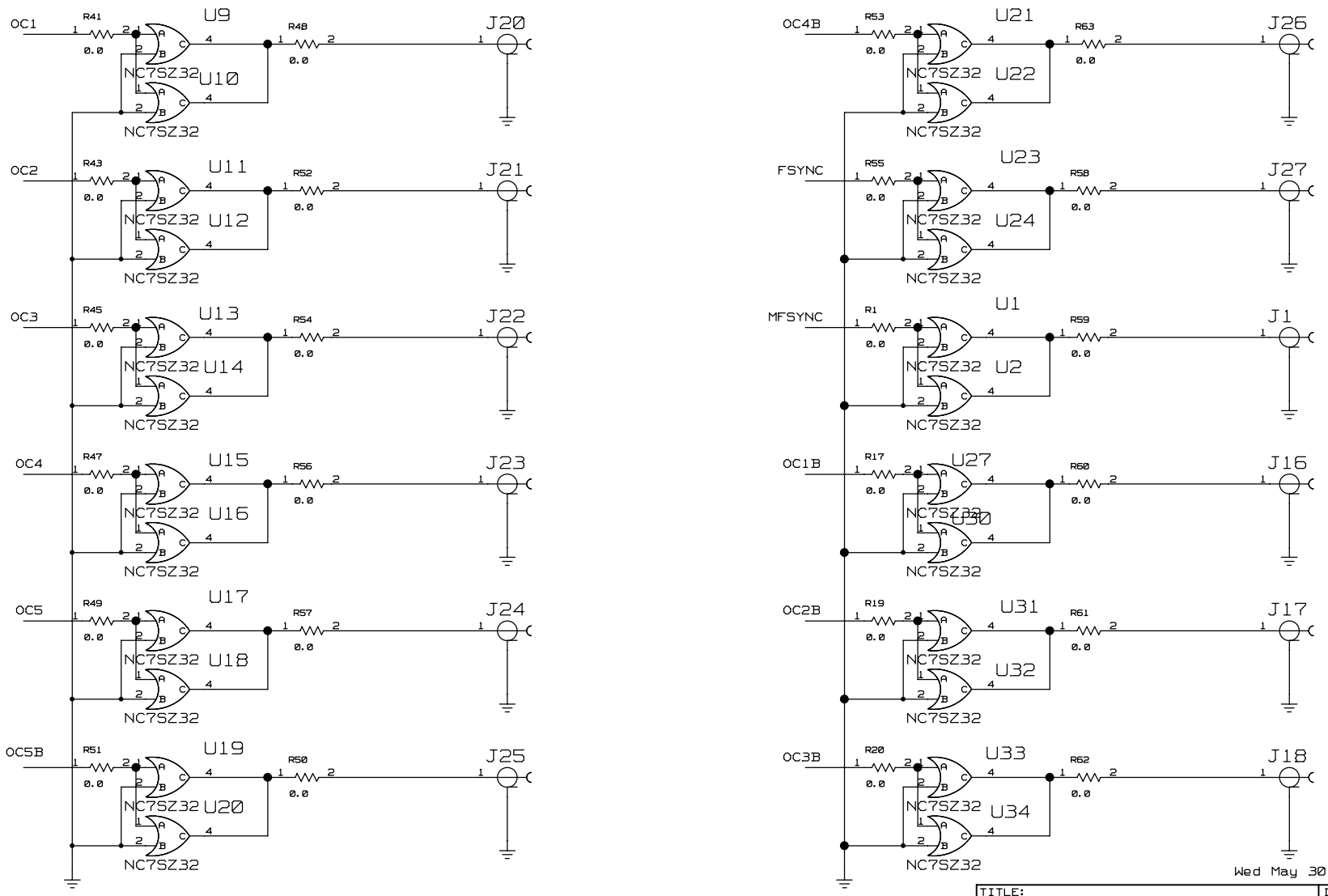
ALL SIGNAL TRACKS ARE 50 OHM WITH RESPECT TO PLANE



INPUT CLOCKS

Wed May 30 13:54:20 2007

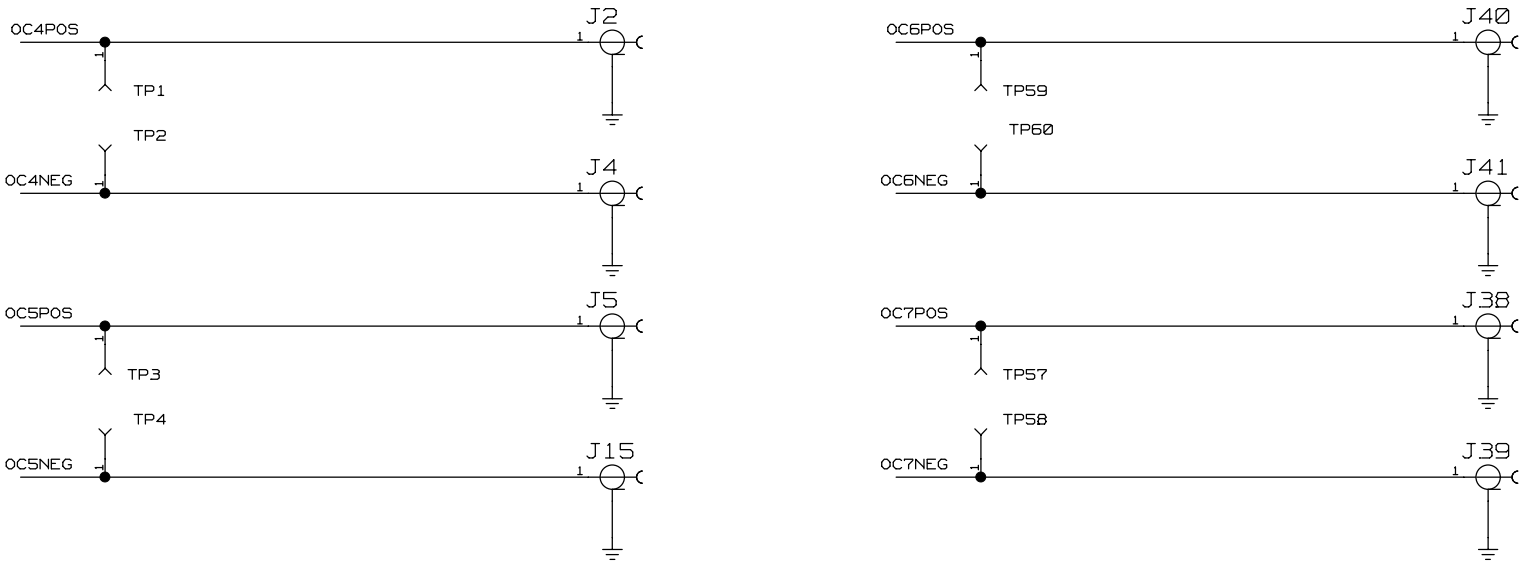
TITLE: DS3104DK01B0	DATE: 013007
ENGINEER: JML	PAGE: 4 OF 12



OUTPUT CLOCKS

Wed May 30 13:54:20 2007

TITLE: DS3104DK01B0	DATE: 013007
ENGINEER: JML	PAGE: 5 OF 12



Thu Feb 15 16:29:11 2007

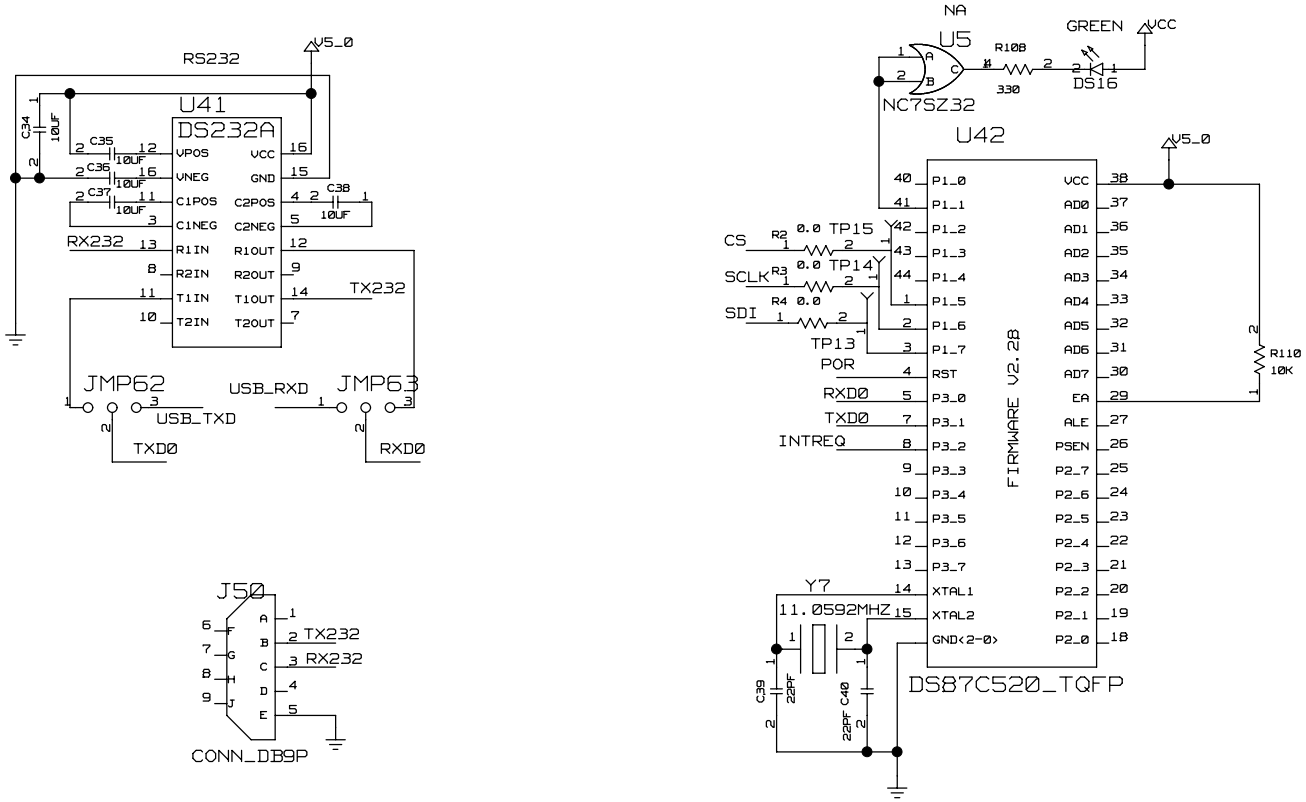
TITLE: DS3104DK01B0	DATE: 013007
ENGINEER: JML	PAGE: 6 OF 12

OUTPUT CLOCKS

INTENTIONALLY LEFT BLANK

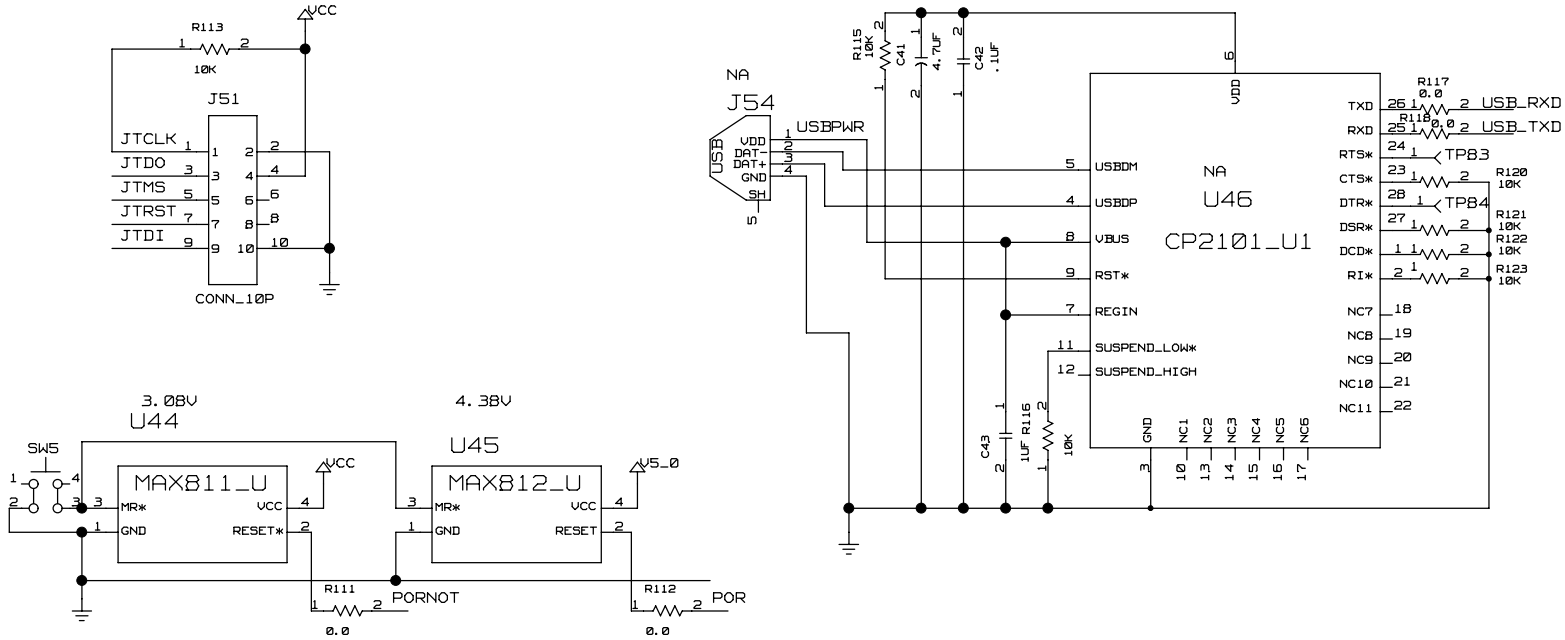
Wed Feb 21 13:57:17 2007

TITLE: DS3104DK01B0	DATE: 013007
ENGINEER: JML	PAGE: 7 OF 12



Wed May 30 13:54:18 2007

TITLE: DS3104DK01B0	DATE: 013007
ENGINEER: JML	PAGE: 8 OF 12



Wed May 30 13:54:19 2007

TITLE: DS3104DK01B0	DATE: 013007
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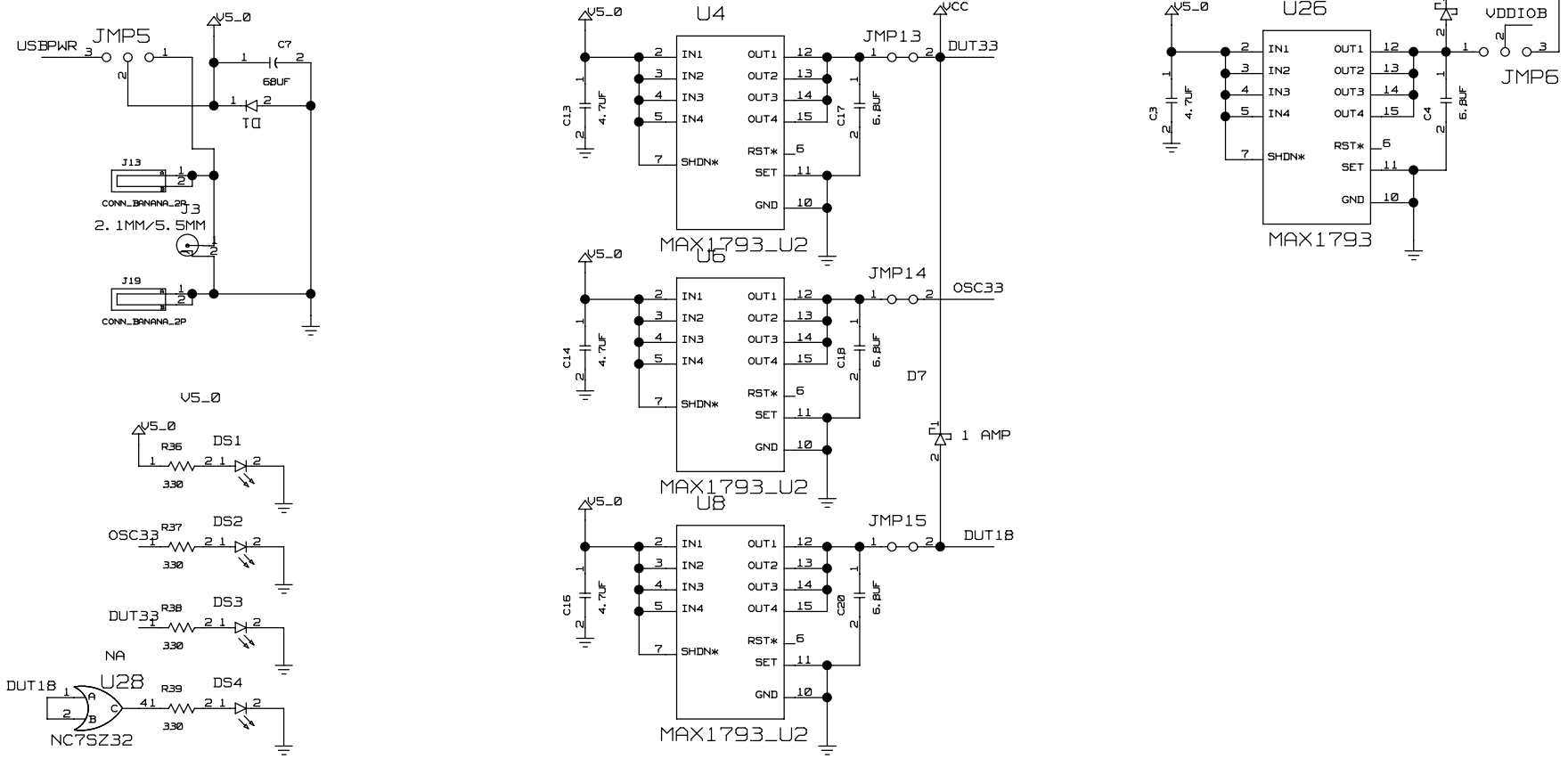
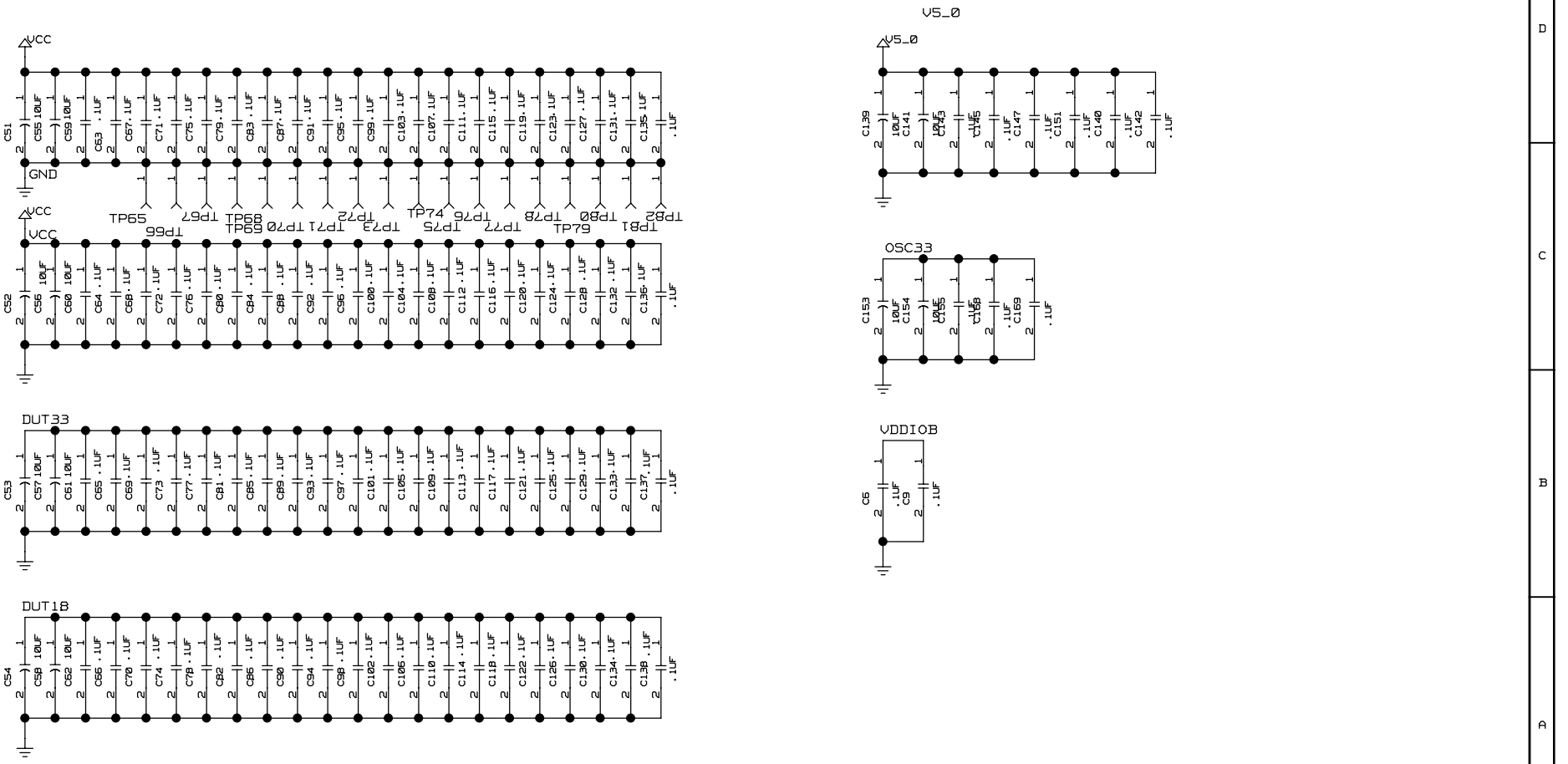


Wed May 30 13:54:20 2007

TITLE: DS3104DK01B0	DATE: 013007
ENGINEER: JML	PAGE: 10 OF 12



Wed May 30 13:54:21 2007

TITLE: DS3104DK01B0	DATE: 013007
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REVISION HISTORY -

01	- 021907	-	RELEASE FOR REVIEW
02	- 030907	-	ADDED TWO FOOTPRINTS FOR SMD STRATUM 4 OSC,
		-	ADDED SPI TESTPOINTS, CHANGED 4.7UF TO 100 UF
		-	ON DS OSC, OTHER CHANGES MADE PER DESIGN REVIEW
A0	- 051707	-	GENERAL CLEANUP, RELEASE TO DATASHEET,
B0	- 052907	-	FIXED USBPWR NET, FIXED SILKSCREEN BELOW SONSDH HEADER

Tue May 29 13:45:02 2007

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