



## TE0715 TRM

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## Overview

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Refer to <https://wiki.trenz-electronic.de/display/PD/TE0715+TRM> for online version of this manual and the rest of available documentation.

The Trenz Electronic TE0715 is an industrial-grade SoM (System on Module) based on [Xilinx Zynq-7000 SoC](#) (XC7Z015 or XC7Z030) with 1GByte of DDR3 SDRAM, 32MBytes of SPI Flash memory, Gigabit Ethernet PHY transceiver, a USB PHY transceiver and powerful switching-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via rugged high-speed stacking strips.

## Key Features

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- Industrial-grade Xilinx Zynq-7000 SoC (XC7Z015, XC7Z030)
- Rugged for shock and high vibration
- 2 x ARM Cortex-A9
- 10/100/1000 Mbps Ethernet transceiver PHY
- MAC address EEPROM
- 32-bit wide 1GB DDR3 SDRAM
- 32 MByte quad SPI Flash memory
- Programmable clock generator
  - Transceiver clock (default 125 MHz)
- Plug-on module with 2 x 100-pin and 1 x 60-pin high-speed hermaphroditic strips
- 132 FPGA I/Os (65 LVDS pairs possible) and 14 PS MIO available on B2B connectors
- 4 GTP/GTX (high-performance transceiver) lanes
  - GTP/GTX (high-performance transceiver) clock input
- USB 2.0 high-speed ULPI transceiver
- On-board high-efficiency DC-DC converters
  - 4.0 A x 1.0 V power rail
  - 1.5 A x 1.5 V power rail
  - 1.5 A x 1.8 V power rail
- System management
- eFUSE bit-stream encryption
- AES bit-stream encryption
- Temperature compensated RTC (real-time clock)
- User LED
- Evenly-spread supply pins for good signal integrity

Additional assembly options are available for cost or performance optimization upon request.

## Block Diagram

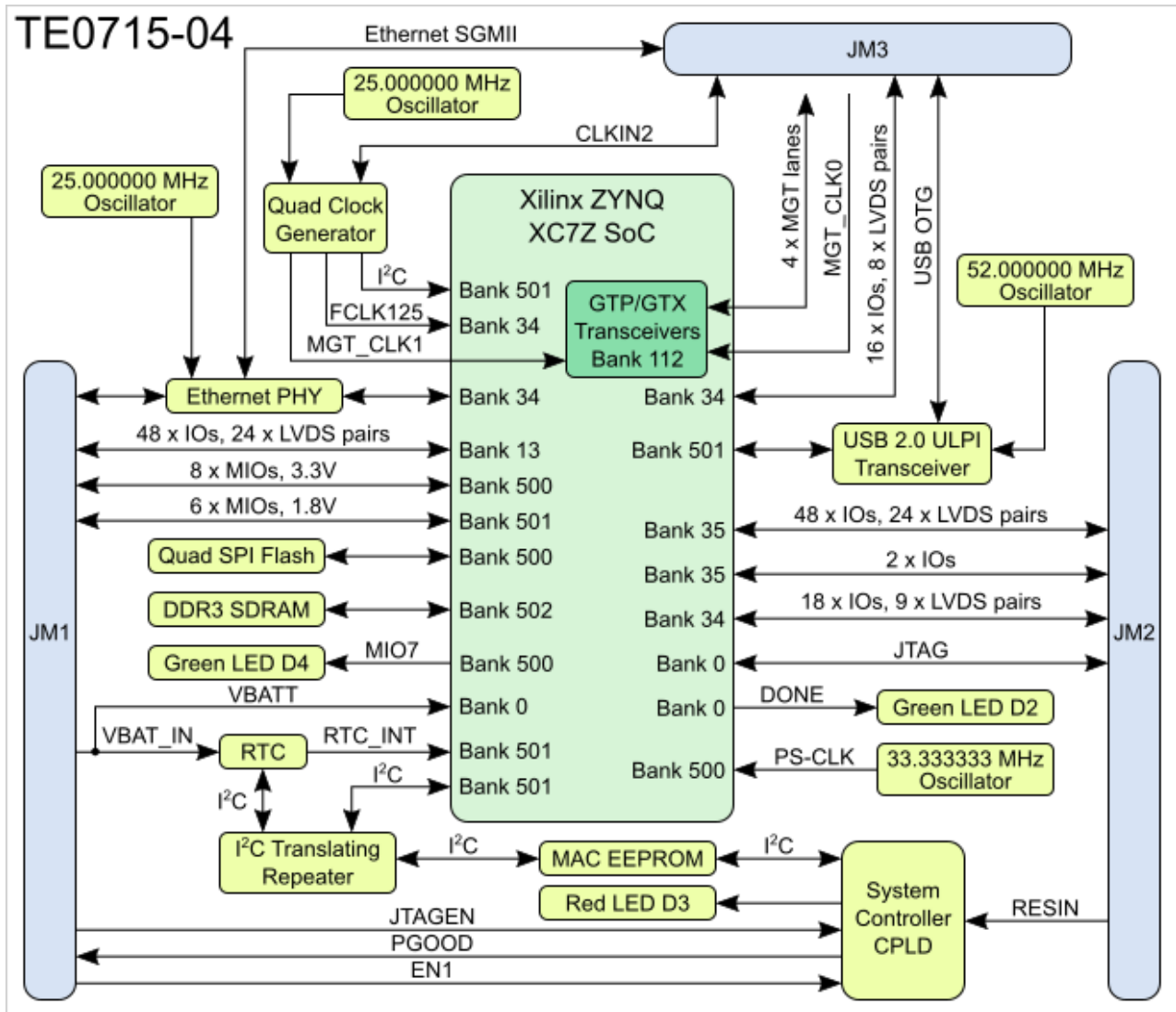
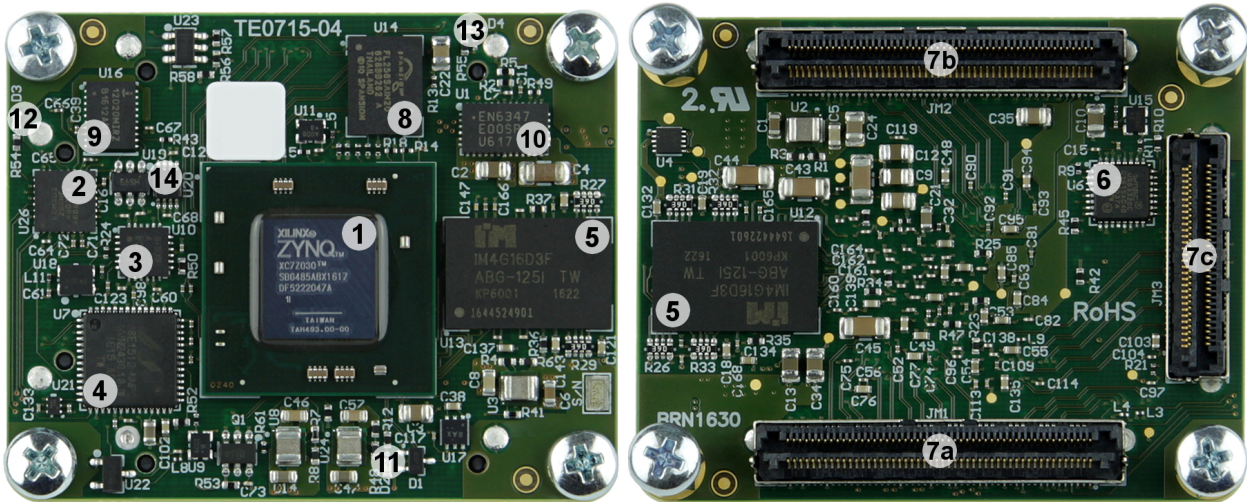


Figure 1: TE0715 block diagram.

## Main Components



**Figure 2:** TE0715 main components.

- 1. Xilinx Zynq-7000 all programmable SoC, U5
- 2. System Controller CPLD, U26
- 3. Programmable quad clock generator , U10
- 4. 10/100/1000 Mbps Ethernet PHY, U7
- 5. 4 Gbit DDR3L SDRAM (1.35 V), U12 and U13
- 6. Hi-speed USB 2.0 ULPI transceiver, U6
- 7a. B2B connector Samtec Razor Beam™ LSHM-150, JM1
- 7b. B2B connector Samtec Razor Beam™ LSHM-150 , JM2
- 7c . B2B connector Samtec Razor Beam™ LSHM-130, JM3
- 8. 32-MByte quad SPI Flash memory, U14
- 9. Low-power RTC with battery backed SRAM, U16
- 10. 4A PowerSoC DC-DC converter, U1
- 11. Green LED (DONE), D2
- 12. Red LED (SC), D3
- 13. Green LED (MIO7), D4
- 14. 2-bit bidirectional 1-MHz I<sup>2</sup>C bus voltage-level translator, U20

## Initial Delivery State

Storage device name	Content	Notes
24AA025E48 EEPROM	User content not programmed	Valid MAC address from manufacturer.
SPI Flash OTP Area	Empty, not programmed	Except serial number programmed by flash vendor.
SPI Flash Quad Enable bit	Programmed	-
SPI Flash main array	Demo design	-
eFUSE USER	Not programmed	-
eFUSE Security	Not programmed	-
Si5338 OTP NVM	Default settings pre-programmed	OTP not re-programmable after delivery from factory

**Table 1:** Initial delivery state of programmable devices on the module.

## Boot Process

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By default the TE-0715 supports quad SPI and SD Card boot modes which is controlled by the MODE input signal from the B2B JM1 connector.

MODE Signal State	Boot Mode
High or open	QSPI
Low or ground	SD Card

**Table 2:** Boot MODE signal description.



# Signals, Interfaces and Pins

## Board to Board (B2B) I/Os

I/O signals connected to the SoC's I/O bank and B2B connector:

Bank	Type	B2B Connector	I/O Signal Count	Voltage	Notes
13	HR	JM1	48	User	Supported voltages from 1.2V to 3.3V.
34	HR /HP	JM2	18	User	TE0715-xx-15 has no HP banks, banks 34 and 35 are HR banks on this module!  Banks 34 and 35 on TE0715-xx-30 are HP banks and support voltages from 1.2V to 1.8V.
35	HR /HP	JM2	50	User	As above.
34	HR /HP	JM3	16	User	As above.
500	MIO	JM1	8	3.3V	-
501	MIO	JM1	6	1.8V	-
112	GT	JM3	4 lanes	N/A	-
112	GT CLK	JM3	1 differential input	N/A	NB! AC coupling capacitors on baseboard required.

**Table 3:** General overview of board to board I/O signals.

For detailed information about the pin-out, please refer to the [Pin-out Table](#).

## MGT Lanes

MGT (Multi Gigabit Transceiver) lane consists of one transmit and one receive (TX/RX) differential pairs, two signals each or four signals total per one MGT lane. Following table lists lane number, MGT bank number, transceiver type, signal schematic name, board-to-board pin connection and FPGA pins connection:

Lane	Bank	Type	Signal Name	B2B Pin	FPGA Pin
0	112	GTX	<ul style="list-style-type: none"> <li>• MGT_RX0_P</li> <li>• MGT_RX0_N</li> <li>• MGT_TX0_P</li> <li>• MGT_TX0_N</li> </ul>	<ul style="list-style-type: none"> <li>• JM3-10</li> <li>• JM3-8</li> <li>• JM3-9</li> <li>• JM3-7</li> </ul>	<ul style="list-style-type: none"> <li>• MGTXRXPO_112, AA7</li> <li>• MGTXRXNO_112, AB7</li> <li>• MGTXTXP0_112, AA3</li> <li>• MGTXTXNO_112, AB3</li> </ul>

Lane	Bank	Type	Signal Name	B2B Pin	FPGA Pin
1	112	GTX	<ul style="list-style-type: none"> <li>• MGT_RX1_P</li> <li>• MGT_RX1_N</li> <li>• MGT_TX1_P</li> <li>• MGT_TX1_N</li> </ul>	<ul style="list-style-type: none"> <li>• JM3-16</li> <li>• JM3-14</li> <li>• JM3-15</li> <li>• JM3-13</li> </ul>	<ul style="list-style-type: none"> <li>• MGTXRX1_112, W8</li> <li>• MGTXRXN1_112, Y8</li> <li>• MGTTXP1_112, W4</li> <li>• MGTTXN1_112, Y4</li> </ul>
2	112	GTX	<ul style="list-style-type: none"> <li>• MGT_RX2_P</li> <li>• MGT_RX2_N</li> <li>• MGT_TX2_P</li> <li>• MGT_TX2_N</li> </ul>	<ul style="list-style-type: none"> <li>• JM3-22</li> <li>• JM3-20</li> <li>• JM3-21</li> <li>• JM3-19</li> </ul>	<ul style="list-style-type: none"> <li>• MGTXRX2_112, AA9</li> <li>• MGTXRXN2_112, AB9</li> <li>• MGTTXP2_112, AA5</li> <li>• MGTTXN2_112, AB5</li> </ul>
3	112	GTX	<ul style="list-style-type: none"> <li>• MGT_RX3_P</li> <li>• MGT_RX3_N</li> <li>• MGT_TX3_P</li> <li>• MGT_TX3_N</li> </ul>	<ul style="list-style-type: none"> <li>• JM3-28</li> <li>• JM3-26</li> <li>• JM3-27</li> <li>• JM3-25</li> </ul>	<ul style="list-style-type: none"> <li>• MGTXRX3_112, W6</li> <li>• MGTXRXN3_112, Y6</li> <li>• MGTTXP3_112, W2</li> <li>• MGTTXN3_112, Y2</li> </ul>

**Table 4:** MGT lanes.

Below are listed MGT banks reference clock sources.

Clock signal	Bank	Source	FPGA Pin	Notes
MGT_CLK0_P	112	B2B, JM3-33	MGTREFCLK0P_112, U9	Supplied by the carrier board.
MGT_CLK0_N	112	B2B, JM3-31	MGTREFCLK0N_112, V9	Supplied by the carrier board.
MGT_CLK1_P	112	U10, CLK2A	MGTREFCLK1P_112, U5	On-board Si5338A.
MGT_CLK1_N	112	U10, CLK2B	MGTREFCLK1N_112, V5	On-board Si5338A.

**Table 5:** MGT reference clock sources.

## JTAG Interface

JTAG access to the Xilinx Zynq-7000 is provided through B2B connector JM2.

JTAG Signal	B2B Connector Pin
TMS	JM2-93
TDI	JM2-95
TDO	JM2-97
TCK	JM2-99

**Table 6:** MGT lanes.


JTAGEN pin in B2B connector JM1 should be kept low or grounded for normal operation.

## System Controller CPLD I/O Pins

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Special purpose pins are connected to System Controller CPLD and have following default configuration:

Pin Name	Mode	Function	Default Configuration
EN1	Input	Power Enable	No hard wired function on PCB, when forced low pulls POR_B low to emulate power on reset.
PGOOD	Output	Power Good	Active high when all on-module power supplies are working properly.
NOSEQ	-	-	No function.
RESIN	Input	Reset	Active low reset, gated to POR_B.
JTAGEN	Input	JTAG Select	Low for normal operation.

**Table 7:** System Controller CPLD I/O pins.

## Quad SPI Interface

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Quad SPI Flash (U14) is connected to the Zynq PS QSPI0 interface via PS MIO bank 500, pins MIO1 ... MIO6.

Zynq SoC's MIO	Signal Name	U5 Pin
1	SPI-CS	C2
2	SPI-DQ0/M3	D3
3	SPI-DQ1/M1	D2
4	SPI-DQ2/M2	C4
5	SPI-DQ3/M0	D4
6	SPI-SCK	B2

**Table 8:** Quad SPI interface signals and connections.

## SD Card Interface

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SD Card interface is connected from the Zynq SoC's PS MIO bank 501 to the B2B connector JM1, signals MIO40 .. MIO45.

## Ethernet Interface

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On-board Gigabit Ethernet PHY is provided with Marvell Alaska 88E1512 IC (U7). The Ethernet PHY RGMII interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signalling. SGMII (SFP copper or fiber) can be used directly with the Ethernet PHY, as the SGMII pins are available on the B2B connector JM3. The reference clock input of the PHY is supplied from an on-board 25.000000 MHz oscillator (U9), the 125MHz output clock signal CLK\_125MHZ is connected to the IN5 pin of the PLL chip (U10).

### Ethernet PHY connection

PHY Pin	Zynq PS	Zynq PL	Notes
MDC/MDIO	MIO52, MIO53	-	-
LED0	-	J3	Can be routed via PL to any free PL I/O pin in B2B connector.
LED1	-	K8	Can be routed via PL to any free PL I/O pin in B2B connector.  This LED is connected to PL via level-shifter implemented in system controller CPLD.
LED2/Interrupt	MIO46	-	-
CONFIG	-	-	By default the PHY address is strapped to 0x00, alternate configuration is possible.
RESETn	MIO50	-	-
RGMII	MIO16..MIO27	-	-
SGMII	-	-	Routed to B2B connector JM3.
MDI	-	-	Routed to B2B connector JM1.

**Table 9:** Ethernet interface.

## USB Interface

USB PHY is provided by USB3320 from Microchip. The ULPI interface is connected to the Zynq PS USB0. The I/O Voltage is fixed at 1.8V. The reference clock input of the PHY is supplied from an on-board 52.000000 MHz oscillator (U15).

### USB PHY connection

PHY Pin	ZYNQ Pin	B2B Name	Notes
ULPI	MIO28..39	-	Zynq USB0 MIO pins are connected to the PHY.
REFCLK	-	-	52.000000 MHz from on board oscillator (U15).
REFSEL[0..2]	-	-	Reference clock frequency select, all set to GND selects 52.000000 MHz.
RESETB	MIO51	-	Active low reset.
CLKOUT	MIO36	-	Connected to 1.8V, selects reference clock operation mode.
DP, DM	-	OTG_D_P, OTG_D_N	USB data lines.
CPEN	-	VBUS_V_EN	External USB power switch active high enable signal.
VBUS	-	USB_VBUS	Connect to USB VBUS via a series of resistors, see reference schematics.
ID	-	OTG_ID	For an A-device connect to the ground, for a B-device leave floating.

**Table 10:** USB interface.

The schematics for the USB connector and required components is different depending on the USB usage. USB standard A or B connectors can be used for host or device modes. A mini-USB connector can be used for USB device mode. A micro-USB connector can be used for device mode, OTG mode or host mode.

## I<sup>2</sup>C Interface

On-board I<sup>2</sup>C devices are connected to MIO48 and MIO49 which are configured as I2C1 by default. I<sup>2</sup>C addresses for on-board devices are listed in the table below:

I <sup>2</sup> C Device	I <sup>2</sup> C Address	Notes
EEPROM	0x50	
RTC	0x6F	
Battery backed RAM	0x57	Integrated into RTC.
PLL	0x70	

**Table 11:** I<sup>2</sup>C interface.

## On-board Peripherals

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### System Controller CPLD

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The System Controller CPLD (U26) is provided by Lattice Semiconductor LCMXO2-256HC (MachXO2 product family). It is the central system management unit with module specific firmware installed to monitor and control various signals of the FPGA, on-board peripherals, I/O interfaces and module as a whole.

### DDR Memory

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TE0715 module has up to 1 GBytes of DDR3L SDRAM arranged into 32-bit wide memory bus. Different memory sizes are available optionally.

### Quad SPI Flash Memory

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On-board quad SPI Flash memory S25FL256S (U14) is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.



SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash during power-on. By default this bit is set to high at the manufacturing plant.

### Gigabit Ethernet PHY

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On-board Gigabit Ethernet PHY (U7) is provided with Marvell Alaska 88E1512. The Ethernet PHY RGMII interface is connected to the Zynq SoC's PS bank 501 pins MIO16 .. MIO27. Reference clock input of the PHY is supplied from the on-board 25.000000 MHz oscillator (U9), the 125MHz output clock signal CLK\_125MHZ is connected to the programmable clock generator (U10) pin IN5.

### High-speed USB ULPI PHY

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Hi-speed USB ULPI PHY (U6) is provided with USB3320 from Microchip. The ULPI interface is connected to the Zynq SoC's PS bank 501 pins MIO28 .. 39. Reference clock input is supplied from the on-board 52.000000 MHz oscillator (U15).

### MAC Address EEPROM

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A Microchip 24AA025E48 EEPROM (U19) is used which contains a globally unique 48-bit node address, that is compatible with EUI-48TM specification. The device is organized as two blocks of 128 x 8-bit memory. One of the blocks stores the 48-bit node address and is write protected, the other block is available for application use. It is accessible through the I<sup>2</sup>C slave address 0x50.

## RTC - Real Time Clock

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An temperature compensated Intersil ISL12020M is used for Real Time Clock (U16). Battery voltage must be supplied to the module from the baseboard. Battery backed registers can be accessed over I<sup>2</sup>C bus at slave address of 0x6F. General purpose RAM is at I<sup>2</sup>C slave address 0x57. RTC IC is supported by Linux so it can be used as *hwclock* device.

## Programmable Clock Generator

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There is a Silicon Labs programmable clock generator Si5338A (U10) chip on the module. It's output frequencies can be programmed via the I<sup>2</sup>C bus, slave device address is 0x70.

U10 Signal	Default Frequency	Notes
IN1/IN2	Externally supplied	Needs decoupling on carrier board.
IN3	25.000000 MHz	Reference input clock.
IN4	-	Wired to the GND.
IN5/IN6	125 MHz	Ethernet PHY output clock.
CLK0 A/B	-	Not used, disabled.
CLK1 A/B	-	Not used, disabled.
CLK2 A/B	125 MHz	MGT reference clock 1.
CLK3A	-	Bank 34 clock input, default disabled, user clock.
CLK3B	-	Not used, disabled.

**Table 12:** Programmable clock generator I/Os.

## Oscillators

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The module has following reference clock signals provided by on-board oscillators:

Source	Signal	Frequency	Destination	Pin Name	Notes
U18	CLK	25.000000 MHz	U10	IN3	
U9	CLK	25.000000 MHz	U7	XTAL_IN	
U11	PS-CLK	33.333333 MHz	U5	PS_CLK_500	Zynq SoC PS subsystem main clock.
U15	CLK	52.000000 MHz	U6	REFCLK	USB3320C PHY reference clock.

**Table 13:** Reference clock signals.

## On-board LEDs

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LED	Color	Connected to	Description and Notes
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LED	Color	Connected to	Description and Notes
D2	Green	DONE	Reflects inverted DONE signal. ON when FPGA is not configured, OFF as soon as PL is configured.  This LED will not operate if the SC can not power on the 3.3V output rail that also powers the 3.3V circuitry on the module.
D3	Red	SC	System main status LED.
D4	Green	MIO7	User controlled, default OFF (when PS7 has not been booted).

**Table 14:** On-board LEDs.



## Power and Power-On Sequence

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 TE0715-xx-30 has several HP banks on B2B connectors. Those banks have maximum voltage tolerance of 1.8V. Please check special instructions for the baseboard to be used with TE0715-xx-30.

### Power Supply

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Power supply with minimum current capability of 3A for system startup is recommended.

#### Power Consumption

Power Input Pin	Typical Current
VIN	TBD*
3.3VIN	TBD*

**Table 15:** Power consumption.

\* TBD - To Be Determined.

Lowest power consumption is achieved when powering the module from single 3.3V supply. When using split 3.3V/5V supplies the power consumption (and heat dissipation) will rise due to the DC-DC converter efficiency (it decreases when VIN/VOUT ratio rises). Typical module power consumption is between 2-3W.

### Power-On Sequence

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For highest efficiency of on board DC/DC regulators, it is recommended to use same 3.3V power source for both VIN and 3.3VIN power rails. Although VIN and 3.3VIN can be powered up in any order, it is recommended to power them up simultaneously.

It is important that all baseboard I/Os are 3-stated at power-on until System Controller sets PGOOD signal high (B2B connector JM1, pin 30), or 3.3V is present on B2B connector JM2 pins 10 and 12, meaning that all on-module voltages have become stable and module is properly powered up.

See Xilinx datasheet [DS187](#) (for XC7Z015) or [DS191](#) (for XC7Z030) for additional information. User should also check related baseboard documentation when choosing baseboard design for TE0715 module.

## Power Rails

B2B Name	B2B JM1 Pins	B2B JM2 Pins	Direction	Note
VIN	1, 3, 5	2, 4, 6, 8	Input	Supply voltage.
3.3VIN	13, 15	-	Input	Supply voltage.
VCCIO13	9, 11	-	Input	High range bank voltage.
VCCIO34	-	5	Input	TE0715-xx-15: high range bank voltage. TE0715-xx-30: high performance bank voltage.
VCCIO35	-	7, 9	Input	TE0715-xx-15: high range bank voltage. TE0715-xx-30: high performance bank voltage.
VBAT_IN	79	-	Input	RTC battery-buffer supply voltage.
3.3V	-	10, 12	Output	Internal 3.3V voltage level.
1.8V	39	-	Output	Internal 1.8V voltage level.
DDR_PWR	-	19	Output	Internal 1.5V or 1.35V voltage level, depends on revision.
VREF_JTAG		91	Output	JTAG reference voltage (3.3V).


**Table 16:** TE0715 power rails.

## Bank Voltages

Bank	Schematic Name	Voltage	TE0715-xx-15	TE0715-xx-30
500	VCCO_MIO0_500	3.3V	-	-
501	VCCO_MIO1_501	1.8V	-	-
502	VCCO_DDR_502	1.5V	-	-
0 Config	VCCO_0	3.3V	-	-
13 HR	VCCO_13	User	HR: 1.2V to 3.3V	HR: 1.2V to 3.3V
34 HR/HP	VCCO_34	User	HR: 1.2V to 3.3V	HP: 1.2V to 1.8V
35 HR/HP	VCCO_35	User	HR: 1.2V to 3.3V	HP: 1.2V to 1.8V

**Table 17:** TE0715 bank voltages.

## Board to Board Connectors

-  These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

Trenz Electronic 4 x 5 modules use two or three Samtec Razor Beam™ LSHM connectors on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height:

Connector on baseboard	compatible to	Mating height
REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

The module can be manufactured using other connectors upon request.

The LSHM connector speed rating depends on the stacking height, please see the following table:

Stacking height	Speed rating
12 mm, Single-ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.9 GHz / 14 Gbps

## Connector Mechanical Ratings

- Shock: 100G, 6 ms sine
- Vibration: 7.5G random, 3 hours 3 axis



## Variants Currently in Production

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Module Variant	Zynq SoC	Temperature Range	B2B Connector Height
TE0715-04-15-1I	XC7Z015-1CLG485I	Industrial	4.0 mm
TE0715-04-15-2I	XC7Z015-2CLG485I	Industrial	4.0 mm
TE0715-04-30-1I	XC7Z030-1SBG485I	Industrial	4.0 mm
TE0715-04-30-3E	XC7Z030-3SBG485E	Extended	4.0 mm
TE0715-04-15-1I3	XC7Z015-1CLG485I	Industrial	2.5 mm
TE0715-04-30-1I3	XC7Z030-1SBG485I	Industrial	2.5 mm
TE0715-04-30-1C	XC7Z030-1SBG485C	Commercial	4.0 mm


**Table 18:** TE0715 variants currently in production.


# Technical Specifications

## Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
VIN supply voltage	-0.3	6.0	V	-
3.3VIN supply voltage	-0.4	3.6	V	-
VBAT supply voltage	-1	6.0	V	-
PL IO bank supply voltage for HR I/O banks (VCCO)	-0.5	3.6	V	-
PL IO bank supply voltage for HP I/O banks (VCCO)	-0.5	2.0	V	TE0715-xx-15 does not have HP banks.
I/O input voltage for HR I/O banks	-0.4	VCCO + 0.55	V	-
I/O input voltage for HP I/O banks	-0.55	VCCO + 0.55	V	TE0715-xx-15 does not have HP banks.
GT receiver (RXP/RXN) and transmitter (TXP/TXN)	-0.5	1.26	V	-
Voltage on module JTAG pins	-0.4	VCCO_0 + 0.55	V	VCCO_0 is 3.3V nominal.
Storage temperature	-40	+85	°C	-
Storage temperature without the ISL12020MIRZ and 88E1512	-55	+100	°C	-

**Table 19:** TE0715 module absolute maximum ratings.

 Assembly variants for higher storage temperature range are available on request.

 Please check Xilinx datasheet [DS187](#) (for XC7Z015) or [DS191](#) (for XC7Z030) for complete list of absolute maximum and recommended operating ratings.

## Recommended Operating Conditions

Parameter	Min	Max	Units	Notes	Reference Document
VIN supply voltage	2.5	5.5	V		
3.3VIN supply voltage	3.135	3.465	V		
VBAT_IN supply voltage	2.7	5.5	V		
PL I/O bank supply voltage for HR I/O banks (VCCO)	1.14	3.465	V		Xilinx datasheet <a href="#">DS191</a>
PL I/O bank supply voltage for HP I/O banks (VCCO)	1.14	1.89	V	TE0715-xx-15 does not have HP banks	Xilinx datasheet <a href="#">DS191</a>
I/O input voltage for HR I/O banks	(*)	(*)	V	(*) Check datasheet	Xilinx datasheet <a href="#">DS191</a> or <a href="#">DS187</a>
I/O input voltage for HP I/O banks	(*)	(*)	V	TE0715-xx-15 does not have HP banks (*) Check datasheet	Xilinx datasheet <a href="#">DS191</a>
Voltage on Module JTAG pins	3.135	3.465	V	VCCO_0 is 3.3 V nominal	

**Table 20:** TE0715 module recommended operating conditions.

## Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

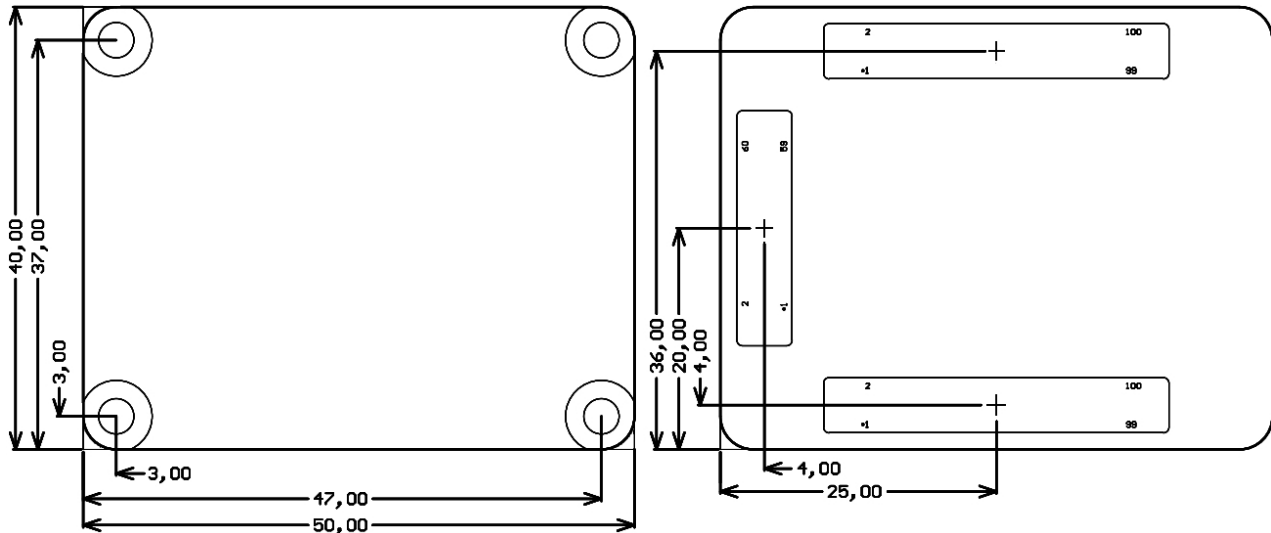
Industrial and extended grade: -40°C to +85°C.

The module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

## Physical Dimensions

- Module size: 50 mm x 40 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 8mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 2.5mm. Please download the step model for exact numbers

All dimensions are given in millimeters.



**Figure 3:** TE0715 physical dimensions.



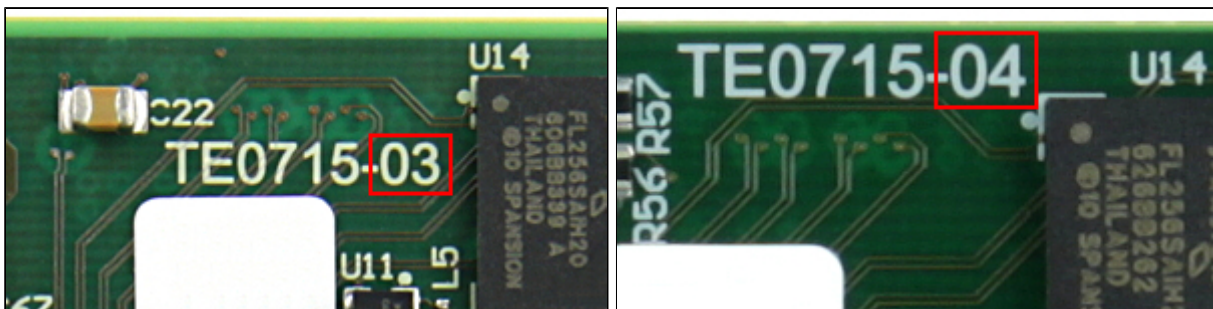
# Revision History

## Hardware Revision History

Date	Revision	Notes	Link to PCN	Documentation Link
2016-06-21	04	Second production release	<a href="#">Click to see PCN</a>	<a href="#">TE0715-04</a>
-	03	First production release		<a href="#">TE0715-03</a>
-	02	Prototypes		<a href="#">TE0715-02</a>
-	01	Prototypes		

**Table 21:** TE0715 module hardware revision history.

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.



**Figure 4:** TE0715 hardware revision number.

## Document Change History

Date	Revision	Contributors	Description
2017-09-06	V.69	Jan Kumann	<ul style="list-style-type: none"> <li>• Document template revision added.</li> <li>• Sections rearranged and missing ones added.</li> <li>• Weight section removed.</li> </ul>
2017-06-07	v.64	Jan Kumann	Minor formatting.
2017-03-02	v.59	Thorsten Trenz	Corrected boot mode table.
2017-02-10	v.58	Thorsten Trenz	Corrected PLL initial delivery state.
2017-01-25	v.55	Jan Kumann	New block diagram.
2017-01-14	v.50	Jan Kumann	<ul style="list-style-type: none"> <li>• Product revision 04 images added.</li> <li>• Formatting changes and small corrections.</li> </ul>
2016-11-15	v.45	Thorsten Trenz	Added B2B Connector section.
2016-10-18	v.40	Ali Naseri	Added table "power rails".

Date	Revision	Contributors	Description
2016-06-28	v.38	Thorsten Trenz, Emmanuel Vassilakis, Jan Kumann	<ul style="list-style-type: none"> <li>• New overall document layout with shorter table of contents.</li> <li>• Revision 01 PCB pictures replaced with the revision 03 ones.</li> <li>• Fixed link to Master Pin-out Table.</li> <li>• New default MIO mapping table design.</li> <li>• Revised Power-on section.</li> <li>• Added links to related Xilinx online documents.</li> <li>• Physical dimensions pictures revised.</li> <li>• Revision number picture with explanation added.</li> </ul>
2016-04-27	v.33	Thorsten Trenz, Emmanuel Vassilakis	<ul style="list-style-type: none"> <li>• Added table "Recommended Operating Conditions".</li> <li>• Storage Temperature edited.</li> </ul>
2016-03-31	v.10	Philipp Bernhardt, Antti Lukats	Initial version.

**Table 22:** Document change history.

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