2-Channel Synchronous Step-down DC/DC Converter IC
MB39A138

By adopting the bottom detection comparator method, this product is capable of stable operation and rapid response even with large difference between input and output voltages and rapid load changes. It does not require phase compensation to prevent oscillation. System construction with a small number of parts is enabled through the use of a built-in bootstrap diode, which is required for FET operation. This product has an output capacity of low voltage of approximately 1.0V with current at 10A or larger. It is capable of providing simultaneous power management to two destinations such as a LSI of core and I/O or a memory. Its soft-start discharge function also enables simple power management sequence control when multiple voltages are used.

Overview

FUJITSU has devoted a great deal of effort toward developing DC/DC power management ICs for high-performance digital home appliances and numerous products have been launched as a result. This time, we have developed "MB39A138," a 2-channel synchronous rectification step-down DC/DC converter IC.

This product is a power management IC that supports low on-duty operation when there is a large difference between input and output voltages by adopting the bottom detection comparator method to fix the ON period and control the OFF period. It uses the output ripple that is generated by the internal resistor ESR of the output capacitor for OFF period control. When the output voltage decreases and falls below the target output voltage value, the comparator responds and generates an ON pulse as output. With a built-in rapid comparator in the output voltage detection block, it responds swiftly and suppresses the output voltage fluctuation to a

Photo 1 External View

minimum when the load suddenly becomes large. The ON period is determined by the input and output voltages and is controlled so that the operation frequency is nearly stable and the output operates stably. This comparator method requires no phase compensation to prevent oscillation.

This product incorporates a built-in bootstrap diode that enables system construction with a small number of parts. Its output capacity has a low voltage of approximately 1.0V with a current of 10A or larger. It is capable of providing simultaneous power management to two destinations such as a LSI of core and I/O or a memory.

This product is also equipped with a soft-start discharge function. This makes it possible to control the power management input and shutdown sequence and adjust the power management ON/OFF timing when multiple voltages are used simultaneously.

These built-in functions make this product optimal as a power management IC for various leading-edge devices that utilize high-performance LSIs such as large digital TVs and copy machines.

Product Features

- Rapid response: Addresses rapid changes in load current
- High efficiency: Stable operation even under large difference between input and output voltages.
- Built-in 2-channel DC/DC converter realizing low-voltage and large-current output
- High-precision reference voltage: Offers high precision of ±1.0% (room temperature).
- Built-in bootstrap diode: Reduces the number of external parts.
- Substantial protective functions: Built-in overvoltage protection, undervoltage protection, overcurrent detection, and overtemperature protection functions.
- Built-in soft-start circuit independent from load conditions which allows simple sequence control
- Built-in output discharge circuit at output voltage OFF which allows simple sequence control
- Built-in synchronous rectification output stages addressing N-ch MOS FET which is optimal for large current output
- Built-in preset function: Output voltage Vo1=1.23V, Vo2=3.45V (connects to the FB terminal and the CVBLPF terminal)
- Small package: TSSOP-24 (**Photo 1**)
  4.40mm×7.80mm×1.2mm (0.65mm pitch)

Figures 1 and **2** present the rapid load change waveforms for this product. **Figures 3** and **4** the conversion efficiency against load current.

Functions

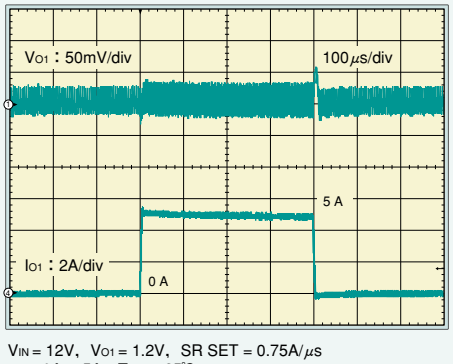
2-channel output

Addresses a high voltage input power supply of 6V to 24V. **Table 1** presents the channel output voltage/current.

Rapid load response

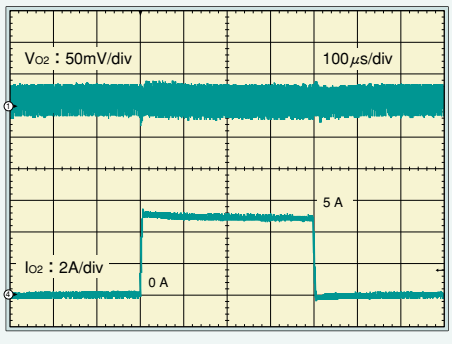
This product adopts a bottom detection comparator to detect the drop in output voltage and address rapid changes in load current. It follows large current differences by load current change 0A→5A→0A with small voltage changes of approximately 50mV to 80mV (**Figure 1**).

Figure 1 Load Step Waveform (Vo1)



V_{IN} = 12V, V_{O1} = 1.2V, SR SET = 0.75A/μs
I_{O1} = 0A⇔5A, Ta = +25℃

Figure 2 Load Step Waveform (Vo2)



V_{IN} = 12V, V_{O2} = 3.3V, SR SET = 0.75A/μs
I_{O2} = 0A⇔5A, Ta = +25℃

Figure 3 Conversion Efficiency/Load Current (Vo1)

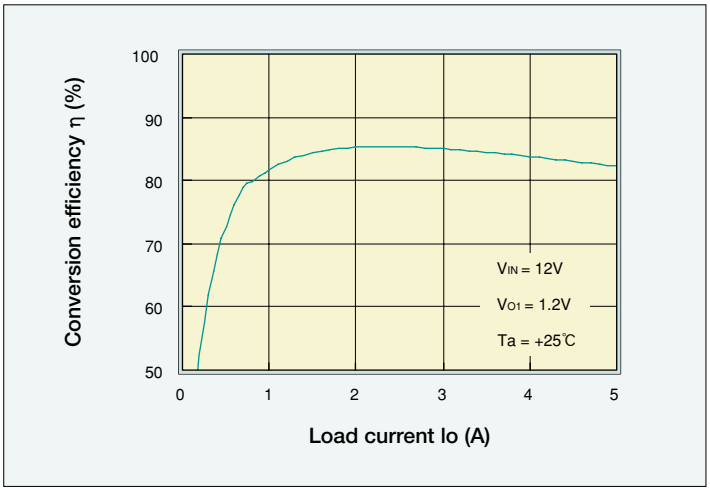


Figure 4 Conversion Efficiency/Load Current (Vo2)

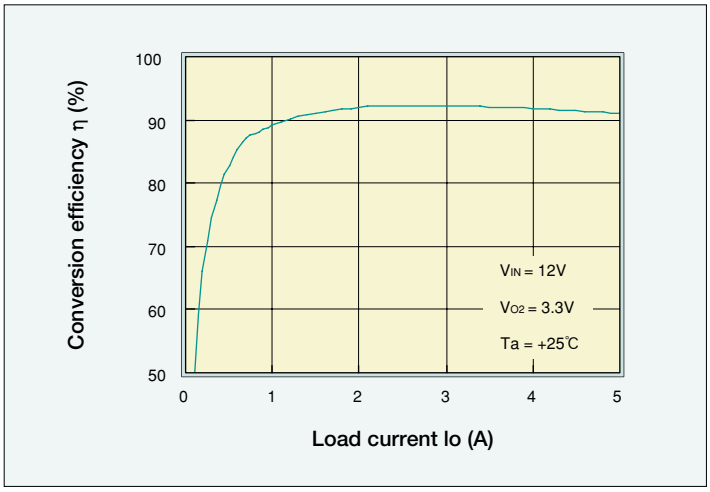


Table 1 Channel Output Voltage/Current

Channel	Output voltage	Output current
Vo1	0.7V to 5.2V	10A to (depends on FET)
Vo2	2.0V to 5.2V	10A to (depends on FET)

High efficiency

The bottom detection comparator method enables this product to operate stably even under high voltage input and low voltage output; it realizes high efficiency.

Circuit Configuration

Figure 5 presents the block diagram.

This product is composed of the following function blocks:

- Bias voltage block (VB Reg.)
- Undervoltage lockout circuit block (UVLO)
- Soft-start, Discharge block (Soft-Start, Discharge)
- ON/OFF period generation block (ton Generator)
- Output voltage setting block (VO Control, Error Comp.)
- Overvoltage protection circuit block (OVP Comp.)
- Undervoltage protection circuit block (UVP Comp.)
- Overtemperature protection block (OTP)
- Output block (DRV1, DRV2)
- Overcurrent detection block (ILIM)
- Control block (CTL)

Evaluation Board

We offer an evaluation board that can be used for evaluation of this product and reference for its built-in performance in product development (**Photo 2**).

The power supply terminal, input/output terminal, and GND terminal, which are necessary for evaluation, are set up as monitor terminals. ✱

Photo 2 Evaluation Board

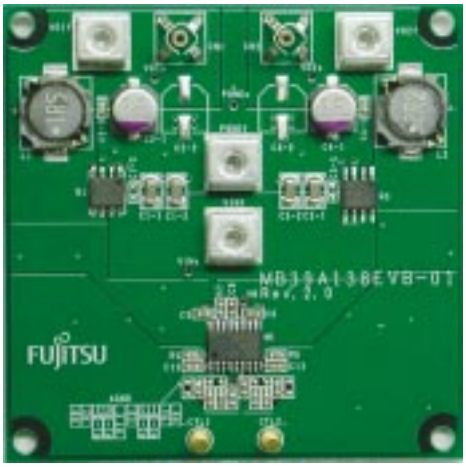


Figure 5 Block Diagram