Features

- **Contactless Read/Write Data Transmission**
- **Sensor Input R_S > 100kΩ (Typical) => Data Stream Inverted**
- **Radio Frequency f_{RF} from 100kHz to 150kHz**
- **e5550 Binary Compatible or ATA5570C Extended Mode**
- **Small Size, Configurable for ISO/IEC 11784/785 Compatibility**
- **7 x 32-bit EEPROM Data Memory Including 32-bit Password**
- **Separate 64-bit Memory for Traceability Data**
- **32-bit Configuration Register in EEPROM to Setup**
    - **Data Rate**
        - **RF/2 to RF/128, Binary Selectable or**
        - **Fixed Atmel e5550 Data Rates**
    - **Modulation/Coding**
        - **FSK, PSK, Manchester, Bi-phase, NRZ**
    - **Other Options**
        - **Password Mode**
        - **Maximum Block Feature**
        - **Answer-On-Request (AOR) Mode**
        - **Inverse Data Output**
        - **Direct Access Mode**
        - **Sequence Terminator(s)**
        - **Write Protection (Through Lock-bit per Block)**
        - **Fast Write Method (5Kbps versus 2Kbps)**
        - **OTP Functionality**
        - **POR Delay up to 67ms**

Multifunctional 330-bit Read/Write RF Sensor Identification IC

Atmel ATA5570C

1. Description

The Atmel® ATA5570C is a contactless R/W **ID**entification **IC** (IDIC®) for applications in the 125kHz frequency range. A single coil, connected to the chip, serves as the IC's power supply and bi-directional communication interface. The antenna and chip together form a transponder or tag.

The on-chip 330-bit EEPROM (10 blocks, 33 bits each) can be read and written block-wise from a reader. Block 0 is reserved for setting the operation modes of the ATA5570C tag. Block 7 may contain a password to prevent unauthorized writing.

Data is transmitted from the IDIC using load modulation. This is achieved by damping the RF field with a resistive load between the two terminals COIL1 and COIL2. The IC receives and decodes 100% amplitude-modulated (OOK) pulse-interval-encoded bit streams from the base station or reader.
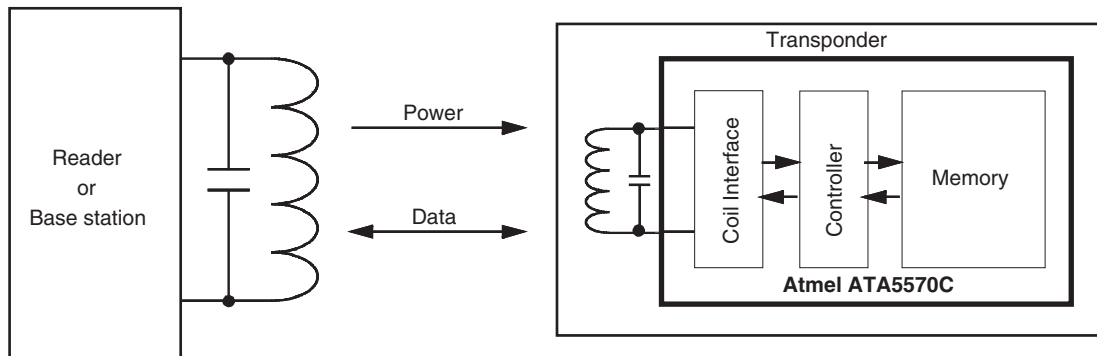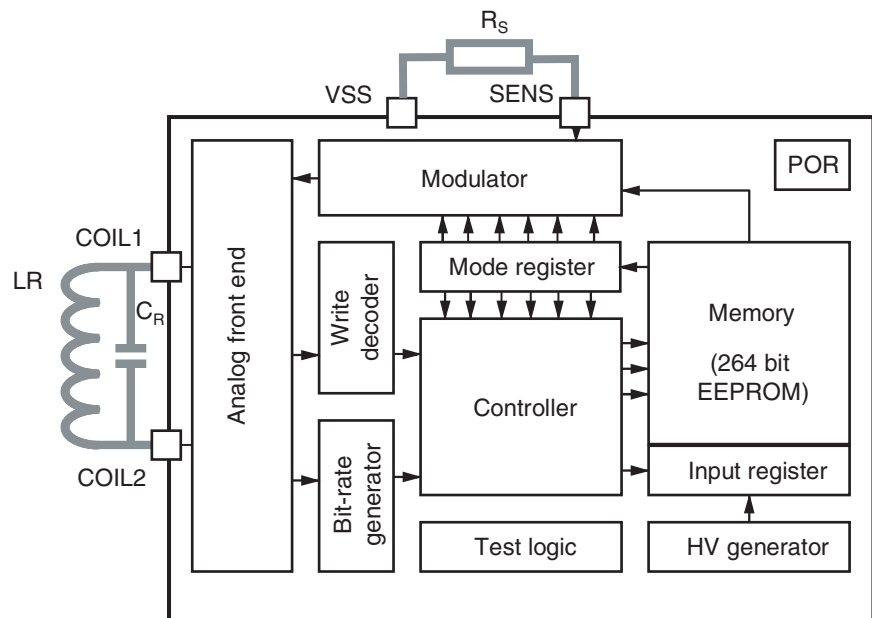
2. System Block Diagram

Figure 2-1. RFID System Using Atmel® ATA5570C Tag

3. ATA5570C – Building Blocks

Figure 3-1. Block Diagram

3.1 Analog Front End (AFE)

The AFE includes all circuits which are directly connected to the coil. It generates the IC's power supply and handles the bi-directional data communication with the reader. It consists of the following blocks:

- Rectifier to generate a DC supply voltage from the AC coil voltage
- Clock extractor
- Switchable load between COIL1 and COIL2 for data transmission from tag to the reader
- Field gap detector for data transmission from the base station to the tag
- ESD protection circuitry

3.2 Data-rate Generator

The data rate is binary programmable to operate at any data rate between RF/2 and RF/128 or equal to any of the fixed Atmel® e5550/e5551 and Atmel T5554 bit rates (RF/8, RF/16, RF/32, RF/40, RF/50, RF/64, RF/100 and RF/128).

3.3 Write Decoder

This function decodes the write gaps and verifies the validity of the data stream according to the Atmel e555x write method (pulse interval encoding).

3.4 HV Generator

This on-chip charge-pump circuit generates the high voltage required for programming of the EEPROM.

3.5 DC Supply

Power is externally supplied to the IDIC via the two coil connections. The IC rectifies and regulates this RF source and uses it to generate its supply voltage.

3.6 Power-On Reset (POR)

This circuit delays the IDIC functionality until an acceptable voltage threshold has been reached.

3.7 Clock Extraction

The clock extraction circuit uses the external RF signal as its internal clock source.

3.8 Controller

The control-logic module executes the following functions:

- Load-mode register with configuration data from EEPROM block 0 after power-on and also during reading
- Control memory access (read, write)
- Handle write data transmission and write error modes
- The first two bits of the reader-to-tag data stream are the opcode, e.g., write, direct access or reset
- In password mode, the 32 bits received after the opcode are compared with the password stored in memory block 7

3.9 Mode Register

The mode register stores the configuration data from the EEPROM block 0. It is continually refreshed at the start of every block read and (re-)loaded after any POR event or reset command. On delivery, the mode register is preprogrammed with the value 0014 8000h which corresponds to continuous read of block 0, Manchester coded, RF/64.

Figure 3-2. Block 0 Configuration Mapping – Atmel® e5550 Compatibility Mode

L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
	0	1	1	0	0	0	0	0	0	0	0				0									0					0	0		

Field groupings (left to right):
- **Lock Bit** (L)
- **Master Key** (bits 1–4), Note 1), 2)
- **Data Bit Rate** (bits 9–11)
- **Modulation** (bits 13–16 / 17–20)
- **PSK CF** (bits 21–22)
- **AOR**
- **Max Block** (bits 25–28)
- **PWD**
- **ST-sequence Terminator**
- **POR delay**

Lock Bit

0	Unlocked
1	Locked

Data Bit Rate

RF/8	0	0	0
RF/16	0	0	1
RF/32	0	1	0
RF/40	0	1	1
RF/50	1	0	0
RF/64	1	0	1
RF/100	1	1	0
RF/128	1	1	1

Modulation

0	0	0	0	0	Direct
0	0	0	0	1	PSK1
0	0	0	1	0	PSK2
0	0	0	1	1	PSK3
0	0	1	0	0	FSK1
0	0	1	0	1	FSK2
0	0	1	1	0	FSK1a
0	0	1	1	1	FSK2a
0	1	0	0	0	Manchester
1	0	0	0	0	Bi-phase ('50)
1	1	0	0	0	Reserved

PSK CF

0	0	RF/2
0	1	RF/4
1	0	RF/8
1	1	RFU

1) If Master Key = 6 then test mode write commands are ignored
2) If Master Key < > 6 or 9 then extended function mode is disabled

3.10 Modulator

The modulator consists of data encoders for the following basic types of modulation:

Table 3-1. Types of Atmel e5550-compatible Modulation Modes

Mode Direct Data Output	Encoding		
FSK1a[1]	FSK/8, FSK/5	"0" = RF/8;	"1" = RF/5
FSK2a[1]	FSK/8, FSK/10	"0" = RF/8;	"1" = RF/10
FSK1[1]	FSK/5, FSK/8	"0" = RF/5;	"1" = RF/8
FSK2[1]	FSK/10, FSK/8	"0" = RF/10;	"1" = RF/8
PSK1[2]	Phase change when input changes		
PSK2[2]	Phase change on bit clock if input high		
PSK3[2]	Phase change on rising edge of input		
Manchester	"0" = falling edge, "1" = rising edge		
Bi-phase	"1" creates an additional mid-bit change		
NRZ	"1" = damping on, "0" = damping off		

Notes: 1. A common multiple of bit rate and FSK frequencies is recommended.

2. In PSK mode the selected data rate has to be an integer multiple of the PSK sub-carrier frequency.

3.11 Sensor Input

Modulated output data stream depends on the state of the sensor input. The data stream is inverted when external resistance, connected between Sensor input and VSS, is more than $R_S > 100$ kΩ (typical). Otherwise, the output data stream is not inverted ("normal").

3.12 Memory

The memory is a 330-bit EEPROM, which is arranged in 10 blocks of 33 bits each. All 33 bits of a block, including the lock bit, are programmed simultaneously.

Block 0 of page 0 contains the mode/configuration data, which is not transmitted during regular-read operations. Block 7 of page 0 may be used as a write-protection password.

Bit 0 of every block is the lock bit for that block. Once locked, the block (including the lock bit itself) is not re-programmable through the RF field.

Blocks 1 and 2 of page 1 contain traceability data and are transmitted with the modulation parameters defined in the configuration register after the opcode "11" is issued by the reader (Figure 4-6 on page 11). These traceability data blocks are programmed and locked by Atmel.

Figure 3-3. Memory Map
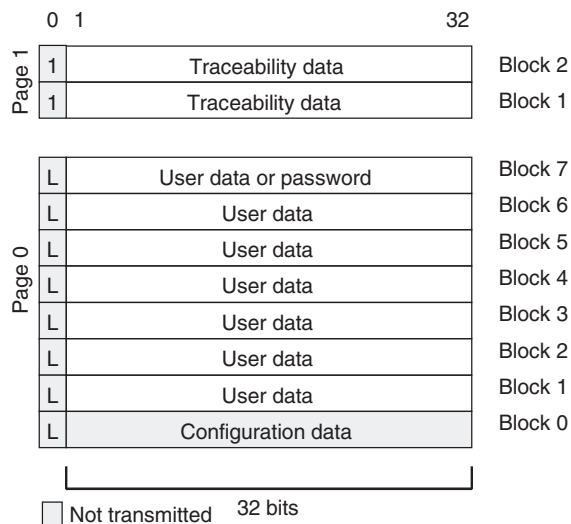
3.13 Traceability Data Structure/Unique ID

Blocks 1 and 2 of page 1 contain the traceability data and are programmed and locked by Atmel during production testing [1]. The most significant byte of block 1 is fixed to E0h, the allocation class (ACL) as defined in ISO/IEC 15963-1. The second byte is therefore defined in ISO/IEC 7816-6 as Atmel's manufacturer ID (15h). The following 5 bits indicate Chip ID (CID, "00011b" for Atmel® ATA5570C) the next bits (IC revision, ICR) are used by Atmel for the IC and/or foundry version of the Atmel ATA5570C.

The lower 40 bits of the data encode Atmel's traceability information and conform to a unique numbering system (unique ID). These 40 data bits contain LotID (Year, Quarter, Number), Wafernumber (Wafer#) and die number on wafer (DW).

Note: 1. This is only valid for sawn wafer on foil delivery.

Figure 3-4. Atmel ATA5570C Traceability Data Structure

Example:	"E0h" 8 bit	"15h" 8 bit	"00011b" 5 bit	"010b" 3 bit	"9h" 4 bit	"00b" 2 bit	"00b" 2 bit
Bit No.	1 … 8	9 … 16	17 … 21	22 … 24	25 … 28	29 30	31 32
Block 1	ACL	MFC	CID	ICR	Year	Quarter	Number
Bit value	63		MSB				32
Bit value	31		LSB				0
Block 2	Number	Wafer#	DW				
Bit No.	1 … 12	13 … 17	18 … 31 32				
	12 bit	5 bit	15 bit				
Example:	"0000 1010 0100b"	"0110 0b"	"000 0100 1101 0010b"				

(Example is for Atmel ATA5570C, Year: 2009, Quarter: 1st, Number: 0164, Wafer#: 12, DW: 1234)

ACL	Allocation class as defined in ISO/IEC 15963-1 = E0h
MFC	Atmel Corporation's manufacturer code as defined in ISO/IEC 7816-6 = 15h
CID	5bit Chip ID for identification of the different products "00011b" for Atmel ATA5570C
ICR	3 bit IC revision to identify foundry and/or revision of IC
Year	1 digit BCD encoded year of manufacturing
Quarter	2bits for quarter of manufacturing
Number	14bits of consecutive number
Wafer#	5bits for wafer number
DW	15bits designating sequential die number on wafer

4. Operating the Atmel ATA5570C

4.1 Initialization and POR Delay

The Power-On-Reset (POR) circuit remains active until an adequate voltage threshold has been reached. This in turn triggers the default start-up delay sequence. During this configuration period of about 192 field clocks, the Atmel® ATA5570C is initialized with the configuration data stored in EEPROM block 0. If the POR delay bit is reset, no additional delay is observed after the configuration period. Tag modulation in regular-read mode will be observed about 3ms after entering the RF field. If the POR delay bit is set, the ATA5570C remains in a permanent damping state until 8190 internal field clocks have elapsed.

$$T_{INIT} = (192 + 8190 \times POR\ delay) \times T_C \approx 67ms; \qquad T_C = 8\ \mu s\ at\ 125kHz$$

Any field gap occurring during this initialization phase will restart the complete sequence. After this initialization time the Atmel ATA5570C enters regular-read mode and modulation starts automatically, using the parameters defined in the configuration register.

4.2 Tag-to-reader Communication

During normal operation, the data stored within the EEPROM is cycled and the COIL1 and COIL2 terminals are load modulated. This resistive load modulation can be detected at the reader module.

4.3 Regular-read Mode

In regular-read mode, data from the memory is transmitted serially, starting with block 1, bit 1, up to the last block (e.g., 7), bit 32. The last block which will be read is defined by the mode parameter field MAXBLK in EEPROM block 0. When the data block addressed by MAXBLK has been read, data transmission restarts with block 1, bit 1.

The user may limit the cyclic datastream in regular-read mode by setting the MAXBLK between 0 and 7 (representing each of the 8 data blocks). If set to 7, blocks 1 through 7 can be read. If set to 1, only block 1 is transmitted continuously. If set to 0, the contents of the configuration block (normally not transmitted) can be read. In the case of MAXBLK = 0 or 1, regular-read mode can not be distinguished from block-read mode.

Figure 4-1. Examples of Different MAXBLK Settings
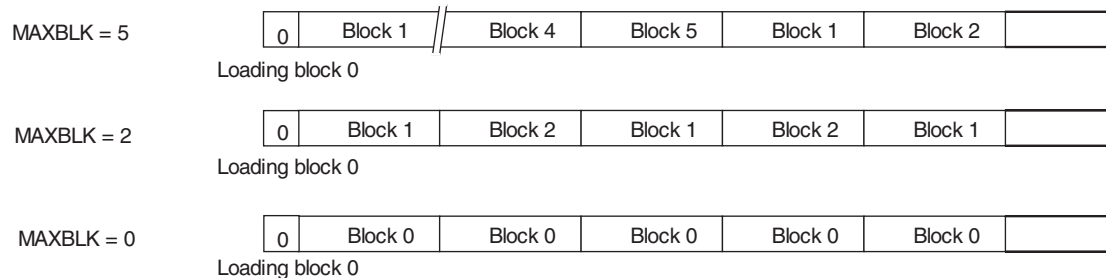
Every time the Atmel® ATA5570C enters regular- or block-read mode, the first bit transmitted is a logical "0". The data stream starts with block 1, bit 1, continues through MAXBLK, bit 32, and cycles continuously if in regular-read mode.

This behavior is different from the original Atmel e555x and helps to decode PSK-modulated data.

4.4 Block-read Mode

With the direct access command, the addressed block is repetitively read only. This mode is called block-read mode. Direct access is entered by transmitting the page access opcode ("10" or "11"), a single "0" bit, and the requested 3-bit block address, when the tag is in normal mode.

In password mode (PWD bit set), the direct access to a single block needs the valid 32-bit password to be transmitted after the page access opcode, whereas a "0" bit and the 3-bit block address follow afterwards. In case the transmitted password does not match with the contents of block 7, the ATA5570C tag returns to the regular-read mode.

Note: A direct access to block 0 of page 1 will read the configuration data of block 0, page 0.
A direct access to block 3 to 7 of page 1 reads all data bits as zero.

4.5 Atmel e5550 Sequence Terminator

The sequence terminator (ST) is a special damping pattern which is inserted before the first block and may be used to synchronize the reader. This Atmel® e5550-compatible sequence terminator consists of four bit periods with underlaying data values of "1". During the second and the fourth bit period, modulation is switched off (if Manchester coding is activated, then modulation is switched on). Bi-phase modulated data blocks need fixed leading and trailing bits in combination with the sequence terminator to be reliably identified.

The sequence terminator may be individually enabled by setting mode bit 29 (ST = "1") in the Atmel e5550-compatibility mode (X-mode = "0").

In the regular-read mode, the sequence terminator is inserted at the start of each MAX-BLK-limited read data stream. In block-read mode, after any block-write or direct access command, or if MAXBLK was set to "0" or "1", the sequence terminator is inserted before the transmission of the selected block.

This behavior is different from former Atmel e5550-compatible ICs (Atmel T5551, Atmel T5554).

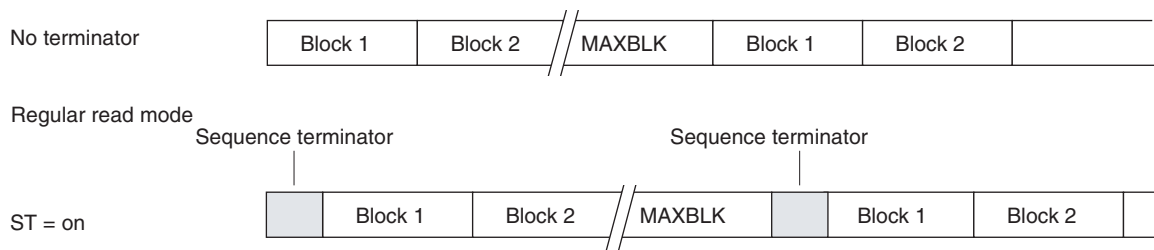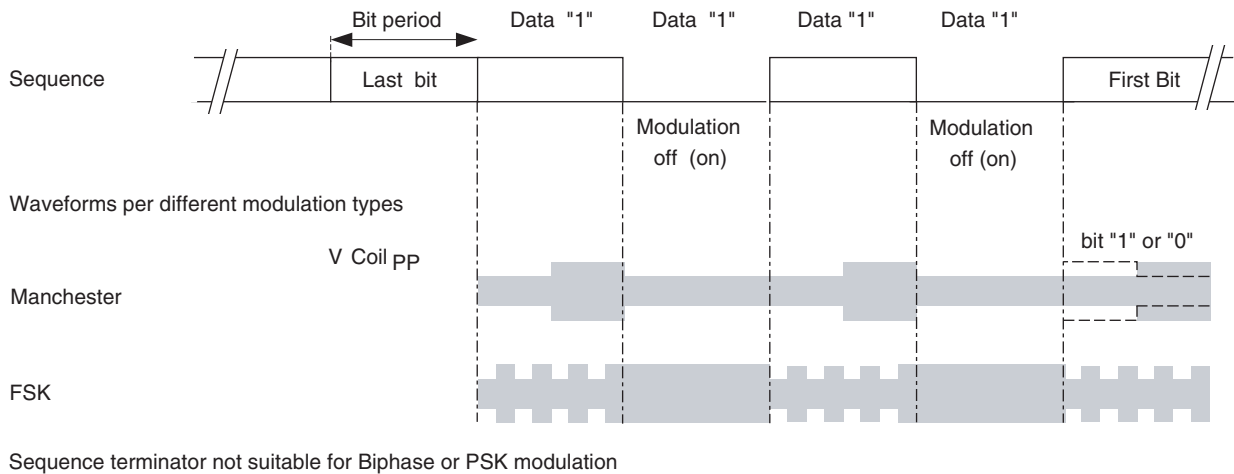**Figure 4-2.** Read Data Stream with Sequence Terminator

Figure 4-3. Atmel® e5550-compatible Sequence Terminator Waveforms

Sequence terminator not suitable for Biphase or PSK modulation

4.6 Reader-to-tag Communication

Data is written to the tag by interrupting the RF field with short field gaps (on-off keying) in accordance with the Atmel e5550 write method. The time between two gaps encodes the "0" or "1" information to be transmitted (pulse interval encoding). The duration of the gaps is usually 50µs to 150µs. The time between two gaps is nominally 24 field clocks for a "0" and 54 field clocks for a "1". When there is no gap for more than 64 field clocks after a previous gap, the Atmel ATA5570C exits the write mode. The tag starts with the command execution if the correct number of bits were received. If there is a failure detected the Atmel ATA5570C does not continue and will enter regular-read mode.

4.7 Start Gap

The initial gap is referred to as the start gap. This triggers the reader-to-tag communication. During this mode of operation, the receive damping is permanently enabled to ease gap detection. The start gap may need to be longer than subsequent gaps in order to be detected reliably.

A start gap will be accepted at any time after the mode register has been loaded ($\geq$ 3ms). A single gap will not change the previously selected page (by former opcode "10" or "11").

Figure 4-4. Start of Reader-to-tag Communication
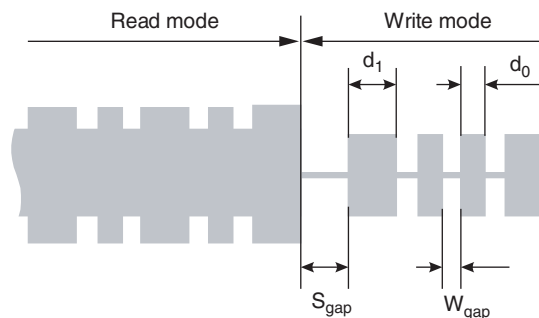
Table 4-1. Write-data Decoding Scheme

Parameters	Remark	Symbol	Min	Max	Unit
Start gap	–	Sgap	10	50	FC
Write gap	Normal write mode	Wgap	8	30	FC
Write data in normal mode	"0" data	d0	16	31	FC
	"1" data	d1	48	63	FC

4.8 Write-data Protocol

The Atmel® ATA5570C expects to receive a dual-bit opcode as the first two bits of a reader command sequence. There are three valid opcodes:

- The opcodes "10" and "11" precede all block-write and direct-access operations for page 0 and page 1
- The RESET opcode "00" initiates a POR cycle
- The opcode "01" precedes all test-mode write operations. Any test-mode access is ignored after the master key (bits 1 to 4) in block 0 has been set to "6". Any further modifications of the master key are prohibited by setting the lock bit of block 0 or the OTP bit.

Writing has to follow these rules:

- Standard write needs the opcode, the lock bit, 32 data bits and the 3-bit address (38bits total)
- Protected write (PWD bit set) requires a valid 32-bit password after opcode and before data and address bits
- For the AOR wake-up command an opcode and a valid password are necessary to select and activate a specific tag

Note: The data bits are read in the same order as written.

If the transmitted command sequence is invalid, the Atmel ATA5570C enters regular-read mode with the previously selected page (by former opcode "10" or "11").

Figure 4-5. Complete Writing Sequence
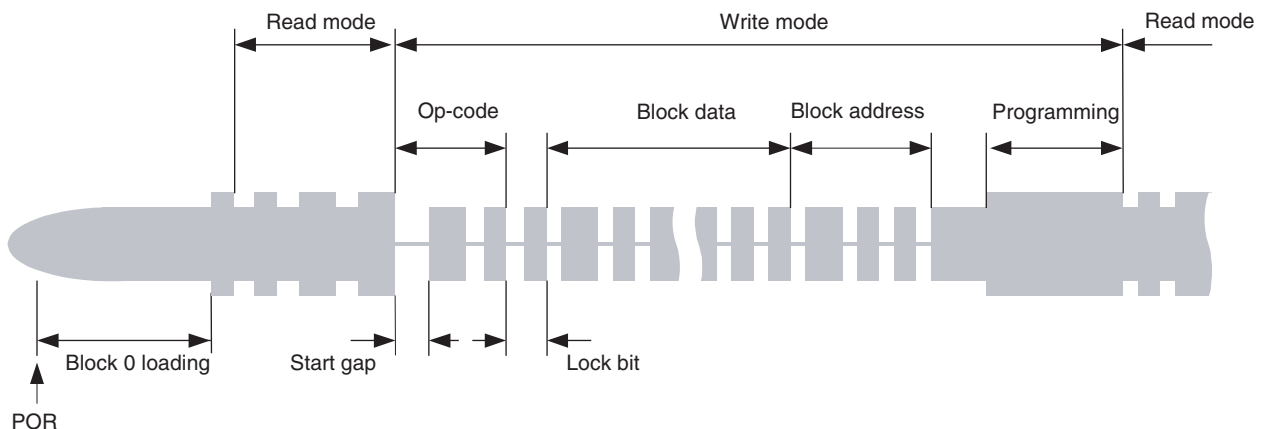
Figure 4-6. Atmel® ATA5570 Command Formats

```
                              OP
Standard write             | 1p* | L | 1        Data        32 | 2  Addr  0 |

Protected write            | 1p* | 1     Password    32 | L | 1        Data        32 | 2  Addr  0 |

AOR (wake-up command)      | 10  | 1     Password    32 |

Direct access (PWD = 1)    | 1p* | 1     Password    32 | 0 | 2  Addr  0 |

Direct access (PWD = 0)    | 1p* | 0 | 2  Addr  0 |

Page  0/1 regular read     | 1p* |

Reset command              | 00  |                      * p = page selector
```

4.9   Password

When password mode is active (PWD = 1), the first 32bits after the opcode are regarded as the password. They are compared bit-by-bit with the contents of block 7, starting at bit 1. If the comparison fails, the Atmel ATA5570C will not program the memory, instead it will restart in regular-read mode once the command transmission is finished.

Note: In password mode, MAXBLK should be set to a value below 7 to prevent the password from being transmitted by the Atmel ATA5570C.

Each transmission of the direct access command (two opcode bits, 32bits password, "0" bit plus 3 address bits = 38bits) needs about 18ms. Testing all possible combinations (about 4.3billion) would take about two years.

4.10   Answer-on-request (AOR) Mode

When the AOR bit is set, the Atmel ATA5570C does not start modulation in the regular-read mode after loading configuration block 0. The tag waits for a valid AOR data stream ("wake-up command") from the reader before modulation is enabled. The wake-up command consists of the opcode ("10") followed by a valid password. The selected tag will remain active until the RF field is turned off or a new command with a different password is transmitted which may address another tag in the RF field.

Table 4-2. Atmel® ATA5570C – Modes of Operation

PWD	AOR	Behavior of Tag After Reset Command or POR	De-activate Function
1	1	Answer-on-request (AOR) mode: - Modulation starts after wake-up with a matching password - Programming needs valid password	Command with non-matching password deactivates the selected tag
1	0	Password mode: - Modulation in regular-read mode starts after reset - Programming and direct access needs valid password	
0	--	Normal mode: - Modulation in regular-read mode starts after reset - Programming and direct access without password	

Figure 4-7. Answer-on-request (AOR) Mode
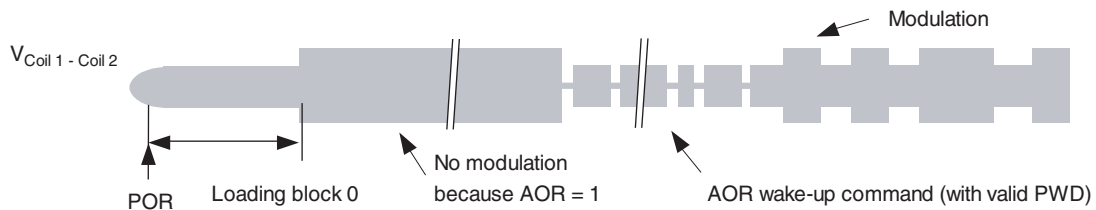
Figure 4-8. Coil Voltage After Programming of a Memory Block
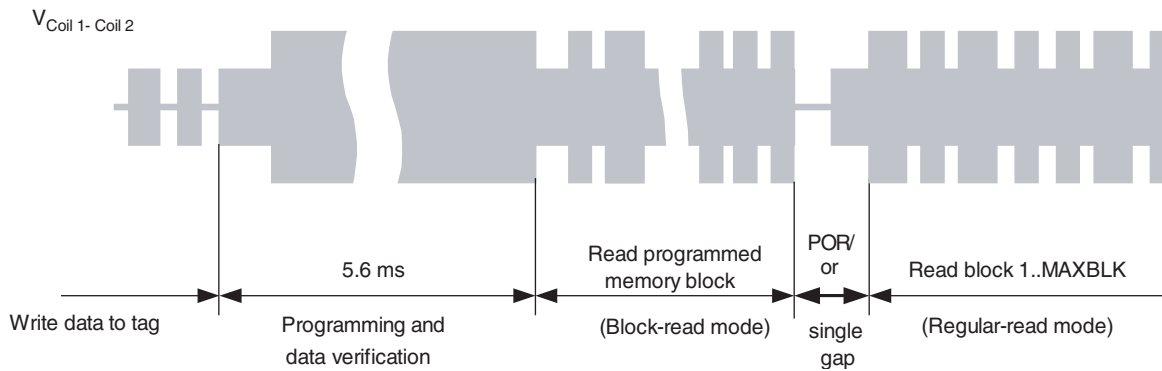
Figure 4-9. Anticollision Procedure Using AOR Mode
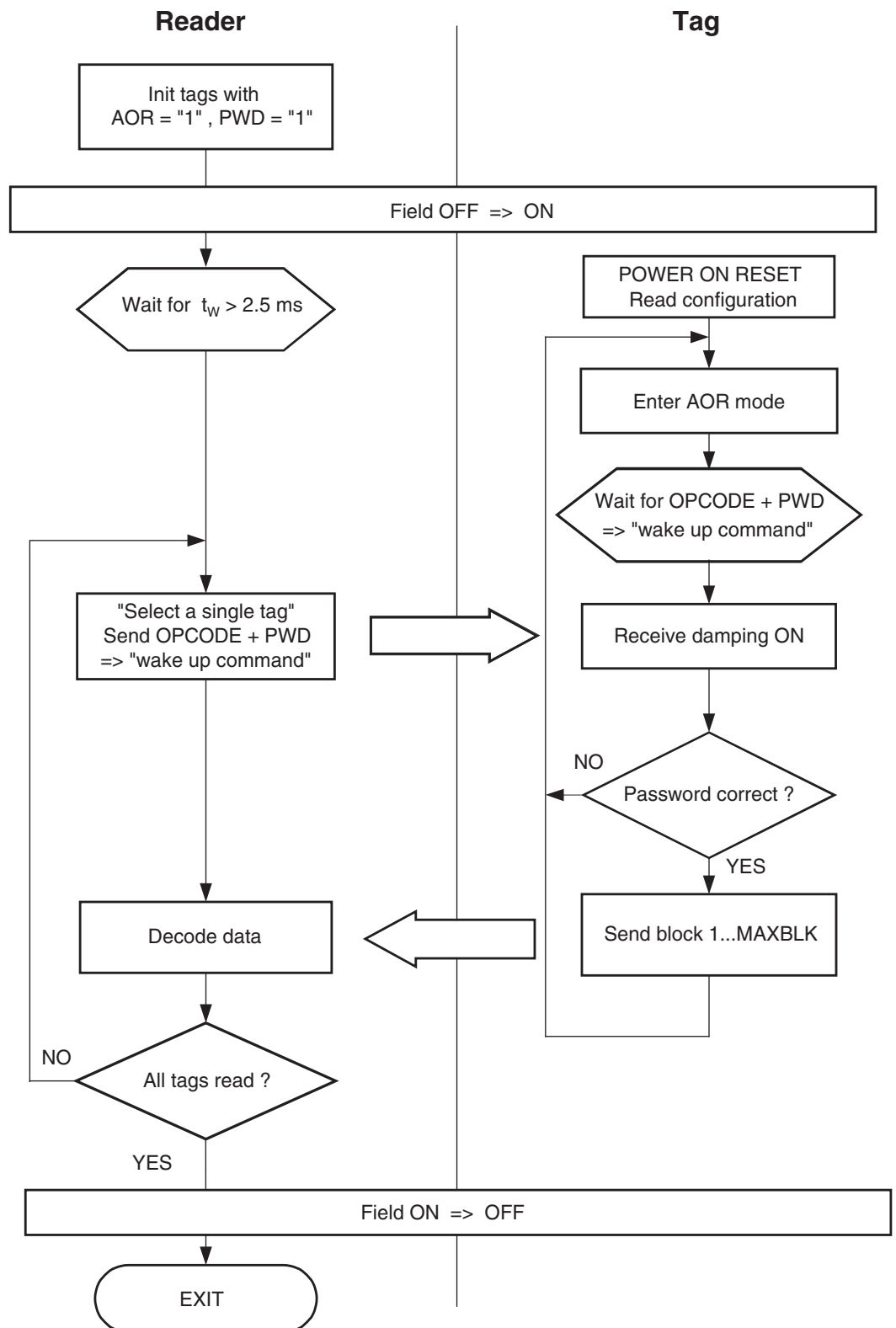
4.11 Programming

When all necessary information has been received by the Atmel® ATA5570C, programming may proceed. There is a clock delay between the end of the writing sequence and the start of programming.

Typical programming time is 5.6ms. This cycle includes a data verification read to grant secure and correct programming. After programming is successfully executed, the Atmel ATA5570C enters block-read mode transmitting the block just programmed (Figure 4-8 on page 12).

Note: This timing and behavior is different from the e555x-family predecessors.

5. Error Handling

Several error conditions can be detected to ensure that only valid bits are programmed into the EEPROM. There are two error types, which lead to two different actions.

5.1 Errors During Writing

The following detectable errors could occur during writing data to the Atmel ATA5570C:

- Wrong number of field clocks between two gaps (i.e., not a valid "1" or "0" pulse stream)
- Password mode is activated and the password does not match the contents of block 7
- The number of bits received in the command sequence is incorrect

Valid bit counts accepted by the Atmel ATA5570C are:

Password write	70 bits	(PWD = 1)
Standard write	38 bits	(PWD = 0)
AOR wake up	34 bits	(PWD = 1)
Direct access with PWD	38 bits	(PWD = 1)
Direct access	6 bits	(PWD = 0)
Reset command	2 bits	
Page 0/1 regular-read	2 bits	

If any of these erroneous conditions are detected, the Atmel ATA5570C enters regular-read mode, starting with block 1 of the page defined in the command sequence.

5.2 Errors Before/During Programming

If the command sequence was received successfully, the following error could still prevent programming:

- The lock bit of the addressed block is already set

In case of a locked block, programming mode will not be entered. The Atmel ATA5570C reverts to block-read mode, continuously transmitting the currently addressed block.

If the command sequence is validated and the addressed block is not write-protected, the new data will be programmed into the EEPROM memory. The new state of the block-write protection bit (lock bit) will be programmed at the same time accordingly.

Each programming cycle consists of 4 consecutive steps.

1. Erase block
2. Erase verification (data = "0")
3. Programming
4. Write verification (corresponding data bits = "1")

- If a data verification error is detected after an executed data block programming, the tag will stop modulation (modulation defeat) until a new command is transmitted.

Figure 5-1. ATA5570C Functional Diagram
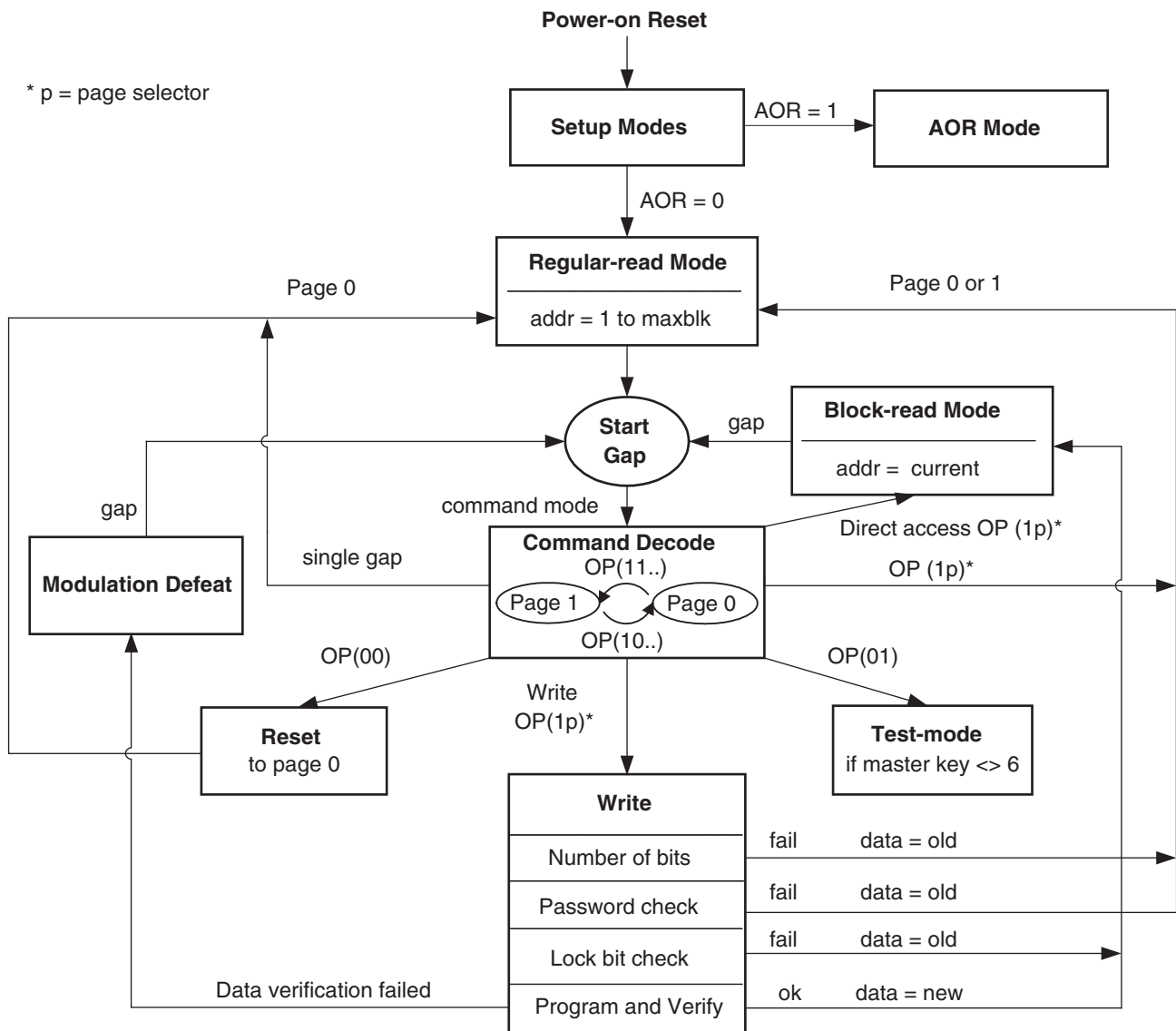
6. Atmel ATA5570C in Extended Mode (X-mode)

In general, the block 0 setting of the master key (bits 1 to 4) to the value "6" or "9" together with the X-mode bit will enable the extended mode functions.

- Master key = "9": Test mode access and extended mode are both enabled.
- Master key = "6": Any test mode access will be denied but the extended mode is still enabled.

Any other master key setting will prevent the activation of the Atmel ATA5570C extended mode options, even when the X-mode bit is set.

6.1 Binary Bit-rate Generator

In extended mode the data rate is binary programmable to operate at any data rate between RF/2 and RF/128 as given in the formula below.

Data rate = RF/(2n + 2)

6.2 OTP Functionality

If the OTP bit is set to "1", all memory blocks are write protected and behave as if all lock bits are set to "1". If, additionally, the master key is set to "6", the Atmel® ATA5570C mode of operation is locked forever (= OTP functionality).

If the master key is set to "9", the test-mode access allows the re-configuration of the tag.

Figure 6-1. Block 0 – Configuration Map in Extended Mode (X-mode)

Table 6-1. Atmel® ATA5570C Types of Modulation in Extended Mode and Sensor Input $R_S < 100k\Omega$ Typical

Mode	Direct Data Output Encoding	Inverse Data Output Encoding
FSK1[1]	FSK/5, FSK/8; "0" = RF/5; "1" = RF/8	FSK/8, FSK/5; "0" = RF/8; "1" = RF/5 (= FSK1a)
FSK2[1]	FSK/10, FSK/8; "0" = RF/10; "1" = RF/8	FSK/8, FSK/10; "0" = RF/8; "1" = RF/10 (= FSK2a)
PSK1[2]	Phase change when input changes	Phase change when input changes
PSK2[2]	Phase change on bit clock if input high	Phase change on bit clock if input low
PSK3[2]	Phase change on rising edge of input	Phase change on falling edge of input
Manchester	"0" = falling edge "1" = rising edge on mid-bit	"1" = falling edge "0" = rising edge on mid-bit
Bi-phase 1 ('50)	"1" creates an additional mid-bit change	"0" creates an additional mid-bit change
Bi-phase 2 ('57)	"0" creates an additional mid-bit change	"1" creates an additional mid-bit change
NRZ	"1" = damping on, "0" = damping off	"0" = damping on, "1" = damping off

Notes: 1. A common multiple of bit rate and FSK frequencies is recommended.

2. In PSK mode the selected data rate has to be an integer multiple of the PSK sub-carrier frequency.

6.3 Sequence Start Marker

**Figure 6-2.** Atmel ATA5570C Sequence Start Marker in Extended Mode
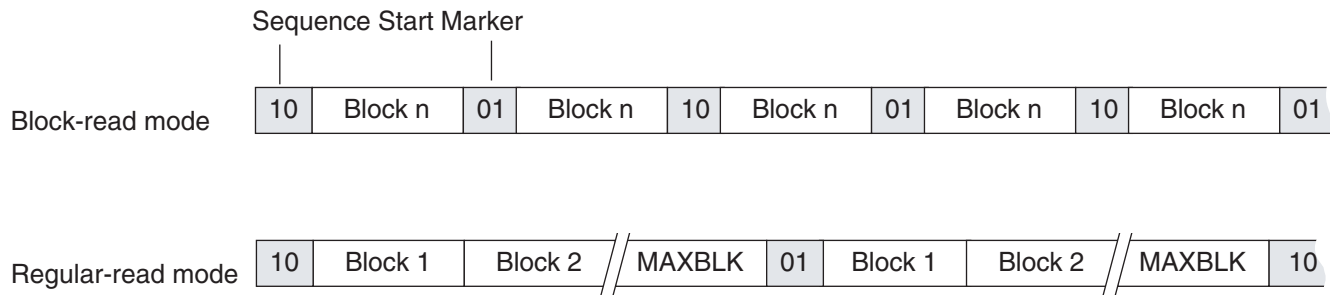
The Atmel® ATA5570C sequence-start marker is a special damping pattern which may be used to synchronize the reader. The sequence start marker consists of two bits ("01" or "10") which are inserted as header before the first block to be transmitted if the bit 29 in extended mode is set. At the start of a new block sequence, the value of the two bits is inverted.

6.4 Inverse Data Output

The Atmel ATA5570C supports in its extended mode (X-mode) an inverse data output option. If inverse data is enabled, the modulator as shown in Figure 6-3 works on inverted data (see Table 6-1). This function is supported for all basic types of encoding. Table 6-1 shows the modulation, when R_S < 100kΩ typical.

Figure 6-3. Data Encoder for Inverse Data Output
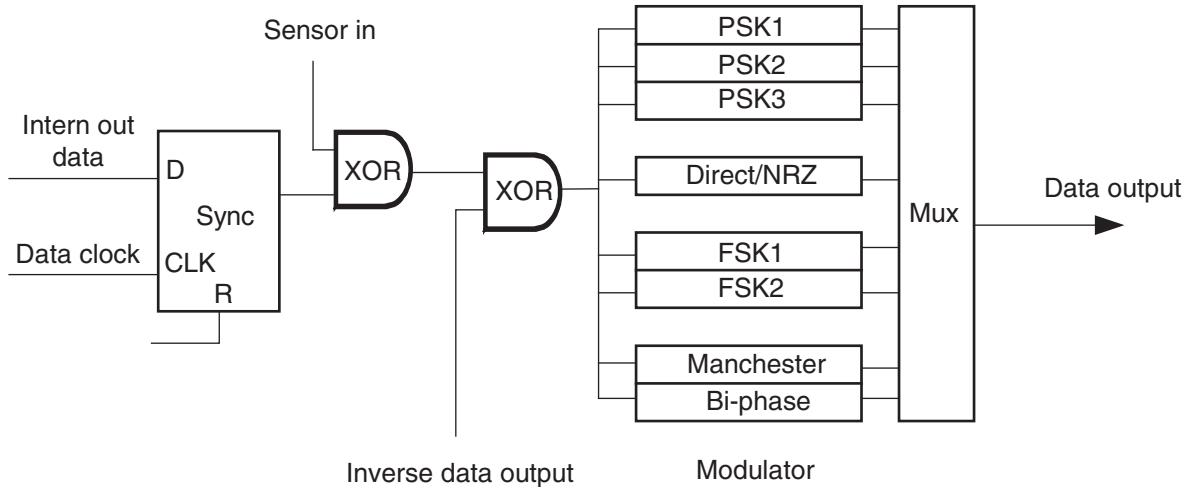
6.5 Fast Write

In the optional fast-write mode the time between two gaps is nominally 12 field clocks for a "0" and 27 field clocks for a "1". When there is no gap for more than 32 field clocks after a previous gap, the ATA5570C will exit the write mode. Please refer to Table 6-2 and Figure 4-6 on page 11.

Table 6-2. Fast Write Decoding Schemes

Parameters	Remark	Symbol	Min	Max	Unit
Start gap	–	Sgap	10	50	FC
Write gap	Normal write mode	Wngap	8	30	FC
	Fast write mode	Wfgap	8	20	FC
Write data in normal mode	"0" data	d0	16	31	FC
	"1" data	d1	48	63	FC
Write data in fast mode	"0" data	d0	8	15	FC
	"1" data	d1	24	31	FC

Figure 6-4. Example of Manchester Coding With Data Rate RF/16
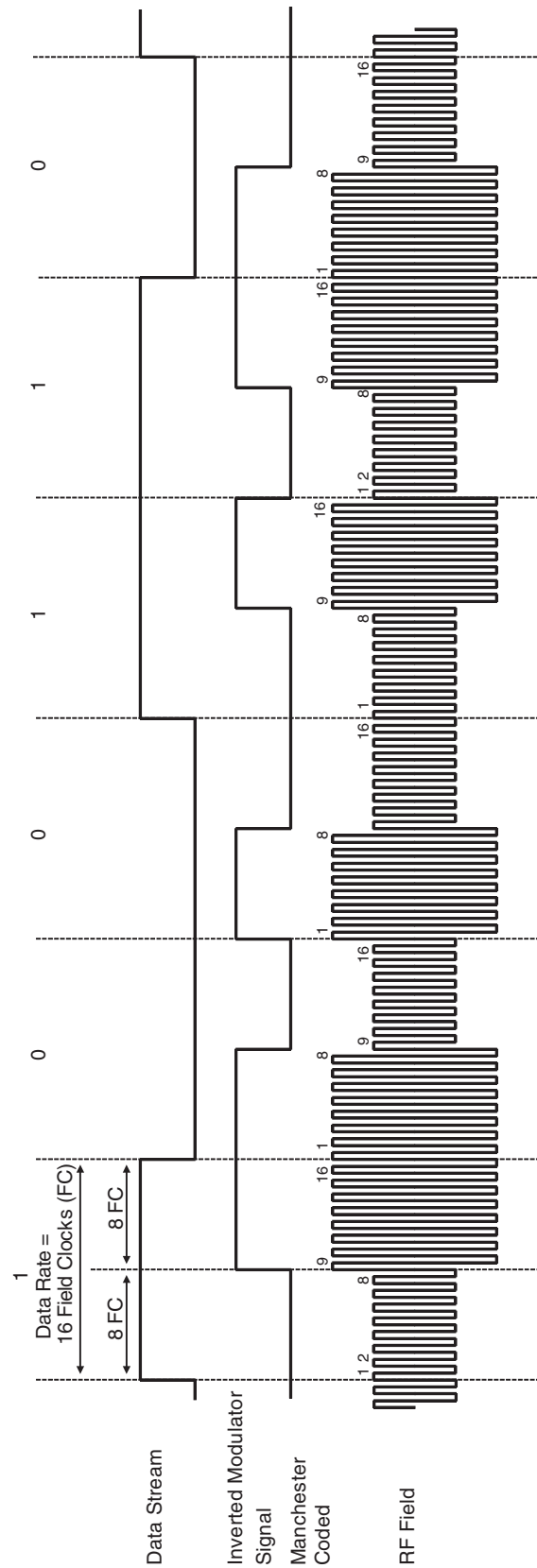
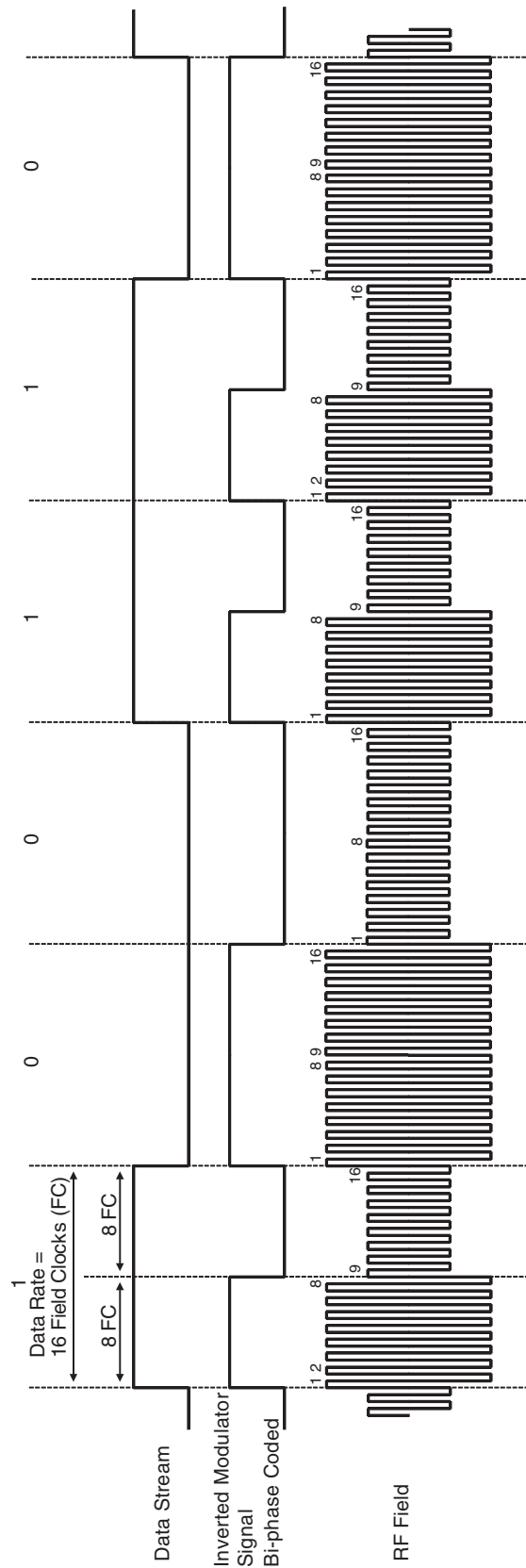**Figure 6-5.** Example of Bi-phase Coding With Data Rate RF/16

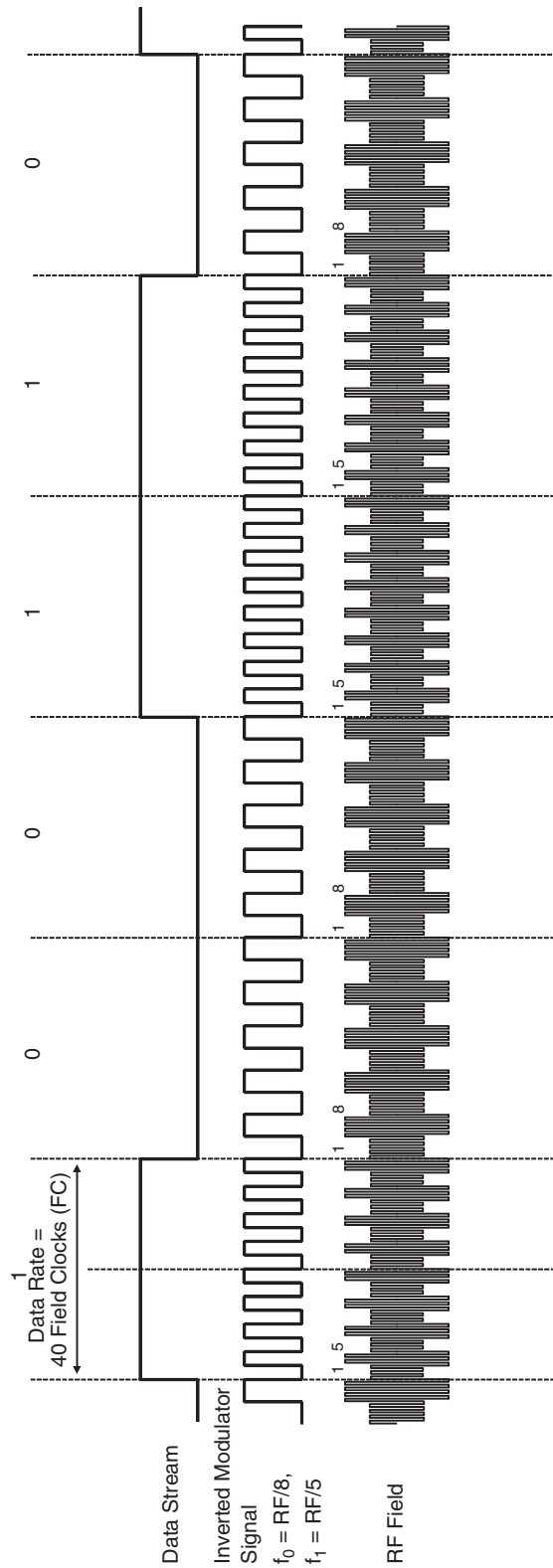**Figure 6-6.** Example: FSK1a Coding With Data Rate RF/40, Subcarrier $f_0 = RF/8$, $f_1 = RF/5$

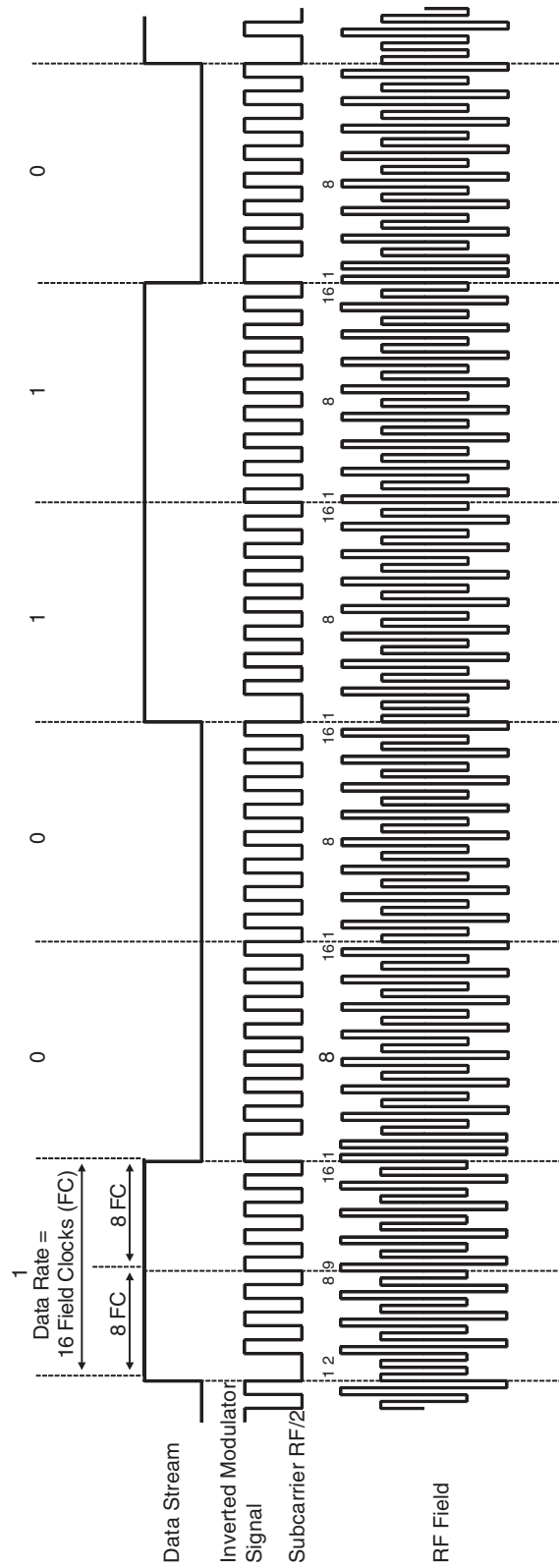**Figure 6-7.** Example of PSK1 Coding With Data Rate RF/16

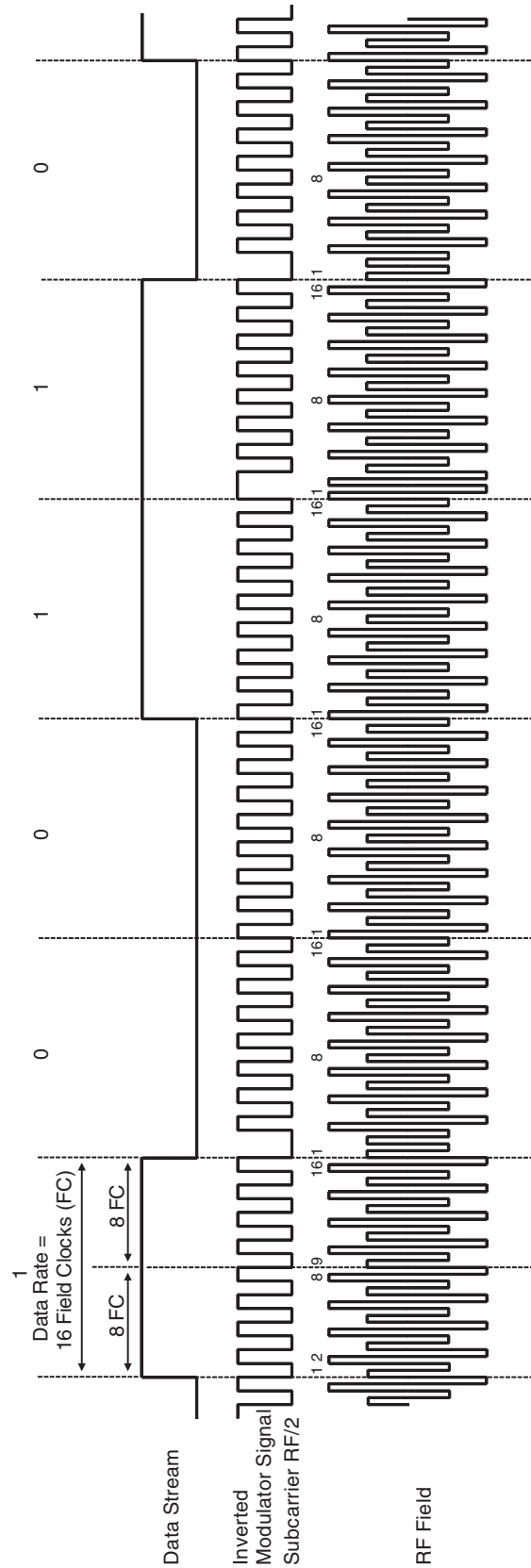**Figure 6-8.** Example of PSK2 Coding With Data Rate RF/16

Figure 6-9. Example of PSK3 Coding With Data Rate RF/16
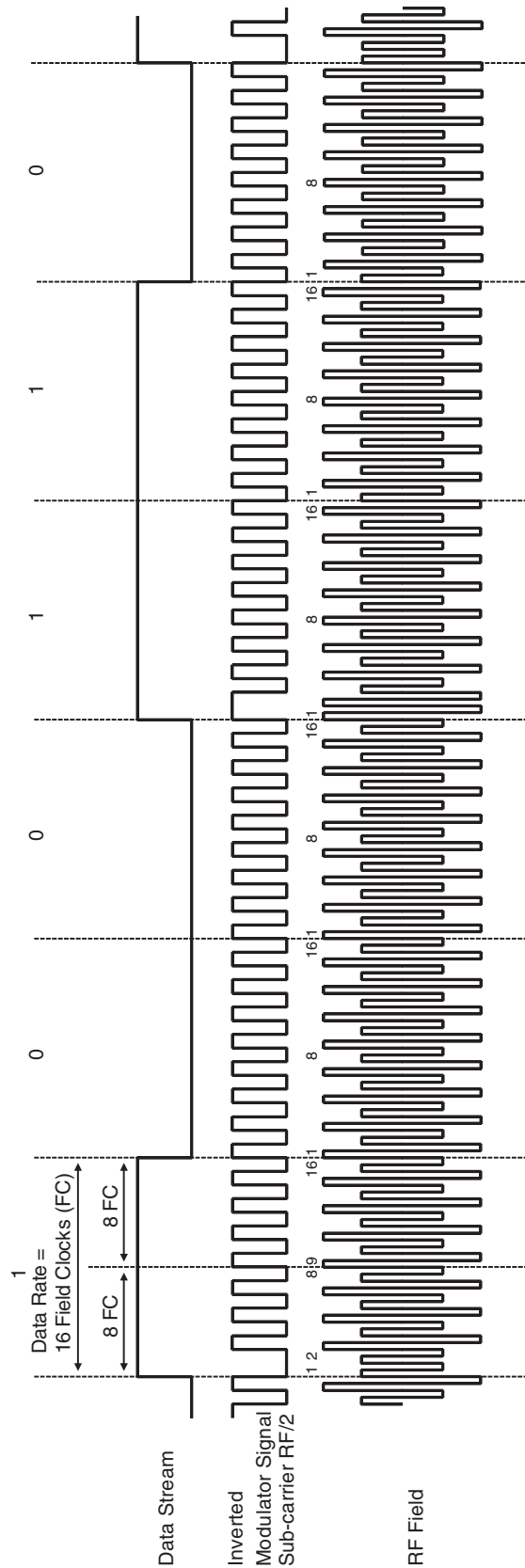
7. Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Pin	Symbol	Value	Unit
Maximum DC current into COIL1/COIL2 (t = 1ms)	2, 7	I_{coil}	20	mA
Maximum AC current into COIL1/COIL2 (f = 125kHz)	2, 7	$I_{coil\ p}$	20	mA
Power dissipation (dice)[1]	2, 7	P_{tot}	100	mW
Operating ambient temperature range		T_{amb}	−25 to +105	°C
Storage temperature range[2]		T_{stg}	−40 to +150	°C

Notes: 1. Free-air condition, time of application: 1s

2. Data retention reduced at high temperature

8. Operating Characteristics

All parameters given are valid for T_{amb} = +25°C and f_{coil} = 125 kHz, unless otherwise specified.

| No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
1	RF frequency range		2, 7	f_{RF}	100	125	150	kHz	
2.1 2.2	Supply current (without current consumed by the external LC tank circuit and without external resistance on sensor input)	T_{amb} = 25°C	2, 7	I_{DD}		1.5	3	µA	T
		Read T_{amb} = −25°C to +85°C	2, 7	I_{DD}		2	4	µA	Q
3.1	Coil voltage (AC supply)	Necessary for read[1]	2, 7	$V_{coil\ pp}$	10		V_{clamp}	V_{pp}	Q
4	Clamp voltage	10mA current into COIL1/COIL2	2, 7	V_{clamp}	17		23	V_{pp}	T
5	Startup time[2]			$t_{startup}$		2.5	3	ms	Q
6.1 6.2	Data retention	T_{op} = 55°C		$t_{retention}$	10	20	50	year	Q
		T_{stg} = 150°C		$t_{retention}$	96			h	T[3]
7	Programming cycles	Erase all/Write all		n_{cycle}	100,000			cycles	Q
8	Sensor Input	Trip point resistance (modulation inverted)	4, 5	R_T	50	100	200	kΩ	T
9	Resonance capacitor C_R[4]	See Figure 2-1 on page 2		C_R	323	340	357	pF	T
10	Q-factor of coil L_R			Q_L	15	20	25		Q

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter, Q = guaranteed based on initial product qualification data, T = directly or indirectly tested during production.

Notes: 1. Current into COIL1/COIL2 has to be limited to 20mA

2. Time from field on to modulation start

3. Tested on wafer basis

4. Only available in SO8 package version

9. Reliability

Parameters	Symbol	Value	Unit
Electrostatic discharge ESD S.5.1 (Human Body Model)	V_{max}	2000	V
Electrostatic discharge JEDEC A115A (Machine Model)	V_{max}	200	V
Lifetime in SO8 at T_{op} =150°C	t_L	1008	h

Figure 9-1. Measurement Setup for I_{DD} and V_{mod}
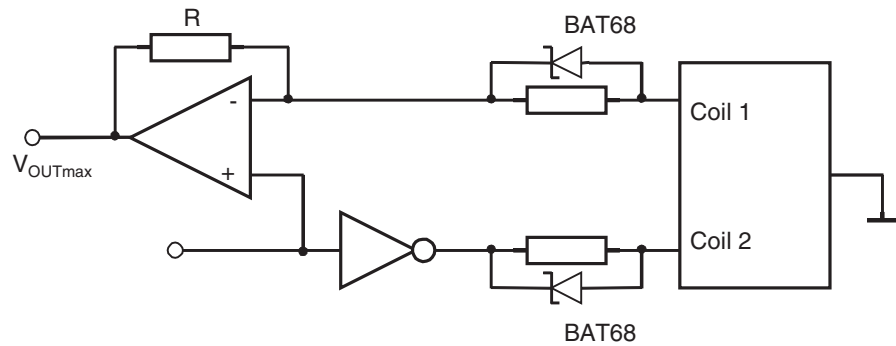
10. Ordering Information

Extended Type Number	Package	Drawing
ATA557001C-DDB	6" sawn wafer on foil with ring, thickness 150µm (approx. 6mil)	Figure 11-2 on page 28
ATA557001C-DDT	Die in waffle pack, thickness 150µm (approx. 6mil)	Figure 11-3 on page 29
ATA557001C-TAQY	SO8 package with additional resonance capacitor of 340pF	Figure 11-4 on page 30

11. Package Information

Figure 11-1. Pad Layout

Dimensions in µm
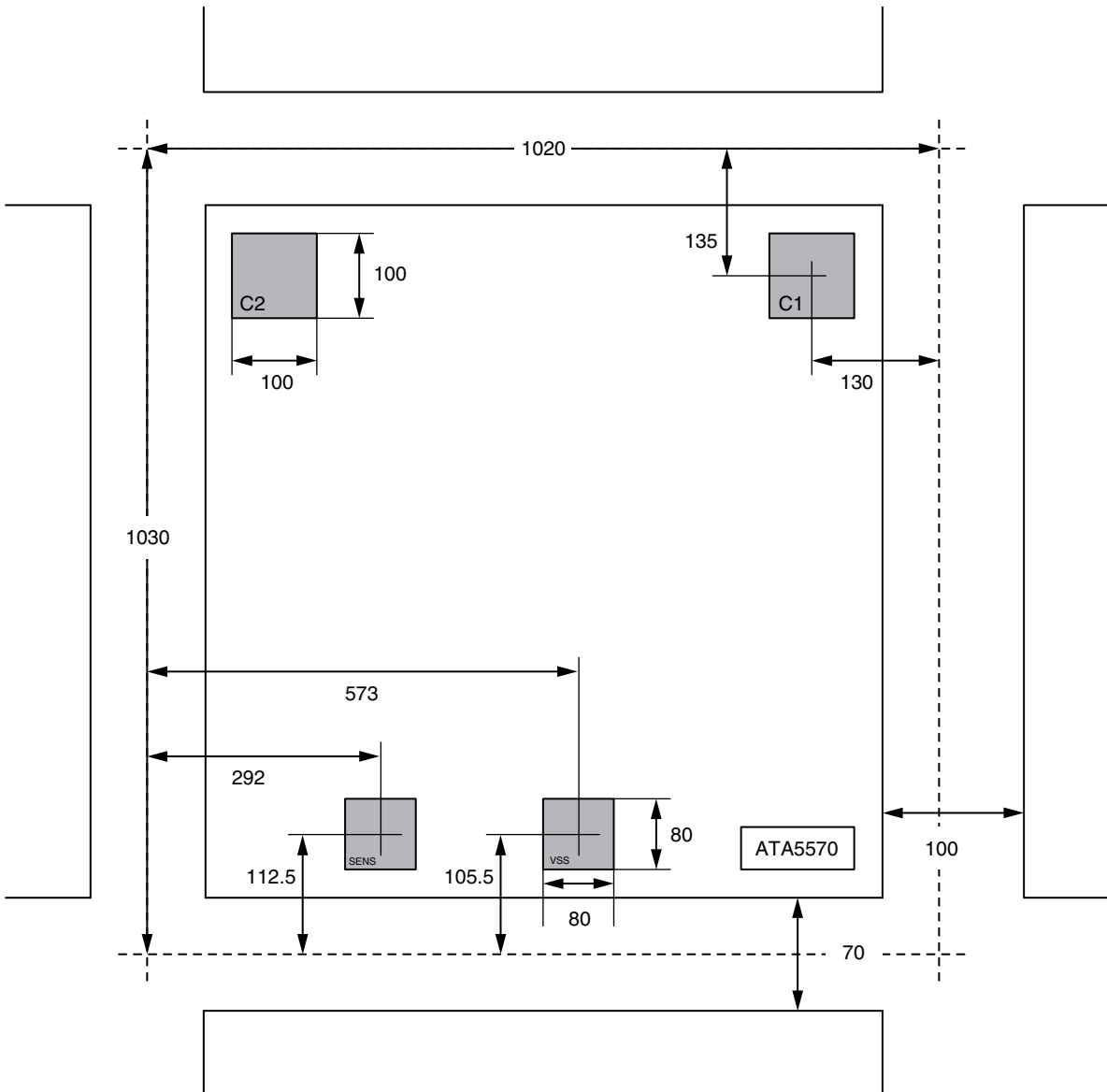
Figure 11-2. Sawn Wafer on Foil with Ring

Die Dimensions

20:1

technical drawings according to DIN specifications

Dimensions in mm

Orientation on frame

Option
xx
01

Label:
Prod: ATA5570xxC-DDB
Lot no:
Wafer no:
Qty:

Wafer ATA5570xxC-DDB

Adwill D176

6" Wafer frame, plastic thickness 2.5mm

10/01/10

	TITLE	**DRAWING NO.**	**REV.**
Package Drawing Contact: packagedrawings@atmel.com	**Dimensions** ATA5570xxC-DDB	9.920-6704.01-4	1

Figure 11-3. Die in Waffle Pack

20:1

Chip Dimensions ATA5570xxC-DDT

technical drawings according to DIN specifications

Dimensions in mm

Option xx
01

0.15±0.012

0.0035±0.001
Polyimide

0.1535±0.013

K0

5:1

Tray: H20-050x12
Material: PS, black, conductive
Qty. per tray: 400

COMMON DIMENSIONS
(Unit of Measure = mm)

A0	B0	K0
1.27	1.27	0.35

Chip orientation

Chip identification ATA5570

02/28/11

	TITLE	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**Chip Dimensions** ATA5570xxC-DDT	9.920-6705.02-4	1

Figure 11-4. SO8 Package

Package: SO 8

Dimensions in mm
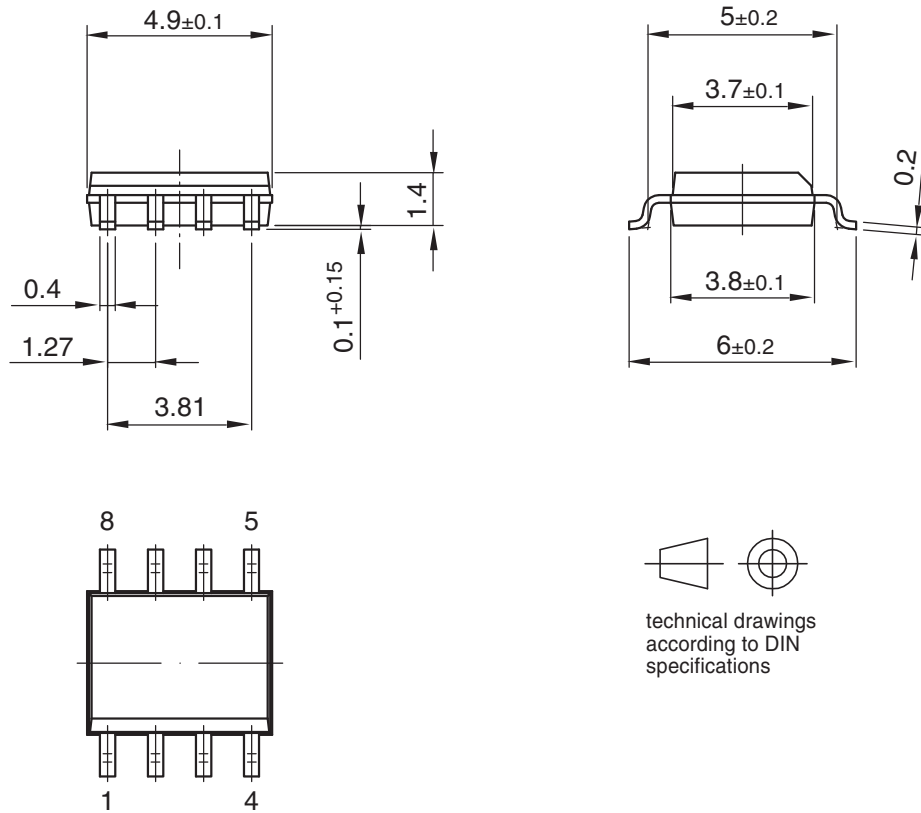
Drawing-No.: 6.541-5031.01-4

Issue: 1; 15.08.06

technical drawings according to DIN specifications

11.1 Pin Configuration of SO8 Version

Figure 11-5. Pinning SO8
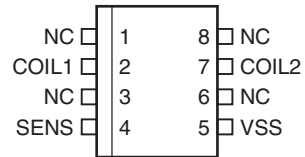
Table 11-1. Pin Description

Pin	Symbol	Function
1	NC	Not connected
2	COIL1	Antenna pin 1
3	NC	Not connected
4	SENS	Sensor input
5	VSS	Ground
6	NC	Not connected
7	COIL2	Antenna pin 2
8	NC	Not connected

12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9191B-RFID-05/11	• Figure 3-2 "Block 0 Configuration Mapping – Atmel® e5550 Compatibility Mode" on page 4 changed

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