Laird
Smart Technology. Delivered.™

User Guide

SU60-SIPT Development Kit (DVK-SU60-SIPT)

Version 1.0

REVISION HISTORY

Version	Date	Notes	Approver
1.0	29 July 2017	Initial Release	Jay White

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

CONTENTS

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

1 Overview

The Laird SU60-SIPT development kit provides a platform for rapid wireless connectivity prototyping, providing multiple options for the development of Wi-Fi and Bluetooth applications.

This guide applies to Rev. 01 of the development PCB and relates to DVK-SU60-SIPT-B0 on the PCB itself. The complete functionality of the development kit hardware requires the use of Laird SU60-SIPT FW version xx.xx.xx or greater.

Part Number: DVK-SU60-SIPT
Applicable to the following Wi-Fi part number: SU60-SIPT (Dual-band 802.11ac Wi-Fi + Bluetooth v4.2 combo SiP

1.1 Introduction

The Laird SU60-SIPT development kit is designed to support the rapid development of applications and software for the SU60-SIPT of Wi-Fi + Bluetooth modules featuring Laird's innovative event-driven programming language – xxxxxx. More information regarding this product series including additional documentation is available from the product page of the Laird website.

1.2 Package Contents

All kits contain the following:

Development board	The development board has the required SU60-SIPT module installed onto it and exposes all the various hardware interfaces available.
Power options	USB cable – Type A to micro B. The cable also provides serial communications via the FTDI USB – RS232 converter chip on the development board DC barrel plug with clips for connection to external power supply
IDC cable x	Supplied to allow a simple connection to the ? x ? way pin headers into J6, J7, and J8. The IDC cables are 2.54 mm pitch.
SDIO extension cable	Supplied to allow a simple connection to the SDIO socket.
Web link card	Provides links to additional information including the 60-series user guide, schematics, quick start guides, and firmware release notes.

2 SU60-SIPT Development Kit – Main Development Board

This section describes the SU60-SIPT development board hardware. The SU60-SIPT development board is delivered with the SU60-SIPT module but no onboard firmware and applications.

The SU60-SIPT development board is a universal development tool to highlight the capabilities of the SU60-SIPT module. The development kit is supplied in a default configuration which should be suitable for multiple experimentation options. It also offers multiple pin headers that help to create different configurations for SU60-SIPT module. This allows you to test different operating scenarios.

The development board allows the SU60-SIPT module to physically connect to a SDIO host via the supplied SDIO extension cable and USB host via USB cable for development purposes. The development board also provides USB-to-Virtual COM port conversion through a FTDI chip – part number FT232R. Any Windows PC (XP or later) and Linux PC (Ubuntu xx.xx or Fedora xx.xx) should auto-install the necessary drivers; if your PC cannot locate the drivers, you can download them from http://www.ftdichip.com/Drivers/VCP.htm

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

2.1 Key Features

The SU60-SIPT development board contains the following features:

SU60-SIPT module installed on-board
Power supply options for powering development board from:
- USB
- External DC supply
- SDIO interface
- PCIe interface

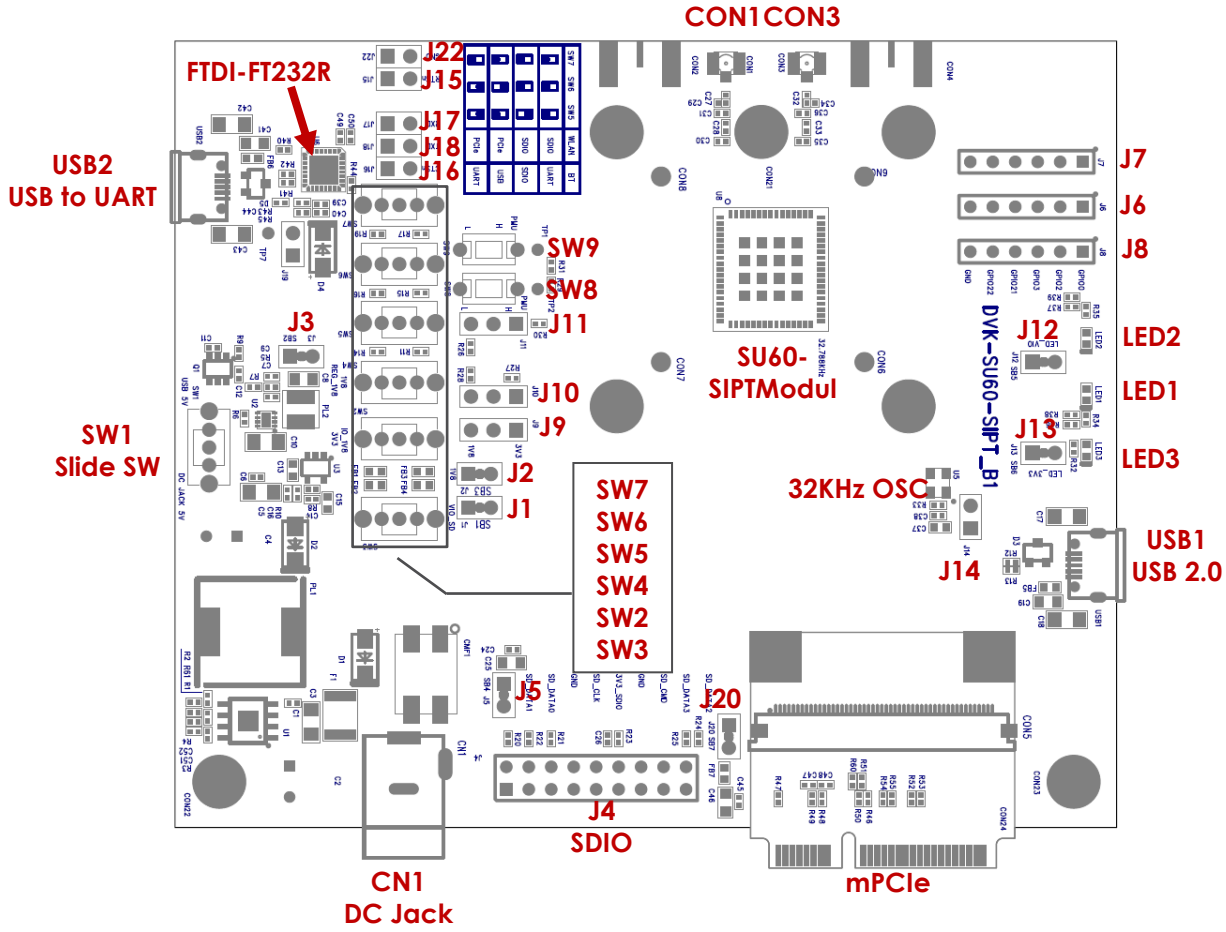
Regulated 3.3 V for powering the SU60-SIPT module. Optional regulated 1.8 V for powering the VCCIO for FTDI chip
USB to UART bridge (FTDI chip)
USB interface for Wi-Fi or Bluetooth
PCIe interface for Wi-Fi
Module UART can be interfaced to:
- USB (PC) using the USB-UART bridge
- External UART source (using IO break-out connector when development board powered from DC jack or SDIO interface)

Current measuring options:
- Pin header (Ammeter)

IO break-out (2.54 mm pitch headers) connectors interface for plugging-in external modules and accessing all interfaces of the SU60-SIPT module [UART, LTE coexistence, PCM, GPIO, JTAG].
Two buttons and LEDs for user interaction
Seven slide switches for DC source, IO level, and host config
External 32 KHz oscillator for the sleep clock

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

2.2 Understanding the Development Board



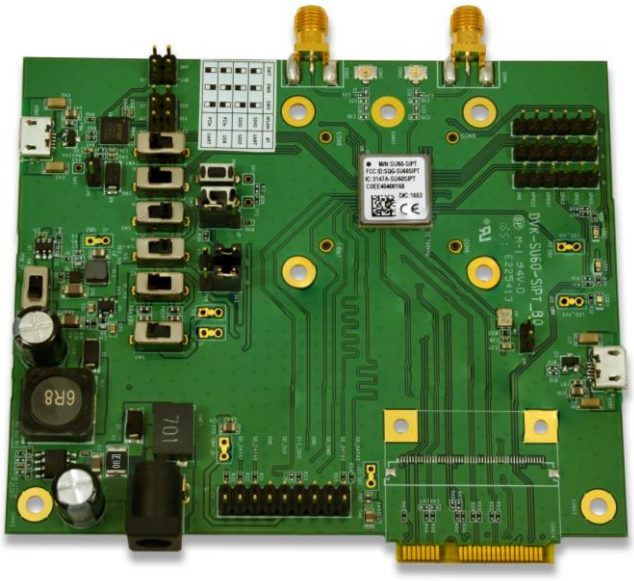


Figure 1: Development board

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

3 Functional Blocks

The development board is formed from the following major functional blocks:

3.1 Pin Definitions

3.1.1 SDIO-Pin Header

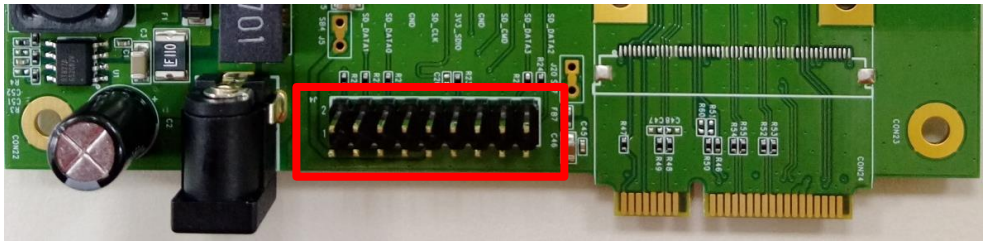


Figure 2: DVK-SU60-SIPT SDIO pin header

Table 1: SDIO pin definitions

Pin #	Name	Type	Voltage Ref.	Description	If Not Used
1	GND	-	-	Ground	GND
2	SDIO DATA2	I/O, PU	1.8V	SDIO 4-bit Mode DATA line Bit[2]	N/C
3	GND	-	-	Ground	GND
4	SDIO DATA3	I/O, PU	1.8V	SDIO 4-bit Mode DATA line Bit[3]	N/C
5	GND	-	-	Ground	GND
6	SDIO CMD	I/O	1.8V	SDIO 4-bit Mode Command/Response	N/C
7	GND	-	-	Ground	GND
8	GND	-	-	Ground	GND
9	SDIO_3V3	Power	-	3.3V module power supply	-
10	SDIO_3V3	Power	-	3.3V module power supply	-
11	GND	-	-	Ground	GND
12	SDIO CLK	I, PU	1.8V	SDIO 4-bit Mode Clock Input	N/C
13	GND	-	-	Ground	GND
14	GND	-	-	Ground	GND
15	GND	-	-	Ground	GND
16	SDIO DATA0	I/O, PU	1.8V	SDIO 4-bit Mode DATA line Bit[0]	N/C
17	GND	-	-	Ground	GND
18	SDIO DATA1	I/O, PU	1.8V	SDIO 4-bit Mode DATA line Bit[1]	N/C

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

3.1.2 PCIe Golden Finger

Table 2: PCIe pin definitions

Pin #	Name	Type	Voltage Ref.	Description	If Not Used
1	PEWAKE0#	I/O	3.3V	PCIe wake signal (input/output) (active low)	N/C
2	PCIE_3V3	Power	-	3.3V module power supply	-
3	-	-	-	-	-
4	GND	-	-	Ground	GND
5	-	-	-	-	-
6	-	-	-	-	-
7	CLKREQ0#	I/O	3.3V	PCIe clock request (input/output) (active low)	GND
8	-	-	-	-	-
9	GND	-	-	Ground	GND
10	-	-	-	-	-
11	REFCLKn0	I	1.8V	PCIe Differential Clock Input-Negative	N/C
12	-	-	-	-	-
13	REFCLKp0	I	1.8V	PCIe Differential Clock Input-Positive	N/C
14	-	-	-	-	-
15	GND	-	-	Ground	GND
16	-	-	-	-	-
17	-	-	-	-	-
18	GND	-	-	Ground	GND
19	-	-	-	-	-
20	W_DISABLE1#	I, PU	3.3V	PCIe host indication to disable the WLAN function of the device (input) (active low)	N/C
21	GND	-	-	Ground	GND
22	PERST0#	I, PD	3.3V	PCIe host indication to reset the device (input) (active low)	N/C
23	PETn0	O	1.8V	PCIe Transmit Data-Negative	N/C
24	PCIE_3V3	Power	-	3.3V module power supply	-
25	PETp0	O	1.8V	PCIe Transmit Data-Positive	N/C
26	GND	-	-	Ground	GND
27	GND	-	-	Ground	GND
28	-	-	-	-	-
29	GND	-	-	Ground	GND
30	-	-	-	-	-
31	PERn0	I	1.8V	PCIe Receive Data-Negative	N/C
32	-	-	-	-	-
33	PERp0	I	1.8V	PCIe Receive Data-Positive	N/C
34	GND	-	-	Ground	GND
35	GND	-	-	Ground	GND

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

Pin #	Name	Type	Voltage Ref.	Description	If Not Used
36	USB_D-	I/O	3.3V	USB Differential Data-Negative	N/C
37	GND	-	-	Ground	GND
38	USB_D+	I/O	3.3V	USB Differential Data-Positive	N/C
39	PCIE_3V3	Power	-	3.3V module power supply	-
40	GND	-	-	Ground	GND
41	PCIE_3V3	Power	-	3.3V module power supply	-
42	-	-	-	-	-
43	GND	-	-	Ground	GND
44	LED1#	O, PU	3.3V	LED indicator for WLAN with 10mA drive capability	N/C
45	-	-	-	-	-
46	LED2#	O, PU	3.3V	LED indicator for BT with 10mA drive capability.	N/C
47	-	-	-	-	-
48	-	-	-	-	-
49	-	-	-	-	-
50	GND	-	-	Ground	GND
51	-	-	-	-	-
52	PCIE_3V3	Power	-	3.3V module power supply	-

3.2 Power Supply

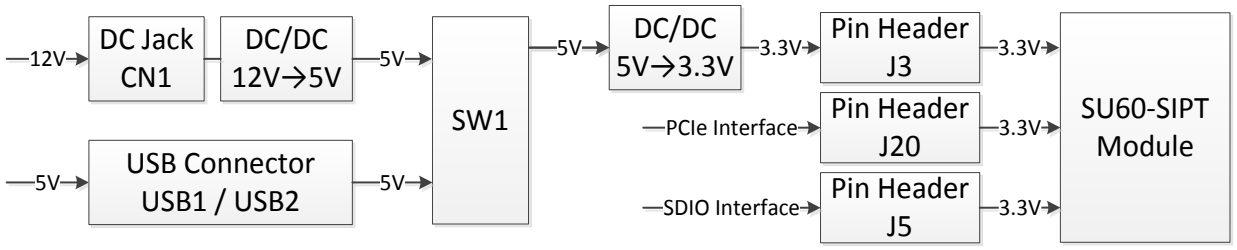


Figure 3: DVK-SU60-SIPT power supply

The development board can be powered from DC 12V supply (into DC jack connector CN1), USB (type micro-B) connector (USB1 and USB2), or the host interface (PCIe or SDIO interface). The power source fed into DC jack is regulated down to 5V with an on-board regulator and wire to SW1.

The 5V from the USB or the DC jack is regulated down to 3.3V with an on-board regulator on the development board. Switch SW1 selects between the regulated 5V and USB. The voltage from host interface (PCIe or SDIO interface) is not regulated but is fed directly to SU60-SIPT module supply pin.

The default position of SW2 is to select regulated 5V.

The development board has a 1.8 V regulator for the VCCIO of FTDI-Chip.

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

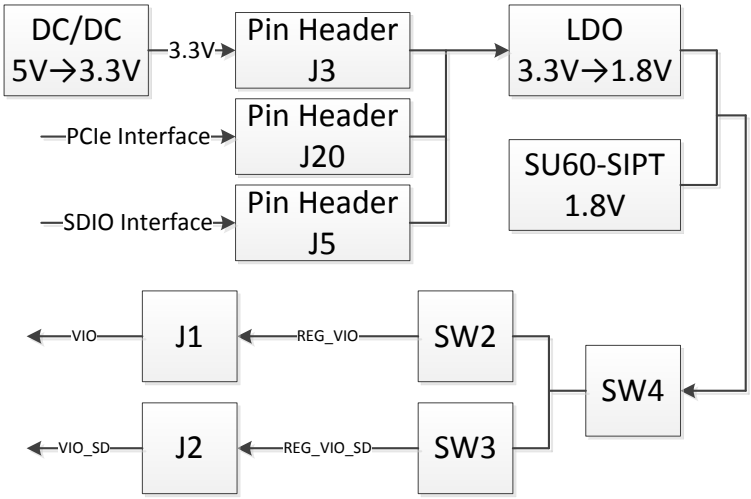


Figure 4: DVK-SU60-2230C 1.8V power supply

On the development board, the power domain:

3V3 supplies the SU60-SIPT module only
The header connectors (J3, J20, J5) can be used to measure the current of power domain 3V3
REG_1V8 supplies the FTDI chip IO, VIO and VIO_SD

3.3 Host Configuration

The development board have three slide switches (SW5, SW6, SW7) for bootstrap configuration. To view its location, refer to Table 3.

Table 3: Bootstrap configuration

Strap Value SW7, SW6, SW5 CON[0], CON[1], CON[2]	WLAN	BT
000	SDIO	UART
001	SDIO	SDIO
010	PCIe	USB 2.0
011	PCIe	UART
101	USB 2.0	USB 2.0

3.4 Tact Switch

The development board have three tact switches (SW8, SW9) for optional. To view its location, refer to Figure 1.

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

3.4.1 PDn (SW9)

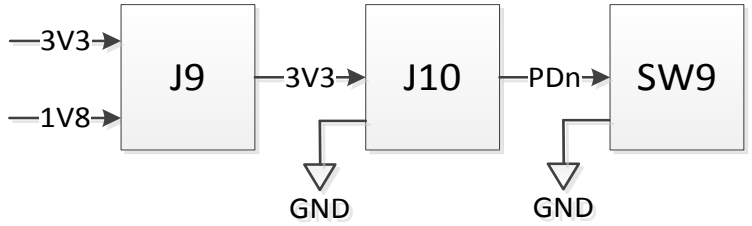


Figure 5: DVK-SU60-2230C PDn power supply

Full Power-Down (Input) (Active Low)

0 – Full power-down mode

1 – Normal mode

PDn can accept an input either 1.8V or 3.3V .
PDn may be driven by the host
PDn must be high for normal operation

There is an internal pull-up resistor on this pin.

3.4.2 PMU_EN (SW8)

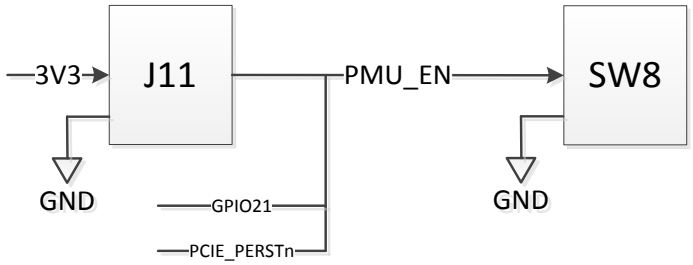


Figure 6: DVK-SU60-2230C PMU_EN power supply

Enable input for internal PMU (Input) (Active Low).

0 – Disable the input for internal PMU.

1 – Normal mode
PMU_EN can accept an input of 3.3V.
PMU_EN may be driven by the host
PMU_EN must be high for normal operation

There is an internal pull-up resister on this pin.

Note: PDn and PMU_EN are also wired to TP1 and TP2 for optional. To view its location, refer to Figure 1.

3.5 4-wire UART Serial Interface

The development board provides access to the SU60-SIPT module 4-wire UART interface (TX, RX, CTS, RTS) either through USB (via U7 FTDI USB-UART convertor chip) or through a breakout header connector J15, J16, J17, and J18. Refer to Figure 1.

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

Note: SU60-SIPT module provides 4-wire UART interface on the HW.

For 3.3V VIO, V_{IH} is from 2.31V to 3.7V; V_{IL} is from -0.4V to 0.99V.

For 1.8V VIO, V_{IH} is from 1.26V to 2.2V; V_{IL} is from -0.4V to 0.54V.

3.5.1 UART Mapping

UART connection on the SU60-SIPT module and FTDI IC are shown in table below. Refer to Figure 1 to see how the SU60-SIPT module UART is mapped to the breakout header connector (J15, J16, J17 and J18).

Table 4: UART mapping

SU60-SIPT Default function	FTDI IC UART
UART_RXD (output)	TXD
UART_TXD (input)	RXD
UART_CTSn (output)	RTS
UART_RTSn (input)	CTS

3.5.2 UART Interface Driven by USB

USB Connector – The development kit provides a USB Type micro-B connector (USB2) which allows connection to any USB host device. The connector optionally supplies power to the development kit and the USB signals are connected to a USB to serial convertor device (FT232R).

USB to UART – The development kit is fitted with a (U6) FTDI FT232R USB to UART converter which provides USB-to-Virtual COM port on any Windows PC (XP or later). Upon connection, Windows auto-installs the required drivers. For more details and driver downloads, visit http://www.ftdichip.com/Products/FT232R.htm.

UART interface driven by USB FTDI chip – In normal operation, the SU60-SIPT module UART interface is driven by the FTDI FT232R USB to UART converter.

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

3.5.3 UART Interface Driven by External Source

UART interface driven by external UART source – The SU60-SIPT module UART interface (TX, RX, CTS, RTS) is presented at a 2.54 mm (0.1”) pitch headers (J15, J16, J17, and J18). To allow the SU60-SIPT UART interface to be driven from the breakout header connector (J15, J16, J17, and J18):

– The development board must be powered from DC jack (CON5) and switch SW1 must be in position *DC JACK 5V*.

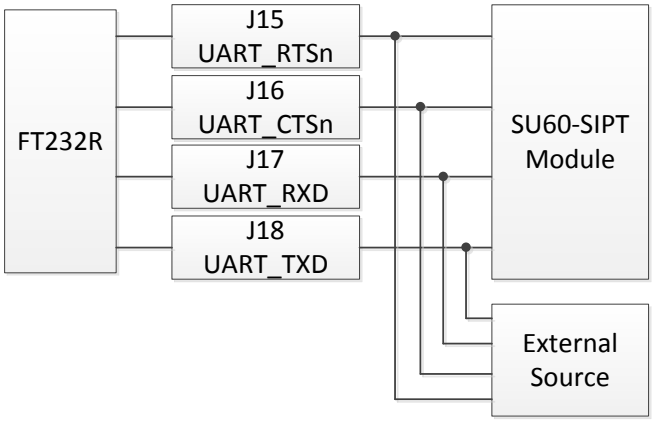


Figure 6: USB to UART Interface and Header to UART interface

3.6 32.768KHz Oscillator

The development kit is fitted with a (U5) 32.768KHz oscillator which provides sleep clock to SU60-SIPT module. Fit a jumper on J14 to disable the sleep clock, if necessary.

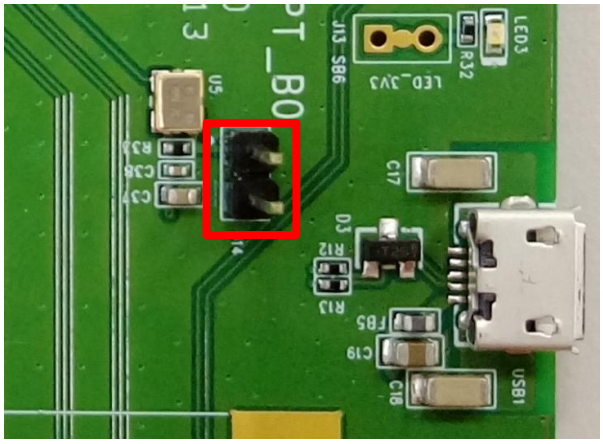


Figure 7: Pin Header J14

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

3.7 PCM

The development kit provides the PCM signal on J7.

The pin descriptions of J20 for PCM signal are shown in below table.

Table 5: PCM signal pins

J20	Description
Pin 1	GND
Pin 2	PCM_IN
Pin 3	PCM_OUT
Pin 4	PCM_BCLK
Pin 5	PCM_SYNC
Pin 6	GND

Note: For 3.3V VIO, V_{IH} is from 2.31V to 3.7V; V_{IL} is from -0.4V to 0.99V.

For 1.8V VIO, V_{IH} is from 1.26V to 2.2V; V_{IL} is from -0.4V to 0.54V.

3.8 LTE Coexistence

The development kit provides the LTE coexistence and JTAG signal on J6.

The pin descriptions of J6 are shown in below table.

Table 6: LTE coexistence pins

J21	Description
Pin 1	GND
Pin 2	LTE_SOUT
Pin 3	LTE_SIN
Pin 4	JTAG_TMS
Pin 5	JTAG_TCK
Pin 6	GND

Note: For 3.3V VIO, V_{IH} is from 2.31V to 3.7V; V_{IL} is from -0.4V to 0.99V.

For 1.8V VIO, V_{IH} is from 1.26V to 2.2V; V_{IL} is from -0.4V to 0.54V

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

3.9 GPIOs

The development kit provides GPIO signal wire to J8.

Table 7: GPIO pins

J8	Description
Pin 1	GPIO0
Pin 2	GPIO2
Pin 3	GPIO3
Pin 4	GPIO21
Pin 5	GPIO22
Pin 6	GND

Note: For 3.3V VIO, V_{IH} is from 2.31V to 3.7V; V_{IL} is from -0.4V to 0.99V.

For 1.8V VIO, V_{IH} is from 1.26V to 2.2V; V_{IL} is from -0.4V to 0.54V

3.10 LED Indicator

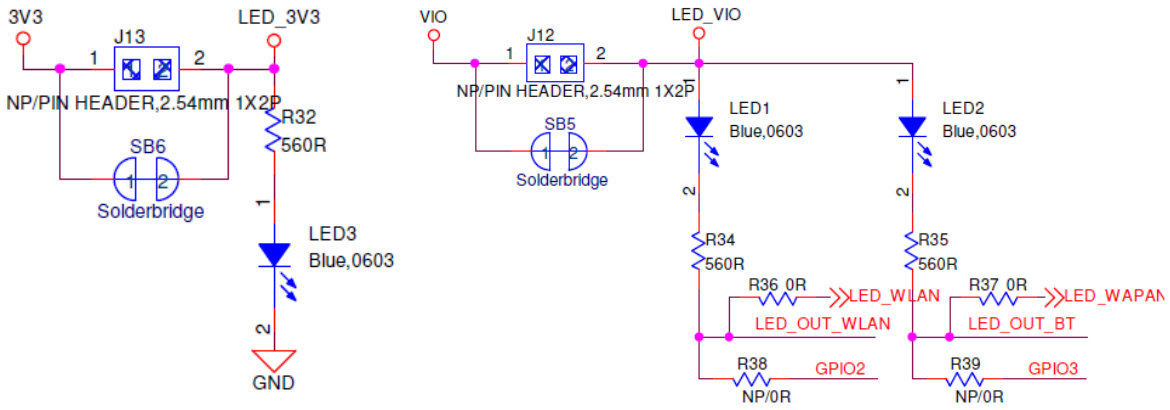


Table 8: LED pins

LEDs	Description
LED1	WLAN status (Active Low)
LED2	BT status (Active Low)
LED3	3.3V Module Power

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

3.11 U.FL Connector

The development kit provides U.FL connectors for RF measurement.

Table 9: U.FL connectors

U.FL	Description
CON3	ANT0 (Wi-Fi)
CON1	ANT1 (Wi-Fi + BT)

4 Additional Documentation

Laird offers a variety of documentation and ancillary information to support our customers through the initial evaluation process and ultimately into mass production. Additional documentation includes:

DVK-SU60-SIPT – User Manual
DVK-SU60-SIPT - Schematics
SU60-SIPT Module – User Manual – Hardware Datasheet and Integration Guide

For any additional questions or queries, or to receive local technical support for this Development Kit or 60 series modules, please contact wirelessinfo@lairdtech.com

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610