UM1922
User manual

VIPower® M0-7 standard high-side drivers hardware design guide

Introduction

VIPower® parallel high-side drivers have reached the 7th generation of smart power drivers (internally called M0-7). In this latest set of drivers all the experience and know-how from existing features of the previous generations as well as new features have been implemented.

The continuous increasing demanding requirements from automotive customers in terms of quality, reliability, flexibility and cost effective system solutions represent the basic factor of new protection feature concept (latch off in overload condition beside the already known auto restart feature) and new diagnostic features like real time device case temperature and battery terminal voltage sensing beside the already existing output current sensing available to the microcontroller in a unique “MultiSense” pin.

Purpose of this user manual is to give a comprehensive “tool kit” for a better understanding of the behavior of the M0-7 parallel High Side Drivers (abbreviation HSDs) in their application usage context and thus allowing the design engineer an easier design in.

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1 General items

1.1 Overview about M0-7 standard high-side drivers

The M0-7 standard high-side drivers are manufactured using STMicroelectronics® proprietary VIPower® technology. The devices are designed to drive 12 V automotive resistive as well as inductive and capacitive loads connected to ground. A 3.3 V and 5 V CMOS-compatible interface to a microcontroller unit is provided. The products feature a very low quiescent current to preserve battery charge during standby mode. Undervoltage shutdown acts below 4 V in order to ensure the loads are driven when charge pump can deliver sufficient power. Overvoltage clamp structure protects the devices effectively from “ISO 7637-2:2004(E)” pulses (with the exception of load dump pulses, unclamped or clamped above 40 V). At loss of ground the outputs are safely turned-off, current injected into the outputs is less than 2 mA. At loss of V_{CC} the outputs are also safely turned-off, but special care must be taken when inductive loads are driven, since additional external protection is required to absorb the demagnetization energy (refer to *Chapter 6: Load compatibility*).

Reverse battery protection is provided in conjunction with external components for monolithic standard high-side drivers, whilst hybrid high-side drivers are reverse battery protected by self turn-on of output channels without the need of external components (refer to *Chapter 2: Reverse battery protection*). Note that no protection features are operating under reverse battery conditions.

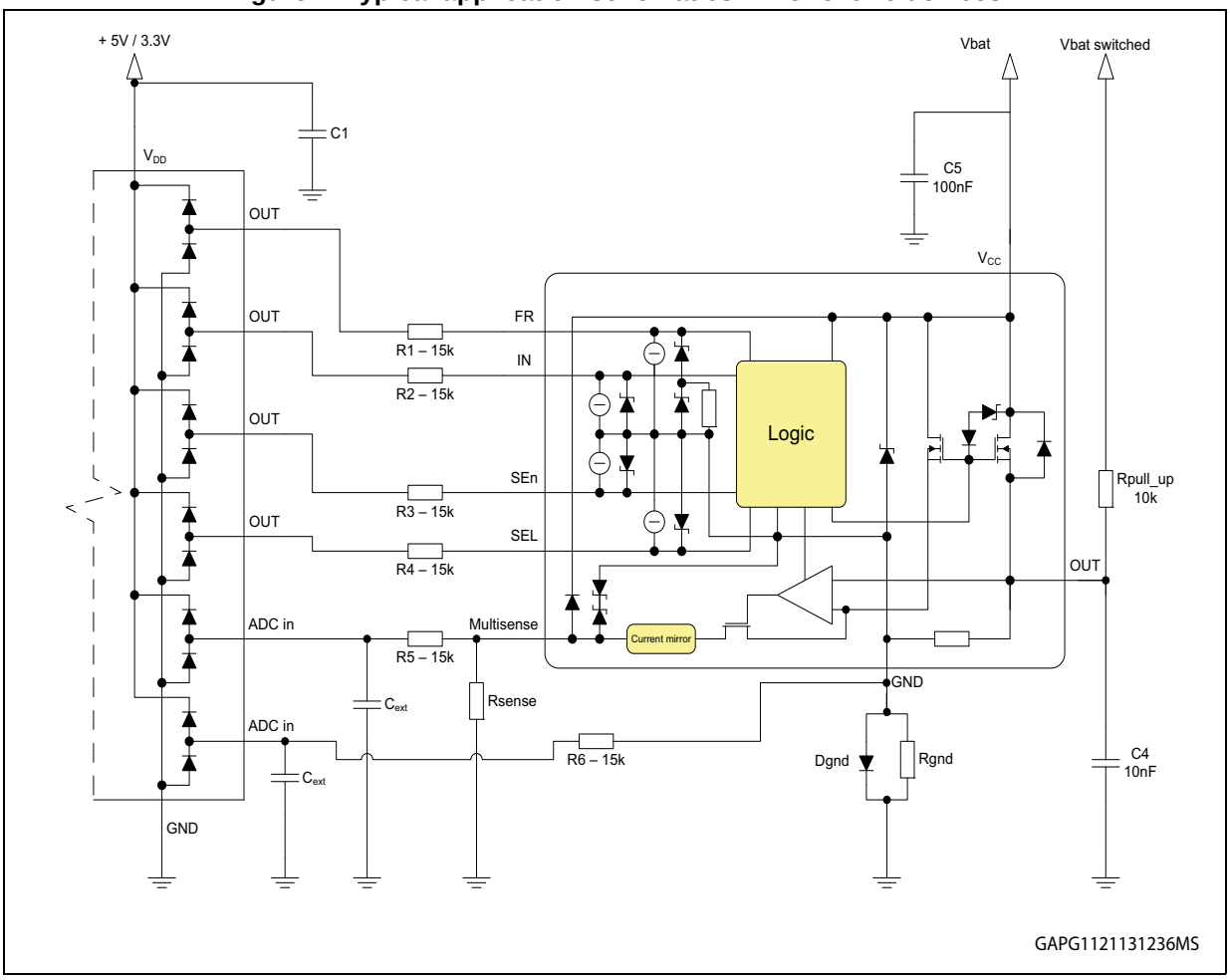
M0-7 standard high-side drivers integrate advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off. A FaultRST pin unlatches the output in case of fault or disables the latch-off functionality. A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including:

- Proportional load current sense
- Supply voltage feedback
- Chip temperature sense
- Detection of overload
- Short circuit to ground
- Short to V_{CC} and
- Off-state open-load

A SenseEnable pin allows off-state diagnosis to be disabled when it is needed to send the module in low power mode. Moreover, thanks to the sense enable functionality, it is possible to share one common external sense resistor among several devices and so to manage a MultiSense diagnostic bus.

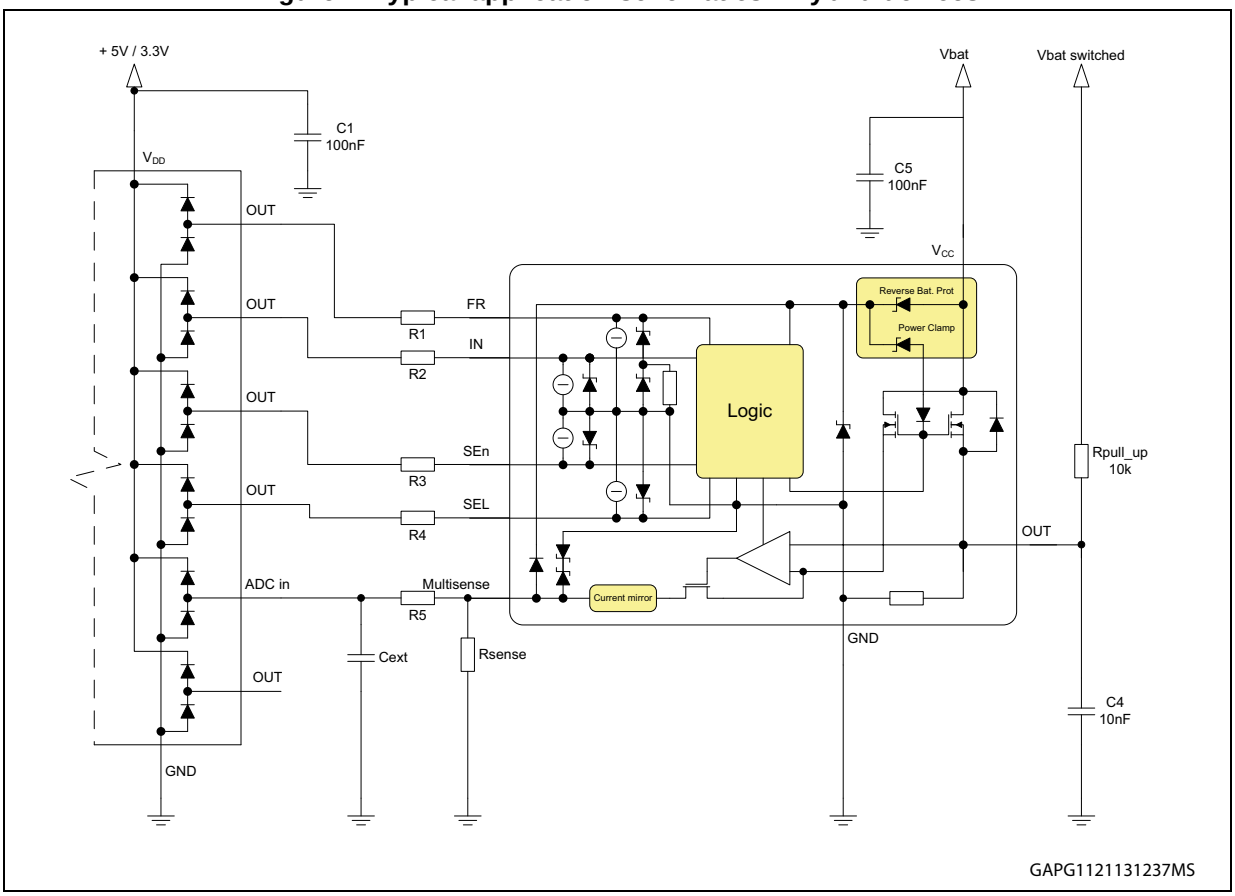
1.2 Application schematics – monolithic devices

Figure 1. Typical application schematics – monolithic devices



1.3 Application schematics – hybrid devices

Figure 2. Typical application schematics – hybrid devices



1.4 Application schematics – description of external components

- Pull-up: this resistor is optional and is needed when open-load in off state diagnostic is required. It has to be dimensioned to pull up the output above the maximum open-load in off state detection voltage (V_{OL} max) and make sure that the output voltage stays below the minimum open-load in off state detection voltage (V_{OL} min) in case the load is connected (for details refer to *Section 7.2.11: Open load detection in off-state*).
- R5//C_{EXT}: a low pass-filter, as an RC filter, can be placed across the R_{SENSE} resistor to suppress HF noise. The time constant of this filter (τ = RC) should be long enough to effectively suppress the noise and short enough to allow MultiSense signal stabilization taking into account multiplexer delay and settling times. C2 should be placed close to the MCU's A/D input. Also, the ground connection for C2 should be at the same potential as the ground of the A/D reference. The filter resistor R5 is also used to limit the A/D's input pin current (for details refer to *Section 7.2.13: MultiSense low pass filtering*).
- R6//C_{EXT}: this low pass-filter and ADC input connection is optional and is recommended for monolithic devices, when a precise chip temperature or supply

voltage feedback reading is required. For dimensioning the same recommendations apply as for R5//C2.

- C4: it is recommended to place a ceramic capacitor on each output to dissipate energy of high frequency, high voltage transients, in particular ESD transient pulses. A 100 V ceramic capacitor generally has sufficient voltage capability. The device ESD robustness of each pin is rated in Absolute Maximum Rating chapter of the datasheet (for details refer to *Chapter 11: Usage in "H-Bridge" configurations*).
- C5: C5 capacitor helps to suppress voltage transients that originate from other actuators connected in parallel and sharing the same battery line. This capacitor will be capable to suppress only low energetic short transient pulses. The device itself is rated to sustain ISO 7637-2:2004(E) transient test pulses 1-4 up to test level IV according to class C. Other methods are needed to protect the module from higher energy transients, such as load dump.

  Moreover C5 capacitor helps to suppress HF noise at the V_{CC} pin that is generated by the high-side driver device itself. The noise can originate from the charge pump circuitry or from the switching slopes of PWMed outputs.

  Using a 100 nF low ESR ceramic capacitor mounted close to device V_{CC} and GND terminals the devices meet CISPR25 Class 5 requirements measured in conducted emission voltage method in DC, as well as in PWM, operation.

  Finally, during a loss of V_{CC} condition, the C5 capacitor supplies load current for the demagnetization of inductive loads.
- R_{SENSE}: R_{SENSE} resistor will convert the MultiSense output current, which is a copy proportional to the load current, into a voltage which can be read by the A/D Converter of the Microcontroller. The R_{SENSE} should be dimensioned to ensure proper resolution range and granularity to monitor nominal current as well as detecting open load or overload events. Typical values of R_{SENSE} are in the range from 1 kΩ to 2.7 kΩ, in order to generate typically 1 V – 2 V sense voltage at nominal load current. R_{SENSE} selection must also take into account maximum power dissipation and maximum current injection during reverse battery conditions and ISO 7637-2:2004(E) and ISO 7637-2:2011(E) pulse 1 transients. Refer to *Section 7.2.6: Considerations on MultiSense resistor choice for current monitor*for details on R_{SENSE} dimensioning rules.
- R1-R5: R1-R5 serial resistors are needed on digital inputs in order to limit the current in the input structures as well as in the microcontroller output structures to a safe value during transient and reverse battery conditions. A proper value for such resistors is 15 kΩ.

  No low ohmic impedance paths to GND such as pull down transistors or capacitors shall be connected directly to the digital inputs. In such conditions, device ground shift may trigger intrinsic parasitic structures and an unlimited, destructive current path from V_{CC} to the digital input will be formed.
- R_{GND}//D_{GND}: a reverse polarity protection network between device ground and module ground is needed for monolithic devices. The diode prevents unlimited destructive current flow through the V_{CC} - GND clamping structure in case of reverse polarity connection. R_{GND} paralleled to D_{GND} avoids device ground dropping to negative voltage during turn-off of inductive loads. Typical values range from 1 kΩ to 4.7 kΩ, higher values reduce power dissipation under reverse battery condition (for details refer to *Chapter 2: Reverse battery protection*).

  Hybrid devices (for classification of Hybrid and Monolithic HSDs please refer to *Section 5.1: Classification of M0-7 HSDs*) do not need GND network (please refer to *Figure 2*) in case pulses belonging to ISO 7637-2:2004(E) standard are requested to be passed. A resistive path in the GND connection of Hybrid devices with R_{GND} > 300,

would not properly activate the self-turn on of the Power MOS in case of reverse battery (the load current would circulate into the Body Diode instead). RON in reverse battery conditions with self-turn on is indicated in the Hybrid devices' datasheets. In case ISO 7637-2:2011(E) is requested to be fulfilled the same schematic applies except in case ISO pulses 1 level IV and 2a level IV are requested to be passed. In this case a GND network must be implemented (for details, please refer to *Section 3.6.2: Dimensioning of the GND network to pass the ISO n.1 and 2a level IV (2011 edition)*).

2 Reverse battery protection

2.1 Introduction

A universal problem in automotive environment is the threat of damage when an end user inverts the battery polarity.

Users of battery powered equipment expect safeguards to prevent damage to the internal electronics in the event of reverse battery installation. These safeguards can be either mechanical (use of special connectors) or electronic. In that case battery powered equipment designers and manufacturers must ensure that any reverse current flow and reverse bias voltage is low enough to prevent damage to the equipment's internal electronics. To provide these electronic safeguards, different concepts applying passive or active reverse polarity protection are possible and described in this chapter.

Depending on the type of device (monolithic or hybrid, for classification please refer to *Section 5.1: Classification of M0-7 HSDs*), a specific protection must be implemented in order not to exceed the device's reverse capability:

- Monolithic HSDs: the reverse battery protection needs to be inserted according to the instructions suggested in this chapter. In particular, if the reverse polarity protection is installed on device GND connection, the device will conduct through the body diode of the power MOSFET with the current limited by the external load. Since no device intrinsic protection schemes are active in reverse condition, special care must be taken on total Power Dissipation.
- Hybrid HSDs: in contrast to monolithic devices, all hybrids VIPower HSD do not need any external components to protect the internal logic in case of a reverse battery condition. The protection is provided by internal structure. Moreover, due to the fact that the output MOSFET turns on even in reverse battery mode and thus providing the same low ohmic path as in regular operation condition, no additional power dissipation has to be considered. Even more: if e.g. a diode without any parallel resistor is connected to GND of a hybrid HSD the output MOSFET is unable to turn on and thus the unique feature of the driver is disabled.

2.2 Reverse battery protection of monolithic HSDs

Reverse battery protection schemes basically can be grouped in the following categories:

- Active or passive reverse polarity protection
- Reverse polarity protection on supply line (V_{CC} terminal) or on GND line (GND terminal)

Table 1. Reverse battery protection concepts

Reverse battery protection concept	Chapter	Active/passive	V_{CC} terminal/ GND terminal	Conduction through output stage
Schottky Diode	*2.2.1*	Passive	V_{CC}	No
Diode || Resistor	*2.2.2*	Passive	GND	Yes
N-channel MOSEFT	*2.2.3*	Active	GND	Yes

Table 1. Reverse battery protection concepts (continued)

Reverse battery protection concept	Chapter	Active/passive	V_{CC} terminal/ GND terminal	Conduction through output stage
p-channel MOSFET	*2.2.4*	Active	V_{CC}	No
Reverse FET	*2.2.5*	Active	V_{CC}	No

2.2.1 Schottky diode

When the battery is installed backwards, the Schottky diode is reverse–biased and only the rated leakage current I_R flows. With respect to a standard diode, the Schottky diode has the advantage of a very low voltage drop in forward direction, hence power dissipation is reduced. However, the disadvantage of using a Schottky diode is, that it is typically more expensive than a standard diode.

Below reported, there is the suggested procedure to choose properly the right device. The following parameters will constitute the selection criteria:

- The average current used by the device, electronic module, load to be reverse battery protected. Failure scenarios, such as an output shorted to GND (load short circuit) have to be considered as well.
- The maximum repetitive peak reverses voltage V_{RRM}
- The maximum ambient temperature T_{amb}

The following inequality must apply in all cases:

$$T_{amb} + R_{th} \cdot P < T_{jMAX}$$

where:

$$P = V_{TO} \cdot I_{F(AV)} + rd \cdot I^2_{F(RMS)}$$

$I_{F(AV)}$ = maximum average forward current

$I_{F(RMS)}$ = RMS forward current

R_{th} = thermal resistance (Junction to ambient) for the device and mounting in use

rd = small signal diode resistance

V_{TO} are depending on the special characteristics of the diode.

One important thing to take into account is the peak reverse voltage limit of the Schottky diode: V_{RRM} = 100 V seems a good compromise with respect to the “ISO 7637-2:2004(E)” pulse 1 Test levels IV. In case compliance with “ISO 7637-2:2011(E)” pulse 1 Test level IV is required, V_{RRM} must be ≥ 150 V. The main drawback of this method is the power dissipation in the Schottky diode in forward direction. Depending on the type of package, the R_{th} and the ambient temperature, the maximum affordable power dissipation in the Schottky diode is typically in the range of 1 W. In consequence the maximum average forward current is limited to the range of 1 A – 2 A.

The direct diode reverse battery protection can also be replaced with a simple fuse. However, upon battery inversion this fuse will blow and the module will need to be replaced or repaired.

2.2.2 Diode + resistor in GND line

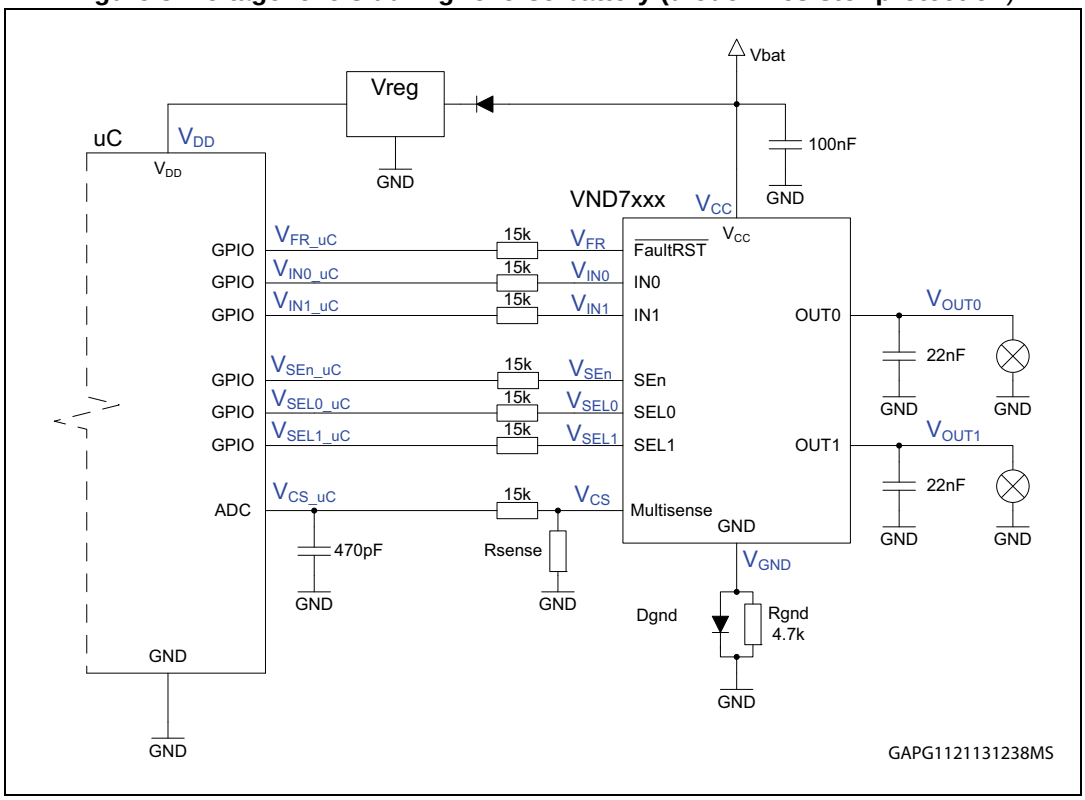
The reverse battery protection is applied to the GND terminal of the driver. This kind of protection leaves the output power stage in reverse battery condition conductive through its body diode. The current is limited by the external load. Since no thermal protection works in reverse condition, special attention must be paid to the total power dissipation in the device. During the reverse battery event, the peak junction temperature shall remain safely below the maximum allowed junction temperature (T_{TSD_max}). Considering a voltage drop on the internal body diode of V_{F_max} = 0.7 V, the resulting power dissipation in the high-side driver per output channel is P_D = 0.7 V * I_{LOAD}. Z_{thj-a} diagrams reported in HSD datasheets support the user to calculate the maximum affordable load current for a given PCB layout.

Note that the intrinsic diode between MultiSense pin and V_{CC} pin will be forward biased in reverse battery condition. The current is limited by the external sense resistor. A 1 kΩ sense resistor will dissipate 250 mW about.

For what concerns the GND path of the device, the integrated V_{CC} - GND clamping protection, which circuit behaves like a Zener diode will be forward biased in reverse battery condition. The power dissipation in the GND resistor therefore is determined by $P_D = (-V_{BAT\_rev} - 0.3\ V)^2 / R_{GND}$. A 1 kΩ GND resistor will dissipate 250 mW about.

The following figure provides an overview about the resulting voltage levels on pins in a typical application schematic during reverse battery condition.

Figure 3. Voltage levels during reverse battery (diode + resistor protection)



Out = 5 W bulb

Out 0, 1 = 5 W bulb

Table 2. Reverse battery-voltages on pins (VND7040AJ)

Pin voltages [V] VND7xxxAJ		Pin voltages [V] microcontroller	
V_{CC}	-16	V_{DD}	-0.4
V_{FR}	-9.7	$V_{FR\_\mu C}$	-0.7
V_{IN0}	-10	$V_{IN0\_\mu C}$	-0.7
V_{IN1}	-10	$V_{IN1\_\mu C}$	-0.7
V_{SEn}	-10	$V_{SEn\_\mu C}$	-0.7
V_{SEL0}	-10	$V_{SEL0\_\mu C}$	-0.7
V_{SEL1}	-10	$V_{SEL1\_\mu C}$	-0.7
V_{CS}	-15.3	$V_{CS\_\mu C}$	-0.7
V_{OUT0}	-15.3		
V_{OUT1}	-15.3		
V_{GND}	-15.4		

GND voltage on device is dropping to the reverse battery voltage plus the forward voltage of the integrated V_{CC} to GND clamping circuit. Voltage on MultiSense pin is dropping to the reverse battery voltage plus the forward voltage across the internal ESD protection diode. The maximum allowed DC output current on MultiSense pin (I_{SENSE}) in reverse battery conditions is limited to 20 mA. Therefore the Sense Resistor R_{SENSE} must be chosen accordingly:

$$R_{SENSE} > (|V_{BAT\_reverse} - 0.7V|) / 0.02A = 765\Omega$$

For generic R_{SENSE} dimensioning rules, please refer to *Chapter 7: MultiSense - analogue current sense* .

Due to the clamping voltage of the integrated ESD protection diodes on logic pins (FaultRST, IN_x, SEL_x, SE_n) the voltage on those pins is dropping to -10 V about. Therefore a serial resistor is needed to limit the current and protect the I/O structure on microcontroller port pins and the high-side driver´s logic pins.

Furthermore the ground network shall ensure the device will work properly when driving inductive loads and/or is not being damaged when submitted to ISO 7637-2:2011(E) pulse 1 test level IV pulses.

The diode at the GND terminal blocks the current through the forward biased internal substrate diode of the HSD during reverse battery condition.

A resistor connected in parallel to the diode is recommended in case the device drives a high inductive load with a demagnetization time longer than t_{D_STBY} (delay time for the device to reach standby mode after the last logic pin (IN_x, $\overline{FaultRST}$, SE_n and SEL_x) is set low). The purpose of this resistor is to suppress a negative voltage on the GND pin during the standby mode if the demagnetization phase is still ongoing. Without this resistor, the low supply current in standby mode (I_{soff} = 0.5 µA max at 85 °C) allows the GND pin to be pulled negative by the demagnetization voltage on the output (~ (V_{CC} - V_{CLAMP}) ~ (13.5 V – 46 V) = -32.5 V) via an internal pull-down resistor (~90 kΩ) on the output (see *Figure 4*). If the negative ground shift exceeds the input high level threshold, the device leaves the standby mode and tends to turn on. The GND pin is immediately pulled high

(~ 600 mV) by the increased supply current I_{SON} so that the standby mode will be activated again after t_{D_STBY}. As a result, we could see short negative peaks on the GND pin with period of t_{D_STBY} during the whole demagnetization phase. These peaks are not long enough to activate the HSD output, which means the device works safely even without the GND resistor. However, this resistor is still needed in order to suppress the described parasitic oscillations (if $T_{DEMAG} > t_{D\_STBY}$).

The ground network can be safely shared amongst several different high-side drivers, provided they are supplied from the same supply rail. Sharing the ground network is even possible among different HSDs, when they are supplied from different supply rails. In this case however, special precautionary measures must be applied (for details refer to *Section 8.3: Paralleling of GND protection network*). The presence of the ground network will produce a shift (~ 600 mV) in the input threshold. This shift will not vary, if more than one HSD share the same diode/resistor. The diode at the GND terminal allows the high-side driver to clamp positive ISO pulses above 46 V (the typical clamping voltage of the HSD). Negative ISO pulses still pass GND and logic terminals. The diode should withstand clamped ISO currents in case of positive ISO pulses and reverse voltages in case of negative ISO pulses.

Dimensioning of the GND diode

The most severe positive “ISO 7637-2:2004(E)” pulse we have to consider is test pulse 2a at level IV (50 V during 50 µs). This voltage is considered on top of the nominal supply voltage of 13.5 V – so the total voltage is 63.5 V. The M0-7 HSDs have a clamping voltage V_{CLAMP} = 46 V typical. In case of a typical device the remaining voltage is 63.5 V - 46 V - 0.7 V = 16.8 V. The ISO pulse generator output impedance is 2 Ω. With this the resulting peak current through the diode is 8.4 A for duration of 50 µs.

The most severe negative “ISO 7637-2:2004(E)” pulse we have to consider is test pulse 1 at level IV (-100 V at 1 ms). This pulse is directly transferred to the GND pin via the internal clamping. So, the maximum peak reverse voltage of the diode should be at least 100 V. In case “ISO 7637-2:2011(E)” pulse 1 test level IV compliance is required, the maximum peak reverse voltage of the diode should be at least 150 V.

Note: The Diode will work in avalanche mode if the pulse level is above the rated reverse voltage.

Conclusion:

The dimensioning the GND diode must fulfill the following:

- Maximum peak forward current: 8.4 A for 50 µs for ISO 7637-2:2004(E)
- Maximum reverse voltage: -100 V for ISO 7637-2:2004(E) resp. -150 V for ISO 7637-2:2011(E)

Note: As seen from above explanation, the HSD with a diode protection at the GND pin doesn’t clamp negative ISO pulses on the supply line. Therefore an appropriate serial protection resistor should be used between microcontroller and HSD (typically 15 kΩ). The resistor value should be calculated according to the maximum injected current to I/O pin of the used microcontroller and to the maximum Input sink current of the HSD.

Diode parameters can be lower if an external clamping circuitry is used (e.g. HSD module is supplied from a protected power supply line).

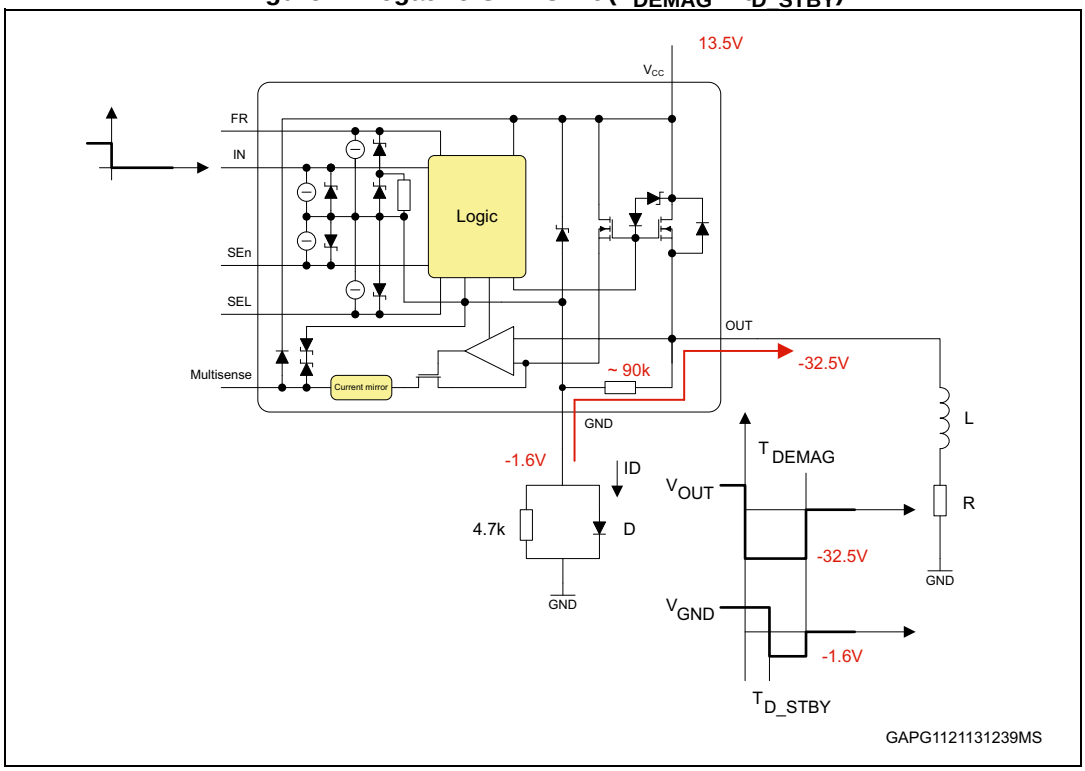
Dimensioning of the GND resistor

The GND resistor is recommended in case of a high inductive load. To determine if the resistor is needed or not, we need to know the demagnetization time (T_{DEMAG}). The resistor is recommended if T_{DEMAG} is higher than the standby delay time (t_{D_STBY}).

A typical t_{D_STBY} value of 350 µs is considered in this comparison.

T_{DEMAG} can be determined by either measurement (*Figure 6*, R_{GND} = 4.7 kΩ, Load: Relay 270 mH/ 90 Ω alternatively Bulb on a typical wire harness with 6 µH stray inductance) or calculation, using *Equation 1* and *Equation 2*.

Figure 4. Negative GND shift (T_{DEMAG} > t_{D_STBY})



Equation 1

$$V_{DEMAG} = V_{BAT} - V_{CLAMP}$$

Equation 2

$$T_{DEMAG} = \frac{L}{R} \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right)$$

Figure 5. GND resistor requirements (inductive load)–test setup

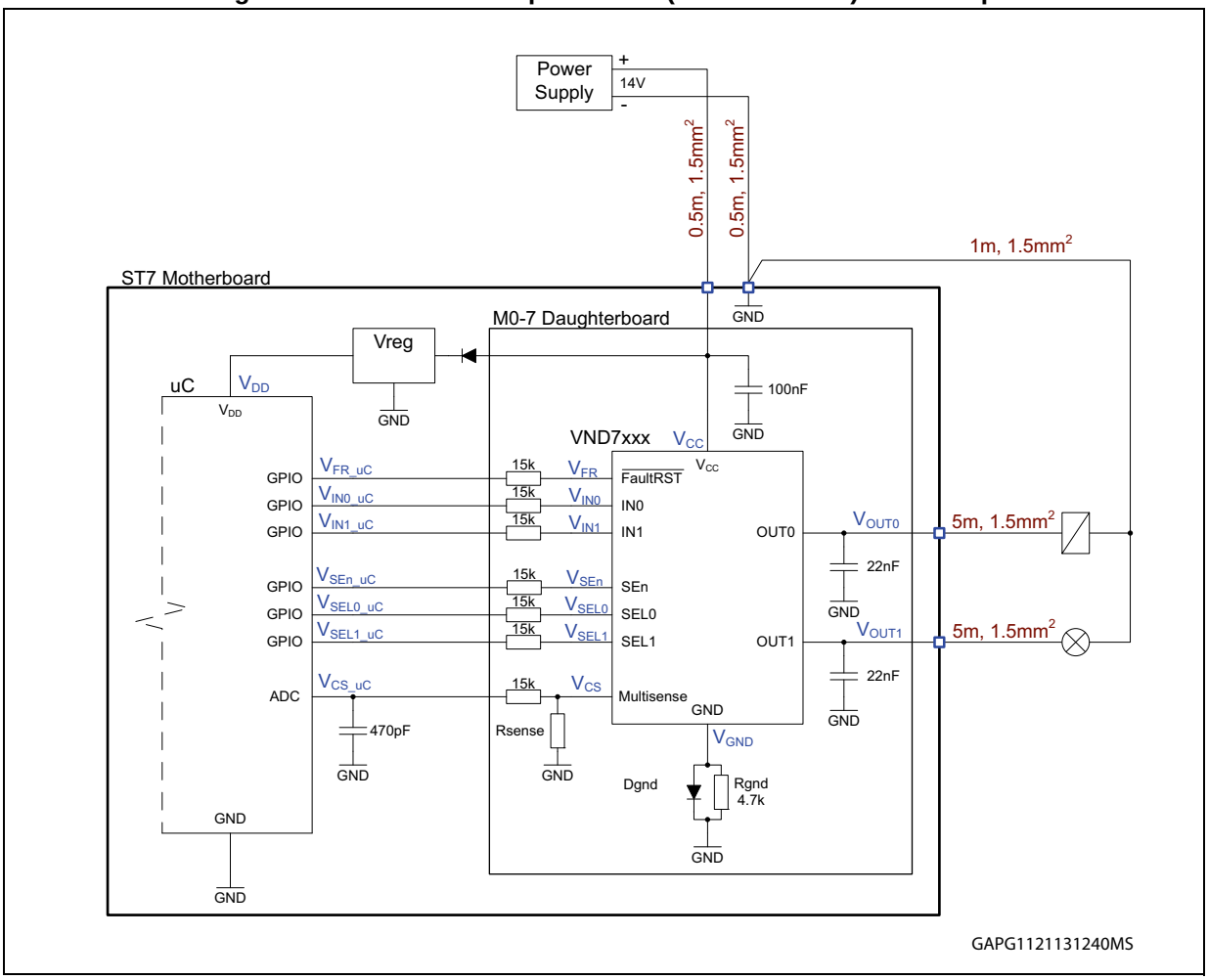


Figure 6. Measurement example (t_{DEMAG} > t_{D_STBY}) without GND resistor

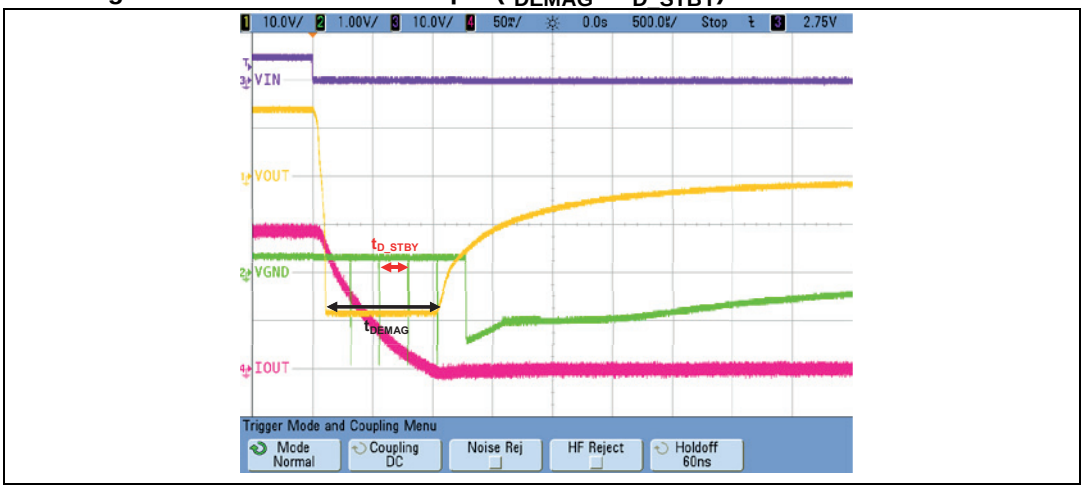


Figure 7. Measurement example (t_{DEMAG} > t_{D_STBY}) with 4.7 kΩ GND resistor

The experimental trials have shown:

- The operation with high inductivity load (T_{DEMAG} > t_{D_STBY}) is correct even without the GND resistor (only the diode), knowing that the device GND pin oscillation with period of t_{D_STBY} may be present (see *Figure 6*)
- In all cases, the 10 kΩ resistor was enough to reduce the GND shift below the logic input activation level (so eliminate the oscillations)
- The 4.7 kΩ appears to be the best compromise between the GND shift safety and power dissipation during static reverse battery condition (~50 mW)

The value of the resistor should be low enough to be sure that the negative voltage at the GND pin is suppressed as much as necessary to keep the device off. This means the V_{GND} should be kept above -1.3 V.

The minimum resistor value is determined by the maximum DC reverse ground pin current of the HSD in reverse battery condition:

$$R_{GND} \geq \frac{V_{BAT(reverse)}}{I_{GND(reverse)max}} = \frac{16V}{200mA} = 80\Omega$$

In order to keep the power dissipation on the resistor during reverse battery condition as low as possible, it is recommended to select the resistor value close to the maximum value (4.7 k).

Summary – dimensioning of the resistor

Resistor recommended if:	$T_{DEMAG} > t_{D\_STBY}$
Resistance:	4.7 kΩ (or lower)
Voltage capability:	min. 150 V (ISO 7637:2-2011(E) pulse 1 at level IV)
	min. 100 V (ISO 7637:2-2004(E) pulse 1 at level IV)
Power dissipation (reverse battery):	min. 50 mW (4.7 kΩ)

Example with relay coil:

In case of a relay coil connected supposing following conditions:

Load resistance:	R_{LOAD} = 90 Ω
Wiring inductances:	L = 270 mH
Initial current I_0:	0.14 A

Applying *Equation 2*, yields a T_{DEMAG} = 1.0 ms > t_{D_STBY}

Example with resistive load with long wire harness:

In case of a resistive load connected via long wires, supposing following conditions:

Load resistance:	R_{LOAD} = 5 Ω
Wiring inductances:	L = 5µH (in case of very long cabling)
Initial current I_0:	2.7 A

Applying *Equation 2*, yields a T_{DEMAG} = 0.4 µs << $t_{D\_STBY\_min}$

Example with short circuit with long wire harness:

In case of a resistive load connected via long wires, supposing following conditions:

Load resistance:	R_{LOAD} = 100 Ω
Wiring inductances:	L = 5 µH (in case of very long cabling)
Initial current I_0:	130 A (I_{LIMH_max} - lowest ohmic monolithic HSD VN7010AJ)

Applying *Equation 2*, yields a T_{DEMAG} = 18µs << $t_{D\_STBY\_min}$

This demagnetization phase lasts very short time in comparison to the standby delay time so, in case of not highly inductive loads, no GND resistor is needed in parallel to the GND diode.

2.2.3 N-channel MOSFET in GND line

In comparison to the solutions described in the previous chapters, reverse polarity protection with MOSFETs offer two main advantages: lower power losses and minimal voltage drop. Generally the MOSFET´s body diode is oriented in the direction of normal current flow. When the battery is installed incorrectly, the N-MOS (P-MOS) FET's gate voltage is low (high), preventing it from turning ON.

When the battery is properly installed and the portable equipment is powered, the N-MOS (P-MOS) FET's gate voltage is taken high (low) and its channel shorts out the diode.

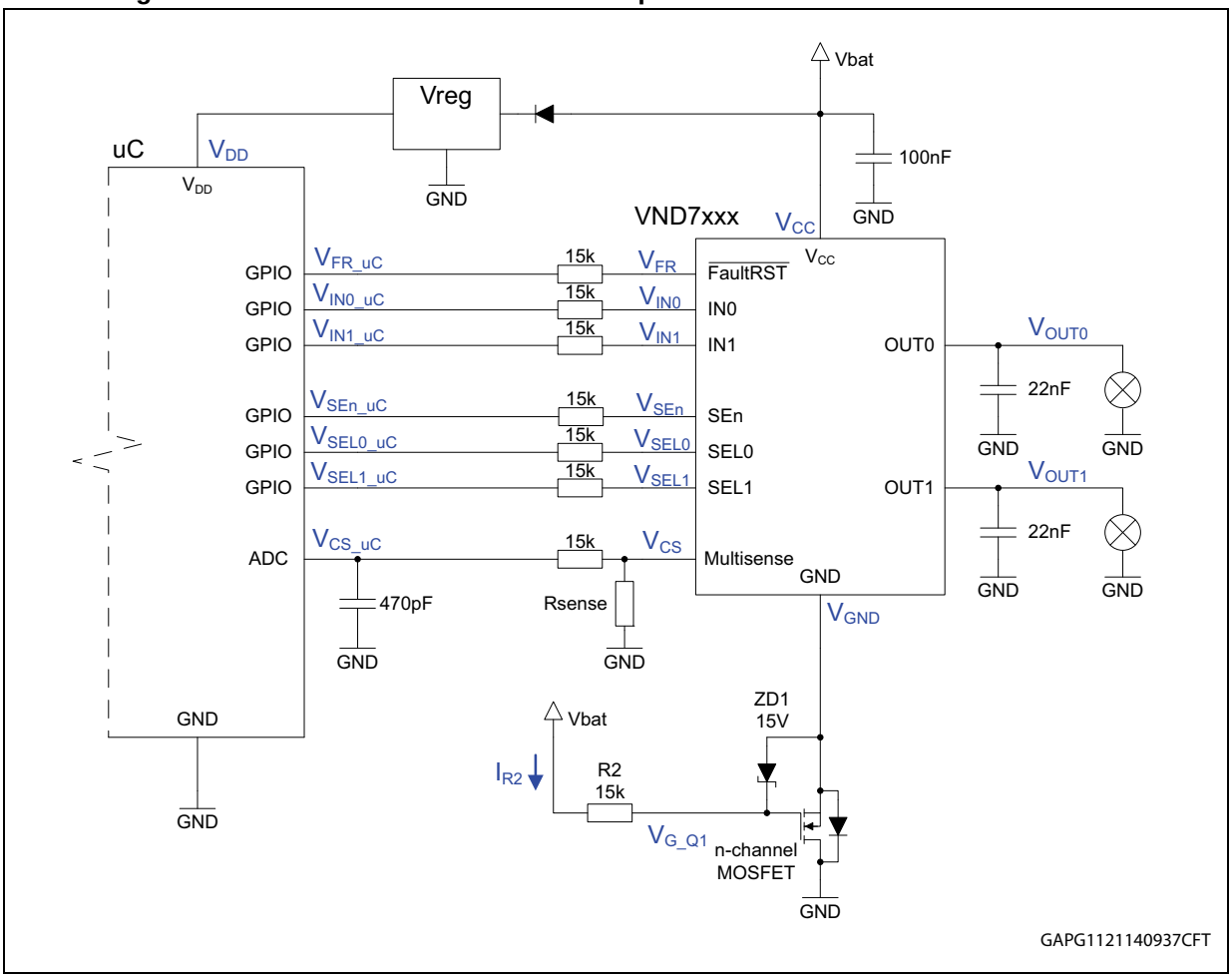
A voltage drop of $R_{DS(on)} \times I_{SON}$ is seen in the ground return path when using the N-MOS FET. A voltage drop of $R_{DS(on)} \times I_{LOAD}$ is seen in the power path when using the PMOS FET. In the past, the primary disadvantage of these circuits has been the high cost of low $R_{DS(on)}$, low-threshold voltage FETs. However, advances in semiconductor processing have resulted in FETs that provide minimal drops in small packages.

The N-channel MOSFET is connected in such a way, that its gate is driven directly by the battery voltage and its drain is connected to ground. In normal condition it is ON whilst a reverse battery event switches it OFF (because $V_{GS} \leq 0$) and protects the HSD.

In *Figure 8* is reported a generic schematic with N-channel MOSFET configuration. In this case, like for the solution with Diode || Resistor network in the GND line, the HSD´s output stage body diode is forward biased and therefore is conducting during the reverse battery. The current is limited by the external load. Since no thermal protection works in reverse condition, special care must be taken on the total power dissipation in the device. During the reverse battery event, the peak junction temperature shall remain safely below the maximum allowed junction temperature (T_{TSD_max}). Considering a voltage drop on the internal body diode of $V_{F\_max} = 0.7$ V, the resulting power dissipation in the HSD per output channel is $P_D = 0.7\ V \cdot I_{LOAD}$.

$Z_{thj\text{-}a}$ diagrams reported in HSD datasheets help the user to calculate the maximum affordable load current for a given PCB layout.

Figure 8. Generic schematic and test setup with N-channel MOSFET in GND line



Measured values (VND7020AJ)

Table 3. Static reverse battery - voltages on pins

	Reverse battery (V_{CC} = -16 V)	Normal operation (standby mode)	Normal operation (out0=on, out1 = off)	Normal operation (out0=on, out1 = on)
V_{CC} [V]	-15.99	14	13.97	13.95
V_{GND} [V]	-15.37	0	0.000028	0.000042
V_{G_Q1} [V]	-15.92	13.97	13.95	13.94
I_{R2} [µA]	-4.1	0.2	0.2	0.2

Table 3 reports the measurement results on VND7020AJ test vehicle: GND voltage on device is dropping to the reverse battery voltage plus the forward voltage of the integrated V_{CC} to GND clamping circuit (substrate diode). Voltage on MultiSense pin is dropping to the reverse battery voltage plus the forward voltage across the internal ESD protection diode. The maximum allowed DC output current on MultiSense pin (I_{SENSE}) in reverse battery conditions is limited to 20 mA. Therefore the sense resistor R_{SENSE} must be chosen accordingly:

$R_{SENSE} > (|V_{BAT\_reverse} – 0.7\ V|) / 0.02\ A = 765\ \Omega$

For generic R_{SENSE} dimensioning rules, please refer to *Chapter 7: MultiSense - analogue current sense* .

Due to the clamping voltage of the integrated ESD protection diodes on logic pins (FaultRST, IN_x, SEL_x, SE_n) the voltage on those pins is dropping to -10 V about. Therefore a serial resistor is needed to limit the current and protect the I/O structure on microcontroller port pins and the high-side driver´s logic pins. The gate voltage of the N-channel MOSFET is pulled down to the reverse battery voltage, ensuring the MOSFET is fully off. In normal operation only the leakage current of ZD1 Zener diode is flowing through R2 to GND. In order to minimize this current even at higher supply voltages, a diode with higher Zener voltage (i.e. 18 V) might be chosen. The Zener voltage should be anyway always lower than the maximum rated Gate Source Voltage V_{GS} of the N-channel MOSFET.

The resistor R2 limits the current through the Zener diode at supply voltages higher than the Zener voltage and limits the charging/discharging current of the gate. In addition the resistor R2 together with the gate capacitance of the N-channel MOSFET determines the turn-off time when exposed to fast negative transients or abrupt reverse polarity according to the LV 124: 2009-10 standard. 15 kΩ as demonstrated by the experiment reported below appears to be a good compromise between minimizing the charging/discharging current and ensuring a fast turn-off time.

A capacitor might be placed between Gate and Source of the N-channel MOSFET. The RC filter composed by R2 and C can be dimensioned to be transparent against the fast negative pulses ISO 7637-2:2004(E) pulse 1 test level IV, keeping the reverse polarity protection circuitry switched on. The usage of such capacitor C is not recommended, when the system must be compliant to ISO 7637-2:2011(E) pulse 1 test level IV. In this case in fact it is needed that the pulse does not discharge through the HSD and the conducting N-channel MOSFET as this might be destructive for the HSD.

Figure 9. MOSFET solution in GND – experiment VND7020AJ, ISOpulse 1 (-150V, 90 Ω)

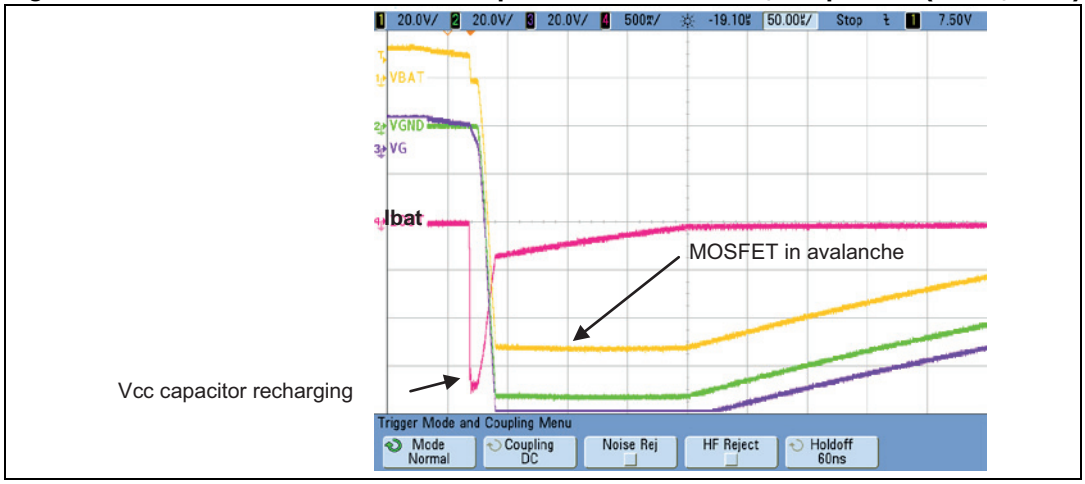


Figure 9 shows the example of a 100 V/100 mΩ N-channel MOSFET in the schematics, as for *Figure 8*, submitted to ISO 7637:2-2011(E) pulse 1 transients. In order to limit the current in this experiment a 90 Ω generator resistor was chosen. As long as the N-channel MOSFET is still conducting during the negative pulse, the voltage on V_{CC} pin (V_{BAT}) is clamped to minus one diode voltage due to the forward biased substrate diode of the HSD. The N-channel MOSFET is turned off once the GND voltage begins to drop. This happens within a few microseconds. The first current spike is due to the recharging of the V_{CC}

capacitor. As soon as the GND voltage drops to -100 V, the N-channel MOSFET starts to conduct in avalanche until the pulse amplitude drops below its breakdown voltage BV_{DSS} = 100 V.

The breakdown voltage BV_{DSS} of the N-channel MOSFET either should be higher than the maximum negative transient peak voltage of ISO 7637:2-2011(E) or the energy capability of the N-channel MOSFET in avalanche must be high enough to sustain the transient pulse energy.

Figure 10. Reverse battery test VN7016AJ (13.5 V → -4 V, 82 mΩ, R2 = 15 kΩ) as per LV 124: 2009-10 standard

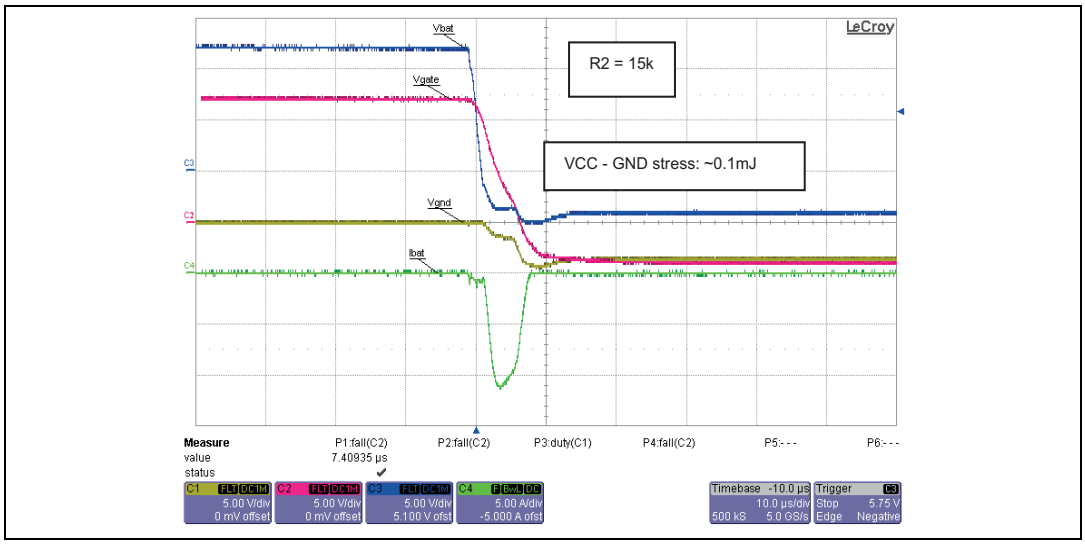


Figure 10 shows an example of an abrupt reverse battery test changing the polarity of the battery supply from 13.5 V to -4 V within a few µs. The test setup used a 100 V/100 mΩ N-channel MOSFET with a gate resistor R2 = 15 kΩ. The total line impedance is measured with 82 mΩ in line with the requirements of LV 124: 2009-10.

The N-channel MOSFET is able to turn-off within 10 µs about. During this time a relatively high current will flow through the HSD substrate diode. The total energy dissipated in the HSD is around 100 µJ, which is withstood by the M0-7 high-side driver family.

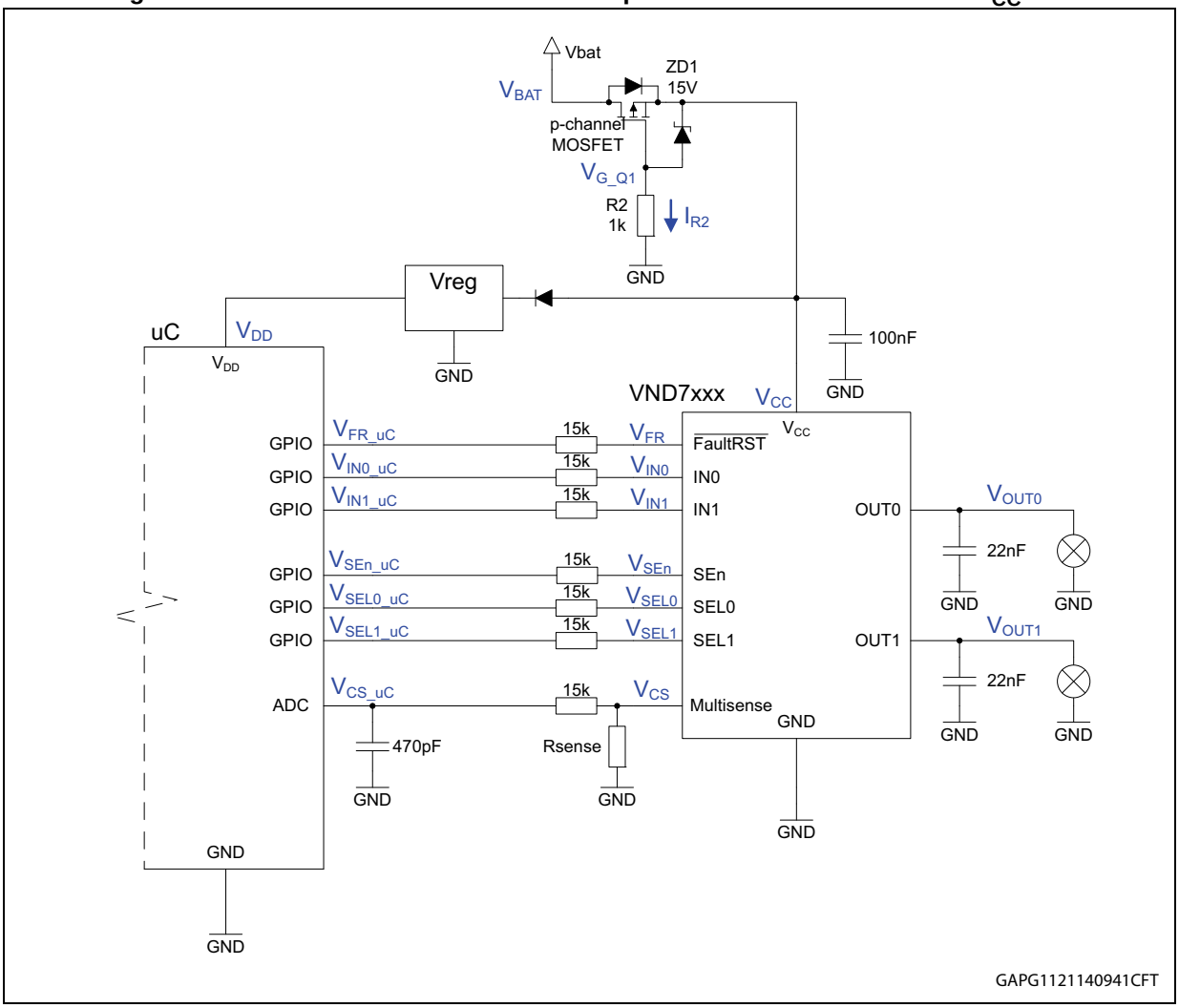
2.2.4 P-channel MOSFET in the V_{CC} line

The P-channel MOSFET is connected in such a way that its Gate is connected to GND via a resistor R2 and its drain to V_{CC} pin, while the source acts as the reverse polarity protected supply. In *Figure 11* is reported a generic schematic with P-channel MOSFET configuration. Compared to an N-channel MOSFET the device will be turned on by applying a negative gate source voltage.

It is important to insert the transistor in the right direction, because the P-channel MOSFET has as well an intrinsic anti parallel body diode which is in forward direction from drain to source.

By referring the gate signal to the ground line, the device is fully turned on when the battery is applied in the right polarity.

Figure 11. Generic schematic and test setup with P-channel MOSFET in V_{CC} line



As soon as the battery voltage is applied and for the first start up, the body diode of the MOSFET will conduct, until the channel is switched on in parallel. The Zener diode will clamp the Gate of the MOSFET to its Zener voltage in case of over voltage on the battery track. In normal operation only the leakage current of ZD1 Zener Diode is flowing through R2 to GND. In order to minimize this current even at higher supply voltages, a diode with higher Zener voltage (i.e. 18 V) might be chosen, however it shall be dimensioned to ensure the Zener voltage is always safely below the maximum rated gate source voltage V_{GS} of the P-channel MOSFET.

The resistor R2 limits the current through the Zener diode at supply voltages higher than the Zener Voltage and limits the charging/discharging current of the gate. In addition the resistor R2 together with the gate capacitance of the P-channel MOSFET determines the turn-off time when exposed to fast negative transients or abrupt reverse polarity according to LV 124: 2009-10 standard. 1 kΩ as demonstrated by the experiment reported below appears to be a good compromise between minimizing the charging/discharging current and ensuring a fast turn-off time. Due to the fact, that the P-channel MOSFET will carry also the load current, it needs to be a lower ohmic component compared to an N-channel reverse polarity protection MOSFET in the GND line. In consequence it will have a higher gate capacitance, hence longer turn-off times for identical gate resistance R2.

Measured values (VND7020AJ)

Table 4. Static reverse battery - voltages on pins

	Reverse battery (V_{BAT} = -16 V)	Normal operation (standby mode)	Normal operation (out0 = on, out1 = off)	Normal operation (out0 = on, out1 = on)
V_{BAT} [V]	-16.02	14.02	14.00	13.98
V_{CC} [V]	0	14.02	13.99	13.97
V_{G_Q1} [V]	0	0	0	0
I_{R2} [µA]	0	0	0	0

Table 4 reports the measurement results on VND7020AJ test vehicle, according to the schematic in *Figure 11*: V_{CC} voltage on device is completely decoupled from the reverse battery voltage. No negative voltage is present on MultiSense and on logic pins. By reverse polarity, the MOSFET will be switched off, because the gate source voltage for this case will be positive $V_{GS} > 0$ (voltage drop over the Zener diode) and protects the HSD.

The same reverse polarity protection network can be shared among several HSD connected to the battery.

A capacitor might be placed between gate and source of the P-channel MOSFET. The RC filter composed by R2 and C can be dimensioned to be transparent against the fast negative pulses ISO 7637-2:2004(E) pulse 1 test level IV, keeping the reverse polarity protection circuitry switched ON. The usage of such capacitor C is not recommended, when the system must be compliant to ISO 7637-2:2011(E) pulse 1 test level IV. In this case in fact it is needed that the pulse does not discharge through the HSD and the conducting P-channel MOSFET as this might be destructive for the HSD.

Figure 12. MOSFET solution in V_{CC} – experiment VND7020AJ, ISOpulse 1 (-100 V, 90 Ω)

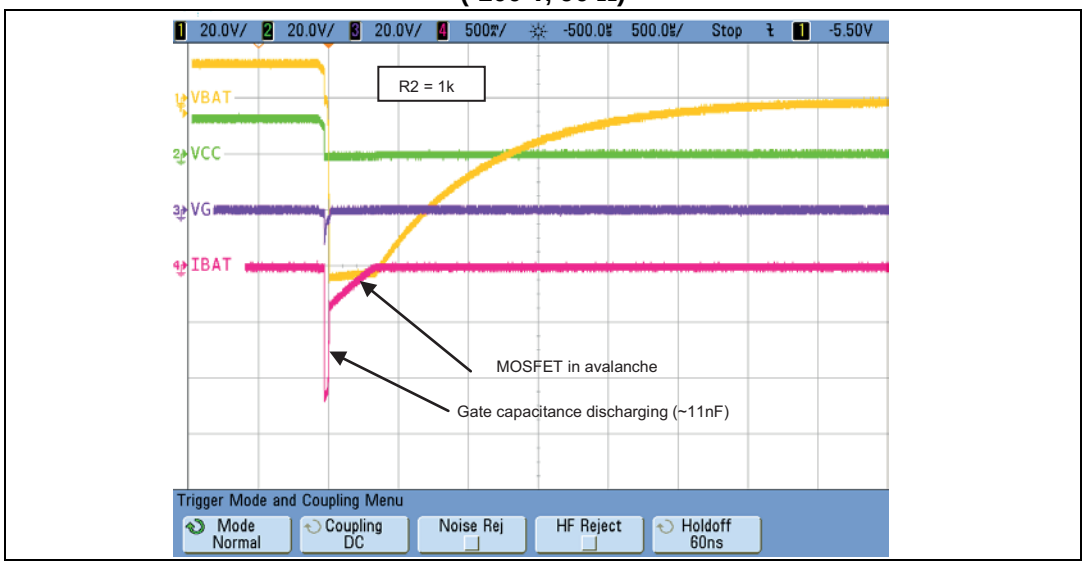


Figure 12 shows the example of a 55 V/16 mΩ P-channel MOSFET in the schematics as per *Figure 11* submitted to ISO 7637:2-2004(E) pulse 1 transients. In order to limit the current in this experiment a 90 Ω generator resistor was chosen. As long as the P-channel

MOSFET is still conducting during the negative pulse, the voltage on V_{CC} pin (V_{BAT}) is clamped to minus one diode voltage due to the forward biased substrate diode of the HSD. The P-channel MOSFET is turned off once the V_{BAT} voltage begins to drop. This happens within few tens of microseconds about. As soon as the V_{BAT} voltage drops to -55 V, the P-channel MOSFET starts to conduct in avalanche until the pulse amplitude drops below its breakdown voltage BV_{DSS} = 55 V.

The breakdown voltage BV_{DSS} of the P-channel MOSFET either should be higher than the maximum negative transient peak voltage of ISO 7637:2-2011(E) or the energy capability of the P-channel MOSFET in avalanche must be high enough to sustain the transient pulse energy.

Figure 13. Reverse battery test according to LV 124:2009-10: VN7016AJ (13.5 V at -4 V, 82 mΩ, R2 = 1kΩ)

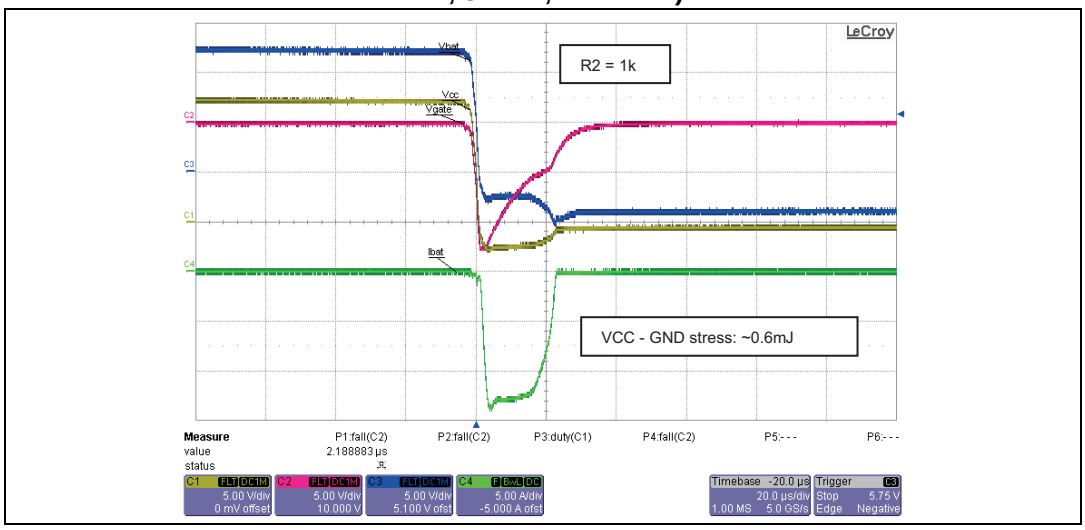


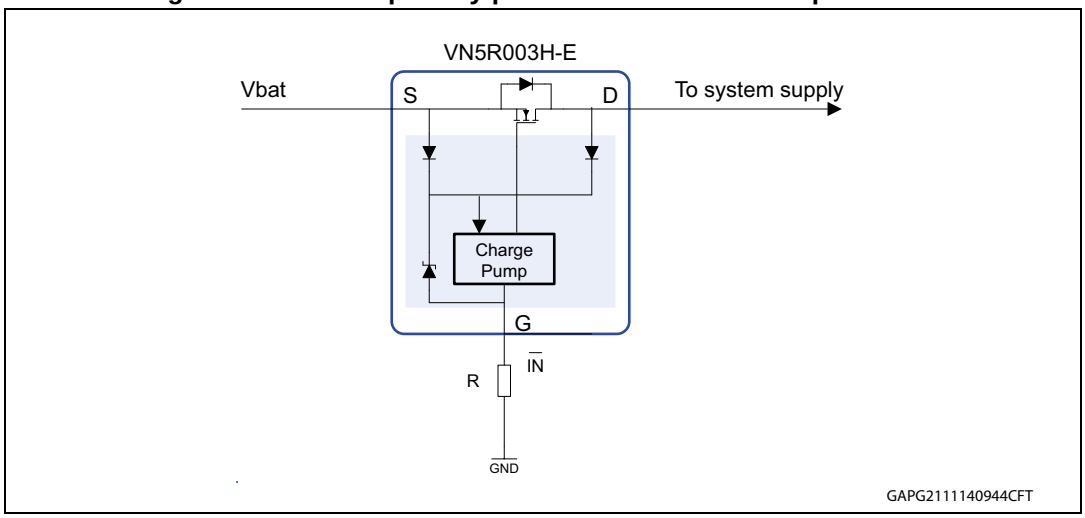
Figure 13 shows the example of an abrupt reverse battery test changing the polarity of the battery supply from 13.5 V to -4 V within a few us. The test setup used a 55 V/16 mΩ P-channel MOSFET with a gate resistor R2 = 1 kΩ. The total line impedance is measured with 82 mΩ in line with the requirements of LV 124:2009-10.

The P-channel MOSFET is able to turn-off within 20 µs about. During this time a relatively high current will flow through the HSD substrate diode. The total energy dissipated in the HSD is around 600 µJ, which is withstood by the M0-7 HSD family.

2.2.5 Dedicated ST Reverse FET solution

The VN5R003H-E is a device made using STMicroelectronics® VIPower® technology. It is intended to provide reverse battery protection to an electronic module. This device, which consists of an N-channel MOSFET and its driver circuit, has two power pins (drain and source) and a control pin, $\overline{IN}$ (see *Figure 14*).

Figure 14. Reverse polarity protection – reverse FET protection



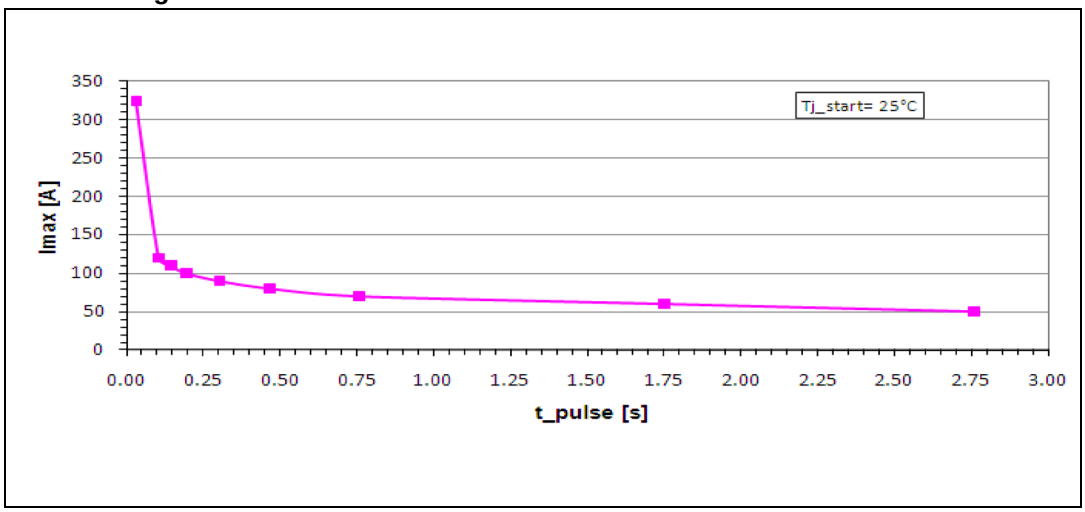
Note that a MOSFET has always an intrinsic anti parallel body diode. If the $\overline{IN}$ voltage versus drain is negative the device is turned ON. The MOSFET is fully turned on when applying the battery voltage and the $\overline{IN}$ pin goes negative versus drain. Due to the fact that the Source is at high potential, the MOSFET is a high-side switch not referring to ground; a charge pump circuit is needed to boost the gate voltage over the source voltage to turn the MOSFET on.

During reverse polarity of the battery, no voltage will supply the gate of the MOSFET which will automatically switch off. When $\overline{IN}$ is left open, device is in OFF state and behaves like a power diode between source and drain pins. The power losses of an N-channel MOSFET for a reverse battery protection are determined by the $R_{DS(on)}$ of the device and the load current. The device is able to withstand an abrupt high load current value, typical of an application where several HSDs are activated simultaneously, and loads like motors or bulbs can have a transient current above the devices' DC Current maximum rating. The diagram reported in *Figure 15* gives information about the safe operating area as well as the maximum pulsed drain current the device is able to manage during normal operation.

The usage of VN5R003H-E for reverse polarity protection is not recommended, when the system must be compliant to ISO 7637-2:2011(E) pulse 1 test level IV. In this case in fact it is needed that the pulse does not discharge through the HSD and the conducting VN5R003H-E device as this might be destructive for the HSD.

The VNR003H-E is robust against "ISO 7637-2 2004 rev E" pulses in the configuration with $\overline{IN}$ pin grounded through a resistance R > 5 Ω.

Figure 15. Maximum current versus duration time of VN5R003H-E



Note: PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 mm, Copper areas: minimum pad lay-out and 2 cm^2.

3 Protection against battery transients

3.1 Introduction on automotive electrical hazards

The automotive environment is the source of many electrical hazards. These hazards, such as electromagnetic interference, electrostatic discharges and other electrical disturbances are generated by various accessories like ignition, relay contacts, alternator, injectors, SMPS (i.e. HID front lights) and other accessories. Because electronic modules are sensitive to electromagnetic disturbances (EMI), electrostatic discharges (ESD) and other electrical disturbances, caution must be taken wherever electronic modules are used in the automotive environment.

These hazards can occur directly in the wiring harness in case of conducted hazards, or be applied indirectly to the electronic modules by radiation. These generated hazards can impact the electronics in two ways - either on the data lines or on the supply rail wires, depending on the environment.

Several standards have been produced to model the electrical hazards that are currently found in automobiles. As a result, manufacturers and suppliers have to consider these standards and have to add protection devices to their modules to fulfill the major obligations imposed by these standards.

The chapter deals with the robustness of M0-L7 monolithic devices submitted to ISO7637-2:2004 and ISO7637-2:2011 disturbances on the battery line and mounted in the typical application scheme.

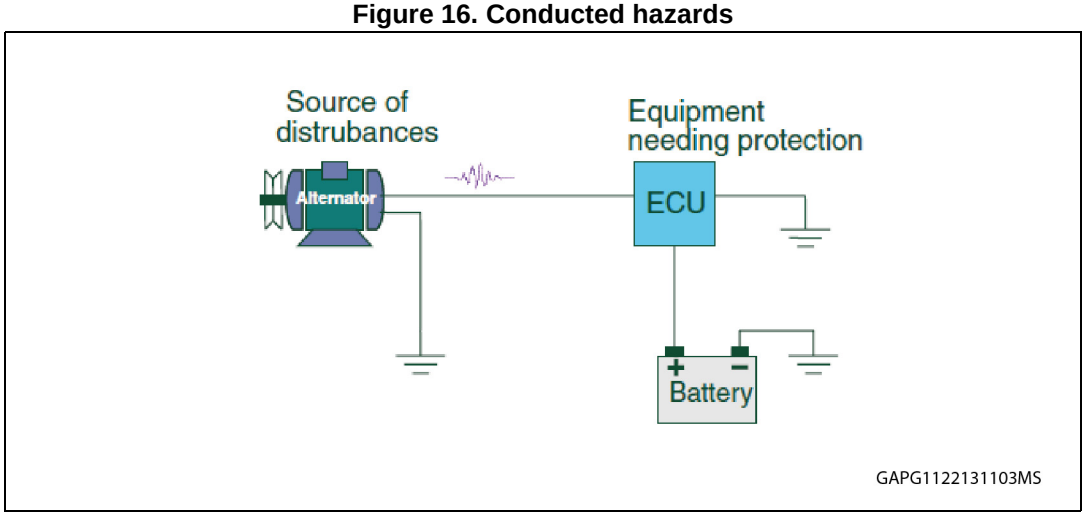
3.2 Source of hazard on automotive

3.2.1 Conducted hazards

These hazards occur directly in the cable harness. They are generated by inductive loads like electro-valves, solenoids, alternators, etc.

The schematic in *Figure 16* is a typical configuration

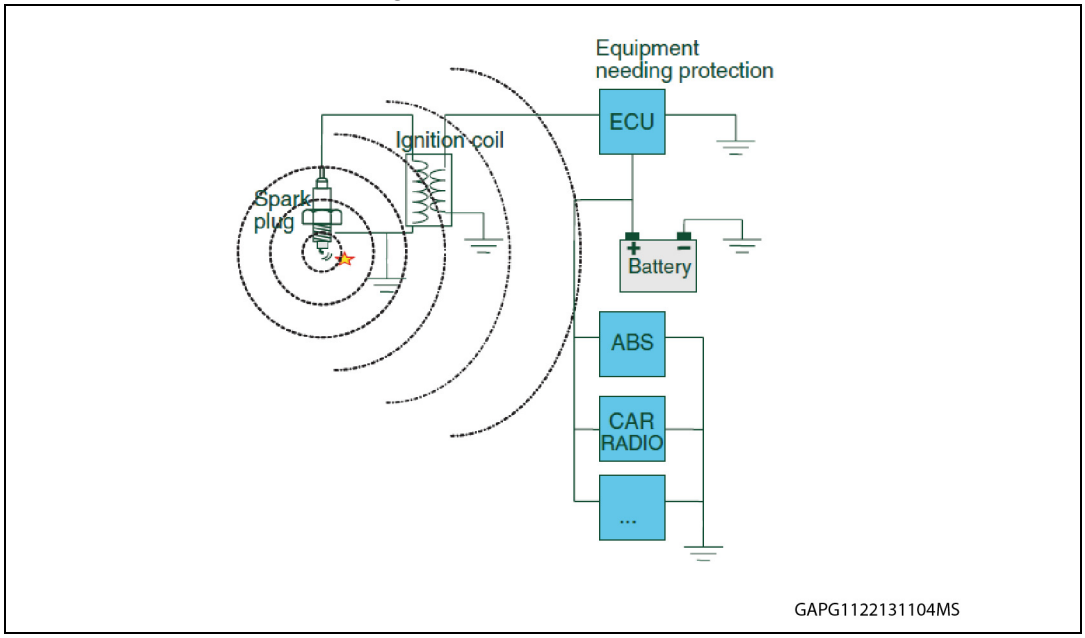
Figure 16. Conducted hazards



These hazards are generated by high current switching like relay contact, high current MOS or IGBT switches, ignition systems, etc. The electromagnetic field generated by these circuits directly affects lines or modules near the source of the electromagnetic radiation.

The schematic diagram in *Figure 17* indicates how electromagnetic radiation creates such hazards as electromagnetic interference in electronic modules**.**

Figure 17. Radiated hazards



3.3 Propagation of electrical hazards on the supply rail

Transients that are generated on the supply rail range mainly concern ISO7637-2 and ISO10605 standards.

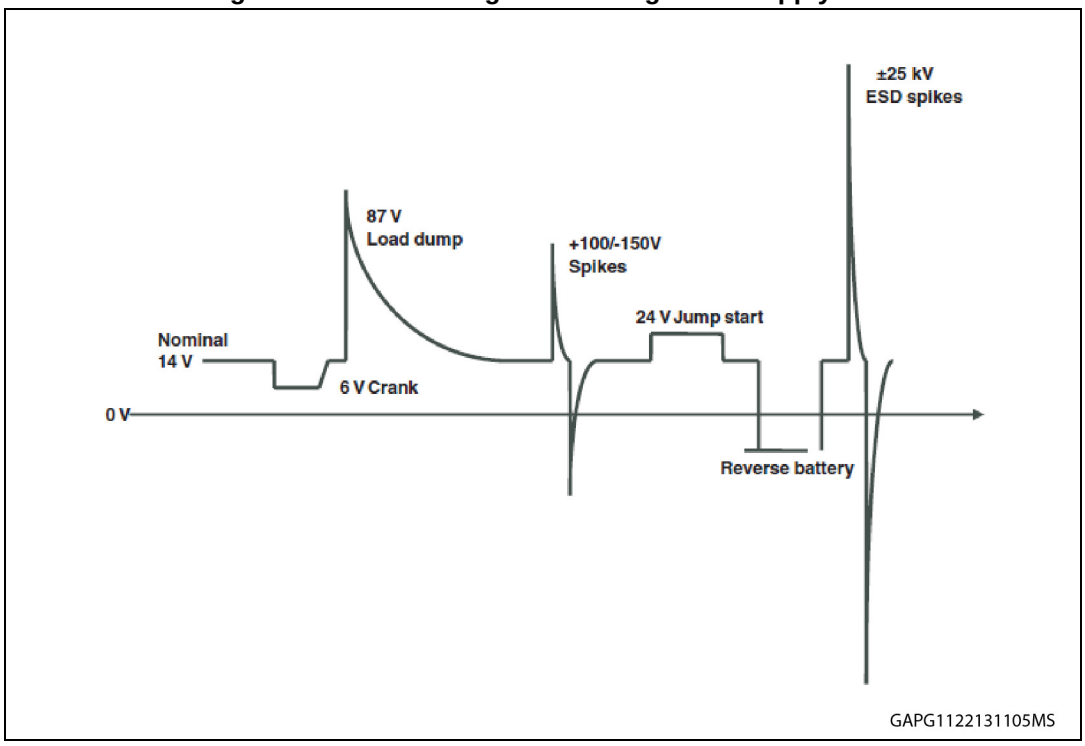
The most energetic transients are those resulting from load-dump and jump start. But all other hazards may affect the normal operation of electronic modules.

The load-dump is caused by the discharged battery being disconnected from the alternator while the alternator is generating charging current. This transient can last 400 ms and the equivalent generator internal resistance is specified as 0.5 Ω minimum to 4 Ω maximum.

According to the ISO 7637-2 standard, the “+100 spikes” are due to supply sudden interruption of currents in a device connected in parallel with the DUT due to the inductance of the wiring harness, while the “-150 V spikes” are due to a supply disconnection from inductive loads.

This chapter deals with voltage transient pulses, detailed on the ISO 7637-2 standard.

Figure 18. Various surges occurring in the supply rail



3.4 Standard for the protection of automotive electronics

All the hazards indicated above are described by several standards bodies such as the Society of Automobile Engineers (SAE), the Automotive Electronic Council (AEC) and the International Standard Organization (ISO).

Since the ISO7637 are the most important automotive standards regarding electrical hazards transient, this document mainly concerns the cases considering such standard:

Below the electrical characteristics of ISO 7637-2 editions 2004 and 2011;

Table 5. ISO 7637-2: 2004 (E)

ISO 7637-2: 2004(E) Test pulse	Test levels		Number of pulses or test times	Burst cycle/pulse repetition time		Delay and impedance
	III	IV		Min.	Max.	
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulses			100 ms, 0.01 Ω
5b	+65 V	+87 V	1 pulses			400 ms, 2 Ω

Table 6. ISO 7637-2: 2011 (E)

Test pulse[1]	Selected test level[2]	Test pulse severity level, U_S[3] [4]			Min. number of pulses or test times	Burst cycle/pulse repetition time	
		IV	III	I/II		Min.	Max.
1		-150 V	-112 V	-75	500 pulses	0.5 s	[5]
2a		+112 V	+55 V	+37	500 pulses	0.2 s	5 s
2b		+10 V	+10 V	+10	10 pulses	0.5 s	5 s
3a		-220 V	-165 V	-112	1 h	90 ms	100 ms
3b		+150	+112 V	+75	1 h	90 ms	100 ms

1. Test pulse as in 5.6 paragraph of ISO 7637-2:2011(E) (see *Appendix A: References*).
2. Values agreed between vehicle manufacturer and equipment supplier.
3. The amplitudes are the values of U_S as defined for each test pulse in 5.6 paragraph of ISO 7637-2:2011(E) (see *Appendix A: References*).
4. The former levels I and II are revised because they did ensure sufficient immunity in subsequent road vehicles' design.
5. The maximum pulse repetition time shall be chosen so that it is the minimum time for the DUT to be correctly initialized before the application of the next pulse and shall be ≥ 0.5 s.

3.5 Basic application schematic to protect a M0-7 standard monolithic high-side driver

The hardware design techniques used for an application will establish the baseline immunity performance. The purpose of hardware techniques is to protect the device from performance degradation or long-term reliability problems.

Below reported, the STM application proposal, for protecting monolithic HSDs under the common stress event mentioned in the ISO 7637-2 editions 2004 and 2011.

To provide these electronic safeguards, manufacturers typically chose either a diode, or resistor or capacitor for protecting both data-line and supply rails.

Components used to suppress or control transients, as well as their implementation details, are described in the next paragraph, providing a basic description of how the most typically used components are employed in low-cost designs for achieving the desired level of transient immunity.

Components used to suppress or control transients can be grouped into two main categories:

- Components that shunt transient currents (voltage limiters)
- Components that block transient currents (current limiters)

Note that depending on the rise time (frequency bandwidth) of the transient, a component may function as either a shunt or a block. For instance, at a slow rise time (low frequency bandwidth) an inductor will have little impedance (a shunt). At faster rise times (higher frequency bandwidth), an inductor will have greater impedance (a block). As a result, transient suppression components must be carefully selected for the optimal operating conditions. The actual performance of the component in the application will depend on the frequency-based characteristics of the component and the board layout.

Resistors

Series resistance between two nodes can provide inexpensive and effective transient protection blocking or limiting transients with frequency-independent resistance. Resistance can be used to create low-pass filters and to decouple power domains. Series resistance is primarily suited to protecting digital or analog signals that carry low currents and can accept a modest voltage drop (across the series resistance).

Capacitors

Capacitors are used in a variety of transient protection roles. They can be used to filter the high frequency pulses produced by an ESD event. They also provide switching current to ICs and serve as energy storage bins that limit voltage variation.

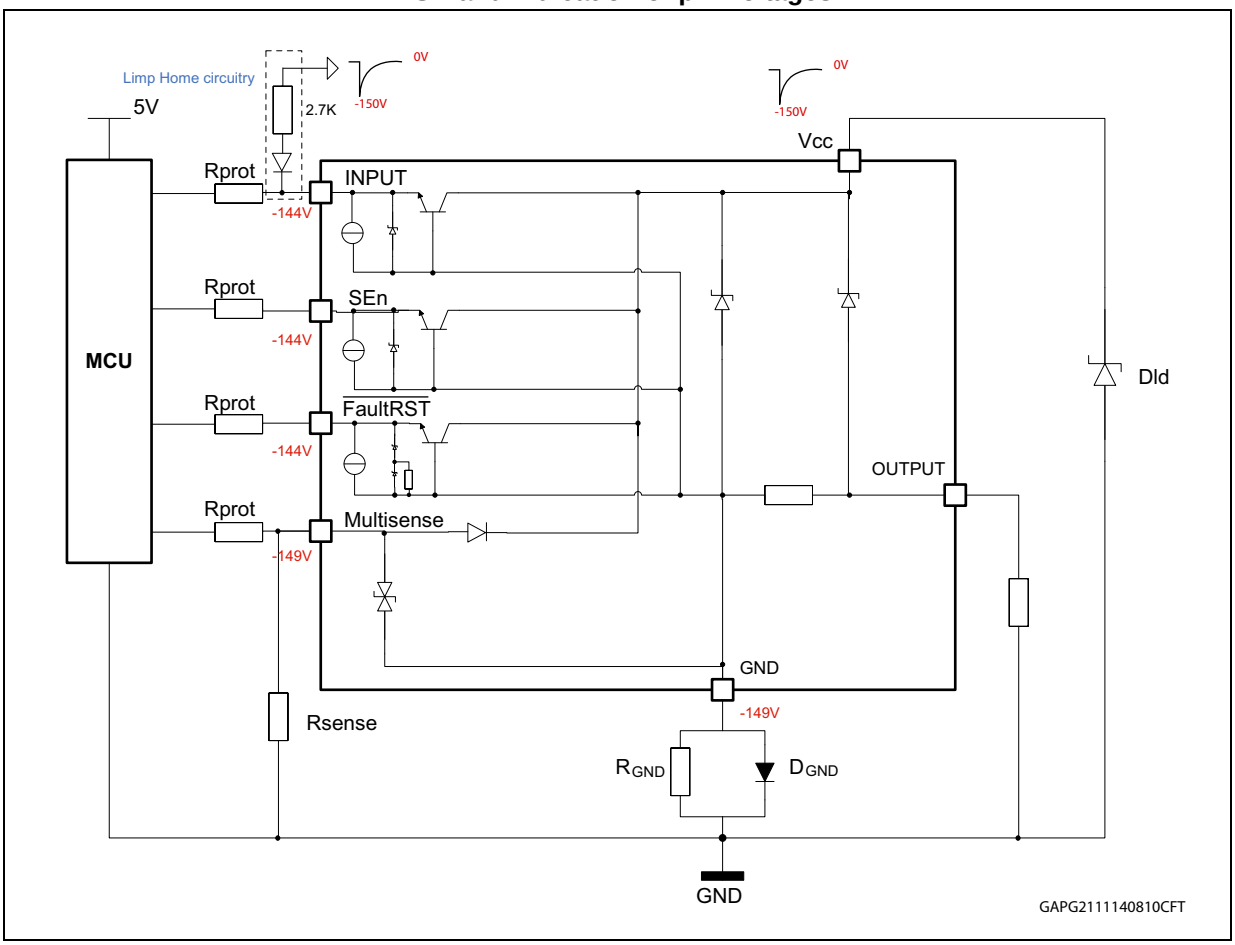
In either role, the capacitor can be used to effectively shunt fast transients of limited energy, such as ESD. Important characteristics to consider, when selecting capacitors, are the maximum DC voltage rating, parasitic inductance, parasitic resistance, and over-voltage failure mechanism.

3.5.1 Components dimensioning

Because the Reverse Battery event, the device needs to be protected by an external diode plus a resistor network (in case of inductive loads) connected in series to the ground pin. In this chapter, the ground network is dimensioned referring to the ISO7637-2 edition 2011 test pulse 1 and 2.

Due to the presence of such protection network, the Negative ISO pulse 1 level IV (-150 V at 1 ms) is directly transferred to the GND pin via the internal clamping. Then, the HSD with a diode protection at the GND pin does not clamp negative ISO pulses on the supply line. Moreover the internal parasitic structures of I/O pins, link these pins directly to V_{BAT} and then to -150 V (see *Figure 19*). Therefore an appropriate serial protection resistor should be used between microcontroller and HSD in order to limit the current injected into these pins.

Figure 19. Internal structures involved during application of ISO 7637-2 pulse 1 in a monolithic HSD and indication of pin voltages



Besides, since the device input may be driven independently of the microcontroller by a separate HW, which is supplied directly from battery, it's mandatory to decouple the signal coming from the microcontroller to the one coming from the limp home circuitry, in order to avoid any backward supply of one circuit versus the other one. The decoupling is ensured by a signal diode, placed in series to the Limp Home path connected to the device input.

Dimensioning of the series resistors on I/O line

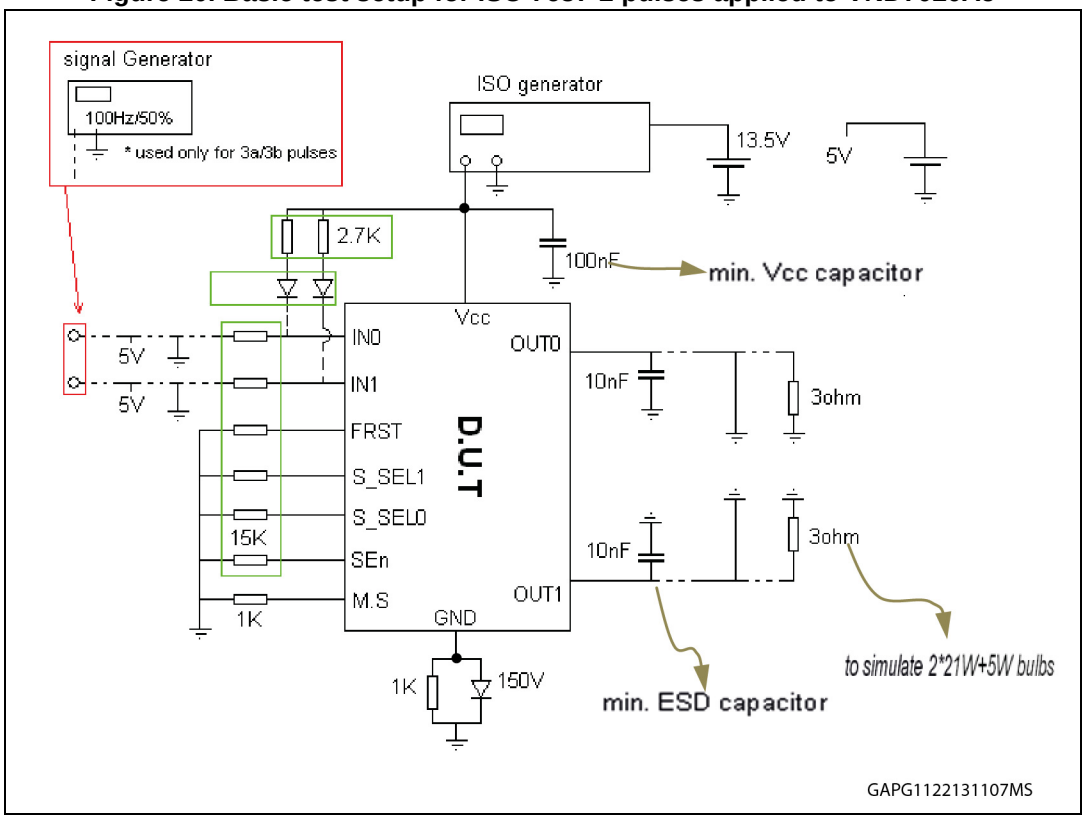
The resistor value should be calculated according to the maximum injected current to I/O pin of the used microcontroller. That value can be assumed about 10 mA so that, the resistors value should be at least 15 kΩ (150 V/10 mA):

$R_i \geq 15\ k\Omega$

The basic application schematic has been validated in order to be reliable with the following stress test, based the ISO7637-2 standard edition 2004 and 2011, in different operative conditions:

- ISO n1 (2 msec/10 Ω, 5 K pulses);
  - Class C must be complied (full operational after each pulse).
- ISO n2a (50 µsec/2 Ω, 5 K pulses);
  - Class C must be complied (full operational after each pulse).
- ISO n3a (0.1 µsec/50 Ω, 1h);
  - Class B must be complied (full operational even during pulses exposure)
- ISO n3b (0.1 µsec/50 Ω, 1h);
  - Class B must be complied (full operational even during pulses exposure)

Figure 20. Basic test setup for ISO 7637-2 pulses applied to VND7020AJ



Below reported the operative conditions (given for VND7020AJ):

- Device in OFF state and output in open load
- Device in OFF state with OUTs in short circuit to GND
- Device in ON state (IN0/IN1 high) and output in open load
- Device in ON state (IN0/IN1 high) driving 3 Ω resistive load on each OUT
- Device in Limp Home state (IN0/IN1 pulled-up by 2.7 kΩ + Diode to V_{CC}) and output in OL.

After test exposure device results are given in the *Table 7* (here the most severe pulses are reported):

Table 7. ISO 7637-2 2004 and 2011 tests and results on monolithic HSDs

ISO 7637-2	TEST PULSE							
	1 Level III	1 Level IV	2a Level III	2a Level IV(1)	3a Level III	3a Level IV	3b Level III	3b Level IV
2004	Class C	Class C	Class C	Class C	Class B	Class B	Class B	Class B
2011	Class C	Class C	Class C	Class C or E(1)	Class B	Class B	Class B	Class B
	Class C: full operational after each pulse Class B: full operational even during pulses exposure Class E: One or more functions of the device do not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device							

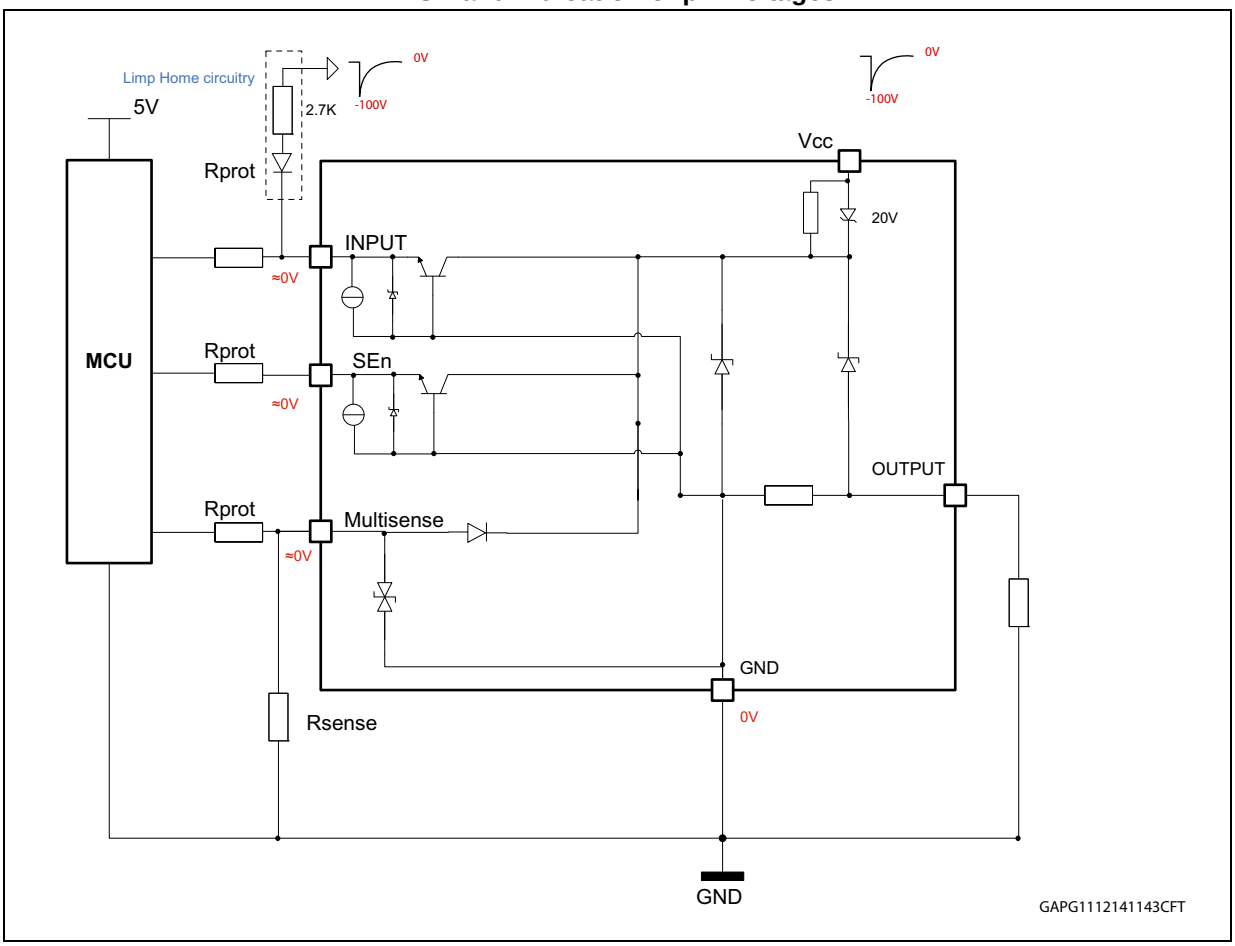
1. The results on pulse ISO7637-2 2011 2a level IV depend mainly on load status and condition (open load, nominal load, shorted load, resistive load, inductive load, capacitive load). Lower ohmic loads with low inductive contribution help to increase the sustainable peak voltage for the device reaching Class C compliance. Tests performed on VND7020AJ, for example, give as result class C in the condition ON state with a resistive load equivalent to the nominal one on each output (see *Figure 20*); instead they give class E with Outputs in open load.

Moreover M0-7 Monolithic HSDs pass the load dump clamped pulse test (class C according to *Table 7* criteria) relevant to the standard ISO-7637-2:2004(E) (5b pulse with 40 V centralized load dump suppressor) as well as the standard ISO 16750-2:2010 (E) (pulse with 35 V centralized load dump suppressor).

3.6 Component dimensioning for hybrid devices

Differently from monolithic devices, the Hybrids do not need the external reverse battery protection network since they have an embedded protection formed by an anti-parallel Zener diode which prevents the signal clamp activation (refer to *Figure 5*). Moreover the reverse battery event enables the self turn-on of output channels. For this reason, during the ISO transients, the parasitic structures of I/O pins are softly triggered with no high current flowing through them. Nevertheless, as precaution, a serial protection resistance is suggested between microcontroller and logic pins to limit the current flowing. Hybrid devices are fully compliant with the tests level specified in the ISO 7637-2: 2004 (see the relevant table for more details).

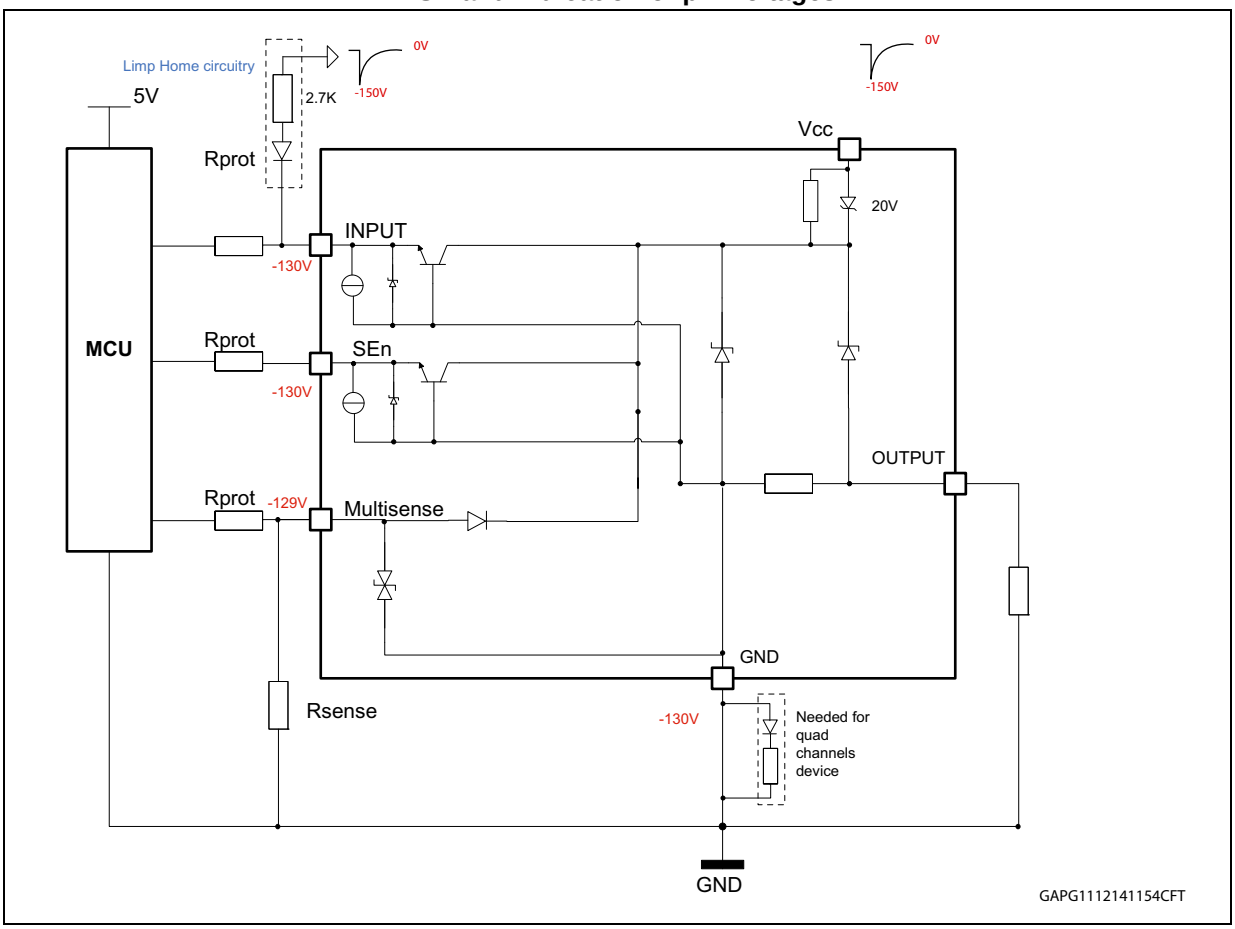
Figure 21. Internal structures involved during application of ISO 7637-2 (2004) pulse 1 in Hybrid HSD and indication of pin voltages



Anyway, to be compliant with the ISO 7637-2 (edition 2011) test pulse 1 level IV and 2a level IV, it is recommended to adopt a GND network in order to limit the current flowing through the internal clamp structure.

Due to the presence of such protection network, the Negative ISO pulse 1 level IV (-150 V for 2 ms) is transferred to the GND pin via the 20 V (typical clamp voltage). Then, logic pins could go down to about -130 V (see *Figure 22*) and this would lead to a triggering of parasitic structures on Signal pins. Therefore a suitable serial protection resistor between microcontroller and HSD is mandatory to limit the current flowing through these pins.

Figure 22. Internal structures involved during application of ISO 7637-2 (2011) pulse 1 in Hybrid HSD and indication of pin voltages



Besides, since the device inputs may be driven independently from the microcontroller by a separate HW (limp home feature), which is supplied directly from battery, it is mandatory to decouple the signal coming from the microcontroller to the one coming from the Limp home Circuitry, in order to avoid any backward supply of one circuit versus the other one. The decoupling is ensured by a signal diode, placed in series to the Limp Home path connected to the device input as shown in *Figure 22*.

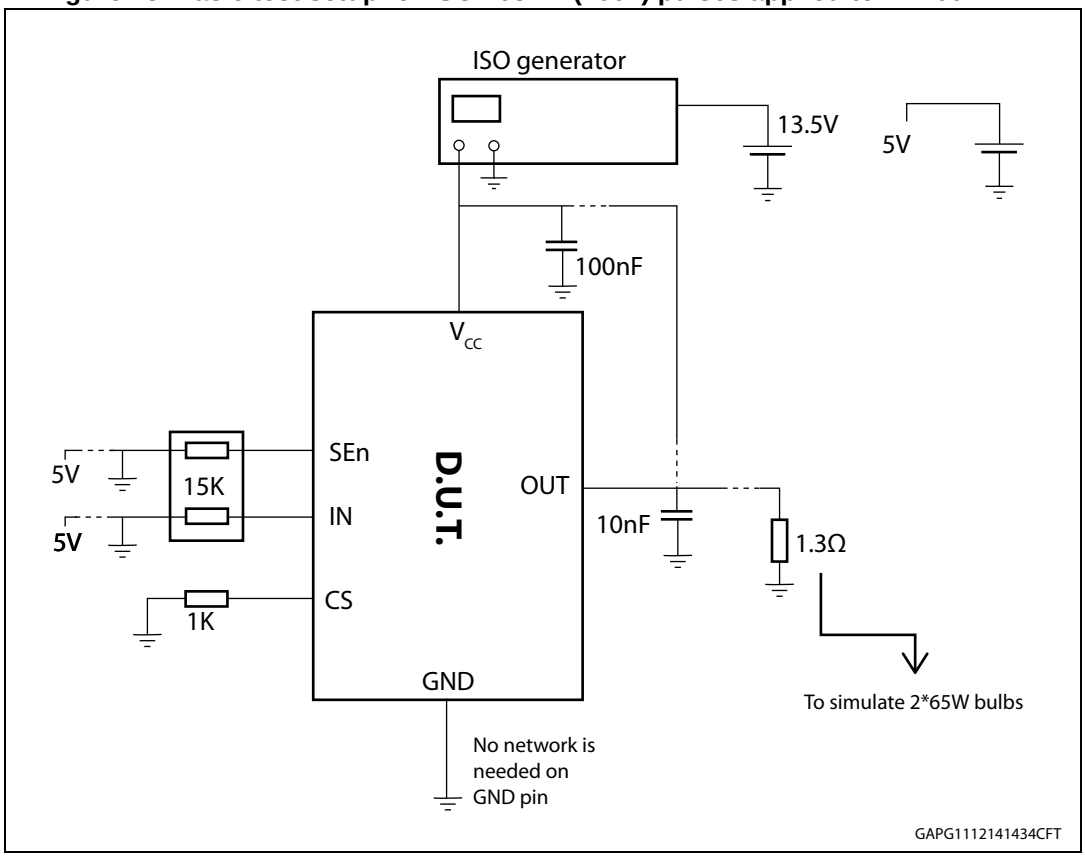
3.6.1 Dimensioning of the series resistors on I/O line

The resistor value should be calculated according to the maximum injected current to I/O pins of the used microcontroller. That value can be assumed equal to 10 mA so that, the resistors value should be at least 13 kΩ (130 V/10 mA); an input series resistor R_i = 15 kΩ can be considered a reasonable value.

The recommended application schematic guarantees device operation according to the below classes standard ISO7637-2 edition 2004 and 2011, as shown in the table below:

- ISO n1 (2 ms/10 Ω, 5K pulses)
  Class C must be complied (full operational after each pulse).
- ISO n2a (50 µs/2 Ω, 5K pulses)
  Class C must be complied (full operational after each pulse).
- ISO n3a (0.1 µs/50 Ω, 1h)
  Class B must be complied (full operational even during pulses exposure)
- ISO n3b (0.1 µs/50 Ω, 1h)
  Class B must be complied (full operational even during pulses exposure)

Figure 23. Basic test setup for ISO 7637-2 (2004) pulses applied to VN7004AH-E

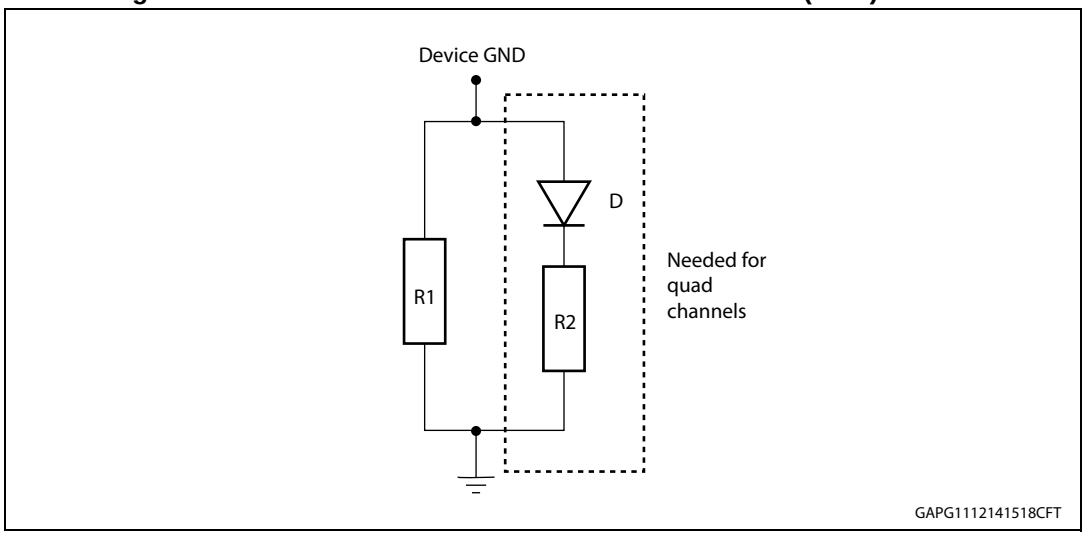


3.6.2 Dimensioning of the GND network to pass the ISO n.1 and 2a level IV (2011 edition)

As already mentioned, to pass the ISO n.1 (-150 V) and 2a (112 V) pulses a dedicated GND network must be used.

The suggested basic solution is represented by a resistance R1 between device GND and module GND

Figure 24. Recommended GND network for ISO 7637-2 (2011) level IV



A second solution with an additional branch in parallel (R2 + low drop diode D) depends on specific considerations. The *Table 8* gives a suggestion according to the Hybrid device type and to the logic level of Input pin adopted.

The given suggestion, based on some experimental measures, take into account a minimum high state input voltage on Regulator's side and the maximum voltage drop on 15 kΩ I/O series resistance.

This yields a maximum allowed GND voltage on the device's GND network for 5 V and 3.3 V system.

Table 8. GND network proposals for Hybrids HSDs

Device/V_{REG} supply voltage	Single/double channels VN7007AH VN7004AH-E VND7012AY	Quad channels VNQ7040AY
5V Assumption: max allowed GND Shift: 1.67 V	Only R1: 150 Ω (value for each driver)	R1 = 270 Ω // (low drop D + series resistor R2 = 47 Ω) (value for each driver) Vz(D) > 150 V
3.3 V Assumption: max allowed GND Shift: 0.33 V	Only R1: 33 Ω (value for each driver)	Only R1 = 18 Ω (value for each driver)

- R1 must be chosen taking into account the two following limits:
  - Minimum value is chosen according to the signal clamp structure energy capability and maximum power dissipation allowed inside the component (the lower is the resistance value the higher is the Power dissipated during the pulses)
  - Maximum value is chosen to guarantee PowerMOS operation in full R_{ON} during reverse battery and a GND shift that guarantees device properly driven ON even in the worst case device limits (relevant parameters to be taken into account at

device level are minimum V_{IH} and maximum $I_{GND(ON)}$, values are both available in datasheets). Experimental trials have led to fix the below range:

— 47 Ω < R1 < 300 Ω in case of 5 V Input logic level and single or double channel Hybrid HSD.

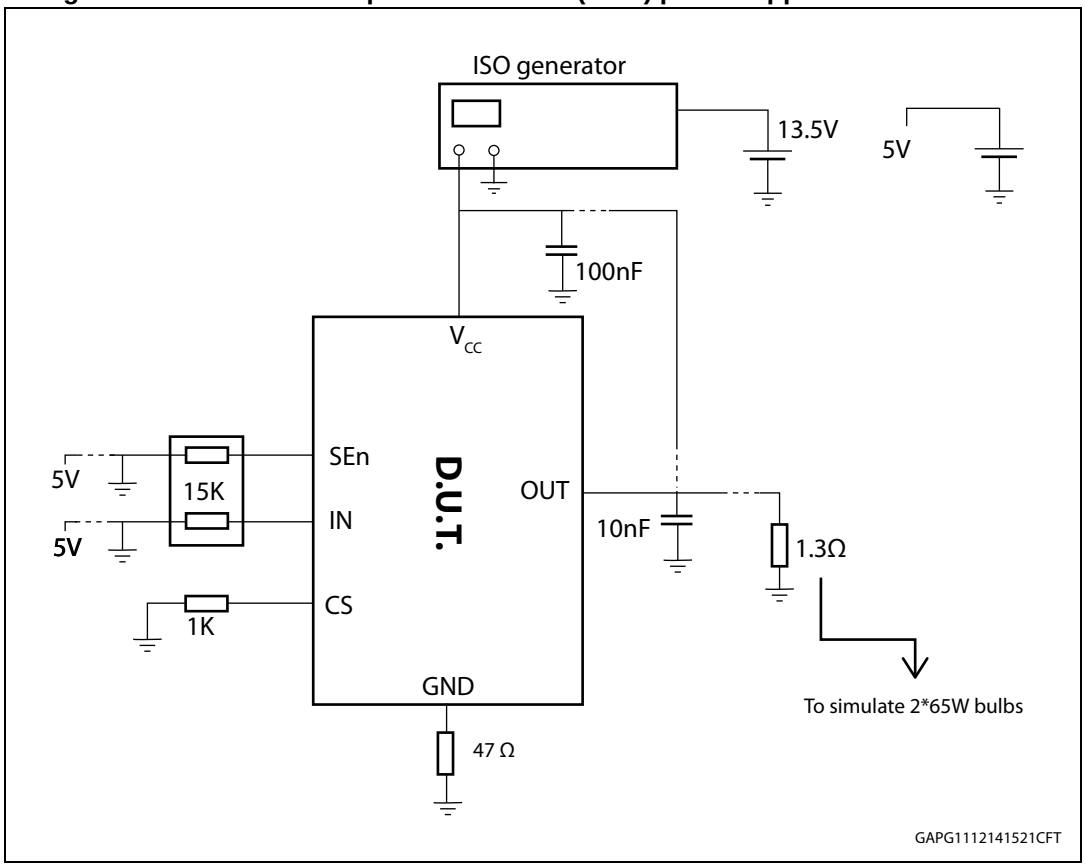
— 18 Ω < R1 < 300 Ω in case of 3.3 V Input logic level and quad channel Hybrid HSD

- The simple reverse battery network (R1) is not always enough. In case of four channels Hybrid HSD, a further D+R2 network is required in order to keep the GND pin voltage drop as little as possible and avoid usage of big space demanding, low ohmic R1 component. R2 must be chosen according to the following limits:
  - Minimum value must limit the current flowing from V_{CC} to GND through the internal signal clamp structure during the ISO 2a pulse;
  - Maximum value according to maximum GND shift that guarantees device properly driven ON even in the worst case device limits (relevant parameters to be taken into account at device level are minimum V_{IH} and maximum $I_{GND(ON)}$, both values are available in datasheets). Experimental trials have led to suggest the below range (assuming R1 = 270 Ω and drop Voltage on diode of 0.4 V):

    — 18 Ω < R2 < 91 Ω

In *Figure 25* a test setup is used in order to measure capability of M0-7 Hybrid device, in this case the VN7004AH-E, to sustain ISO7637-2: (2011) pulses.

Figure 25. Basic Test setup for ISO 7637-2 (2011) pulses applied to VN7004AH-E



Operative conditions (given for VN7004AH-E) are reported below:

- Device in OFF state and output in open load
- Device in OFF state with OUTs in short circuit to GND
- Device in ON state (IN0/IN1 high) and output in open load
- Device in ON state (IN0/IN1 high) driving 1.3 Ω resistive load on each OUT
- Device in Limp Home state (IN0/IN1 pulled-up by 2.7 K + Diode to V_{CC}) and output in OL.

Results are reported in *Table 9*:

Table 9. ISO 7637-2 levels and results for Hybrid HSDs

ISO 7637-2	Test pulse							
	1 Level III	1 Level IV	2a Level III	2a Level IV	3a Level III	3a Level IV	3b Level III	3b Level IV
2004	Class C	Class C	Class C	Class C	Class B	Class B	Class B	Class B
2011	Class C	Class C or E(1)	Class C	Class C or E(2)	Class B	Class B	Class B	Class B
	Class C: full operational after each pulse Class B: full operational even during pulses exposure Class E: One or more functions of the device do not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device							

1. By adding a series resistance (47 Ω) on GND pin, the device is able to pass level IV of ISO 7637-2 (2011) N 1 edition 2011.
2. Device is not able to pass the level IV of ISO 7637-2: 2011 in off-state with open-load condition.
In off-state condition with a minimum series resistance on the GND pin, the device is able to pass level ISO 1 and 2a, level IV of ISO 7637-2: 2011.

Moreover M0-7 Hybrid HSDs pass the load dump clamped pulse test (class C according to *Table 7* criteria) relevant to the standard ISO-7637-2:2004(E) (5b pulse with 40 V centralized load dump suppressor) as well as the standard ISO 16750-2:2010 (E) (pulse with 35 V centralized load dump suppressor).

4 Usage/handling of fault reset and standby

On top of M0-5 Enhanced HSDs functions and protections, in the new M0-7 devices additional features have been implemented:

- Latch-off functionality:
  - FaultRST pin = high:
    The drivers will latch-off in case of power limitation or thermal shutdown. In order to unlatch the channel(s), a low level pulse on FaultRST pin is required for minimum duration of t_{LATCH_RST}. This time ensure the device clears the latch only if required and not accidentally.
  - FaultRST pin = low or left open:
    The drivers will behave like M0-5Enhanced devices (autorestart in case of power limitation or thermal shutdown).
- Standby mode (all generic input pins: IN_x, SE_n, SEL_x, FaultRST low or open):
  A permanent low level on FaultRST pin, SE_n pin, SEL_x pin and all IN_x pins disables all outputs and sets the devices in standby mode after elapse of standby mode blanking time t_{D_STBY} (open load diagnostic in off-state is disabled). Current consumption in this state is I_{STBY}. The device reverts to active mode (normal operation) as soon as at least one of the generic inputs is set high.

FaultRST pin and Latch-off functionality are not present on specific device classes of the M0-7 standard HSD family:

Table 10. M0-7 HSD devices not featuring latch-off functionality and FaultRST pin

Octapak	SO-8
VN7004AH-E	VN7040AS
VN7007AH	VN7050AS
	VN7140AS

Devices listed in *Table 10* operate in auto restart mode in case of power limitation or thermal shutdown.

4.1 Latch-off functionality

The latch-off functionality is available when the FaultRST pin (logic input) is set high. This pin is common for all device channels.

In case an overload occurs, the related channel is automatically latched-off at the first intervention of either power limitation or thermal shutdown. The latch condition is indicated by V_{SENSEH} level on the related multi sense pin. Please refer to the truth tables to identify the conditions to detect a latched channel through the V_{SENSEH} level on the related multi sense pin.

Table 11. Truth table

Mode	Conditions	IN_X	FR	SE_n	SEL_x	OUTx	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected: $T_j < T_{TSD}$ and $\Delta T_j < \Delta T_{j\_SD}$	L	X	Refer to *Table 12*		L	Refer to *Table 12*	
		H	L			H		Outputs configured for auto-restart
		H	H			H		Outputs configured for latch-off
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ and $\Delta T_j > \Delta T_{j\_SD}$	L	X	Refer to *Table 12*		L	Refer to *Table 12*	
		H	L			H		Output cycles with temperature hysteresis
		H	H			L		Outputs latch-off
Undervoltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD}$ + $V_{USD\ hyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	X	Refer to *Table 12*		H	Refer to *Table 12*	
	Open-load	L	X			H		External pull-up
Negative output voltage	Inductive loads turn-off	L	X			<0 V		

Table 12. MultiSense multiplexer addressing for a dual channel device

SE_n	SEL_1	SEL_0	MUXchannel	MultiSense output			
				Normal mode	Overload	OFF-state diag.	Negative output
L	X	X		Hi-Z			
H	L	L	Channel 0 diagnostic	$I_{SENSE} = 1/K * I_{OUT0}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	0
H	L	H	Channel 1 diagnostic	$I_{SENSE} = 1/K * I_{OUT1}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	0
H	H	L	T_{CHIP} sense	$V_{SENSE} = V_{SENSE\_TC}$			
H	H	H	V_{CC} sense	$V_{SENSE} = V_{SENSE\_VCC}$			

As indicated in *Table 12* the V_{SENSEH} failure flag is present on MultiSense pin of a latched channel x, if the following conditions are met:

- MultiSense is enabled (SE_n = High)
- The channel x is driven on through its input (INx = High)
- The multiplexed MultiSense is mapped to channel x through appropriate SELx pin settings

Note: Off-state diagnostic is provided on the MultiSense, if INx = Low.

All latched channels can be restarted by setting the FaultRST pin low for a duration corresponding to the maximum t_{LATCH_RST} (this parameter is given in the datasheet)

A graphical explanation of the latch-off functionality can be seen in *Figure 26*, *Figure 27* and *Figure 28*:

Figure 26. Latch functionality - behavior in hard short circuit condition ($T_{junction} << T_{TSD}$)

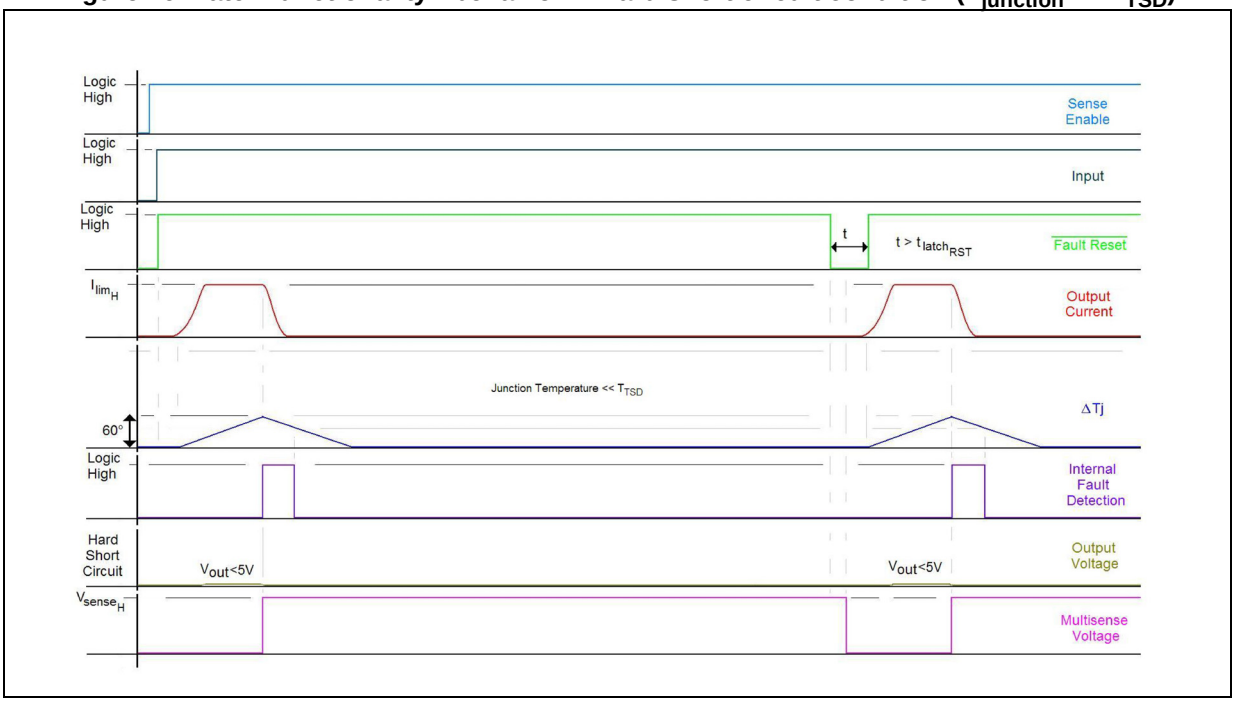


Figure 27. Latch functionality - behavior in hard short circuit condition ($T_R < T_{junction} < T_{TSD}$)

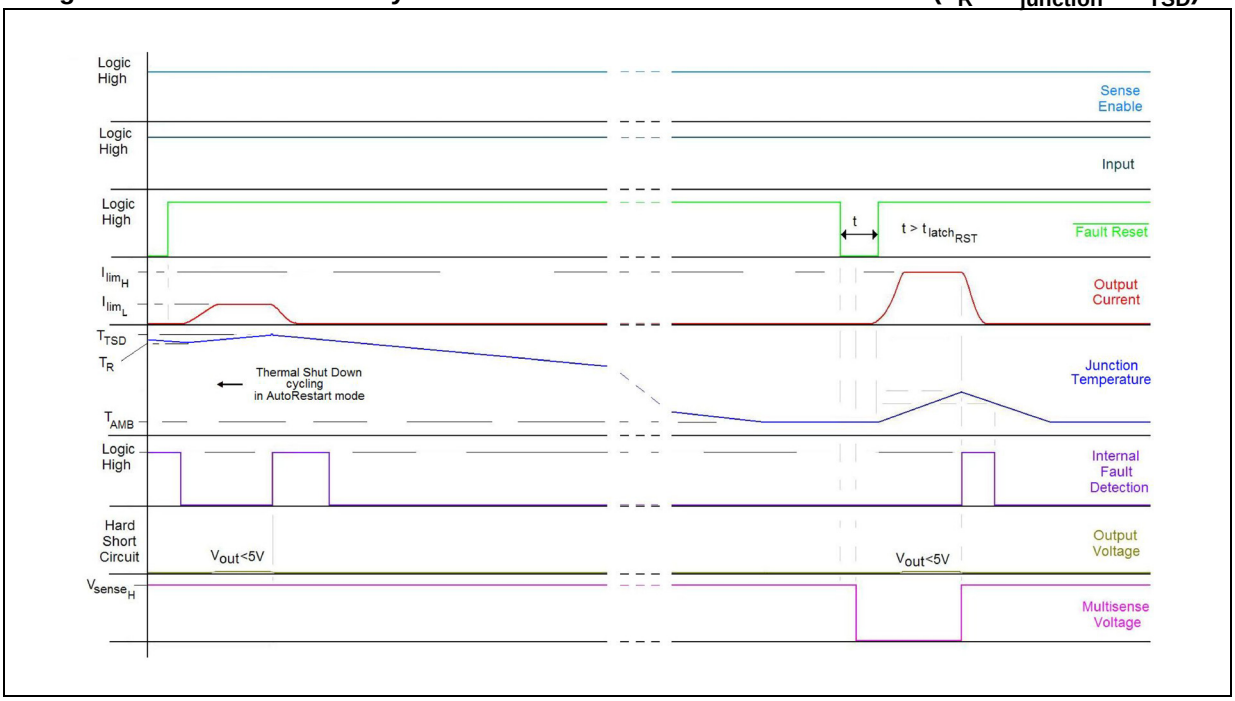
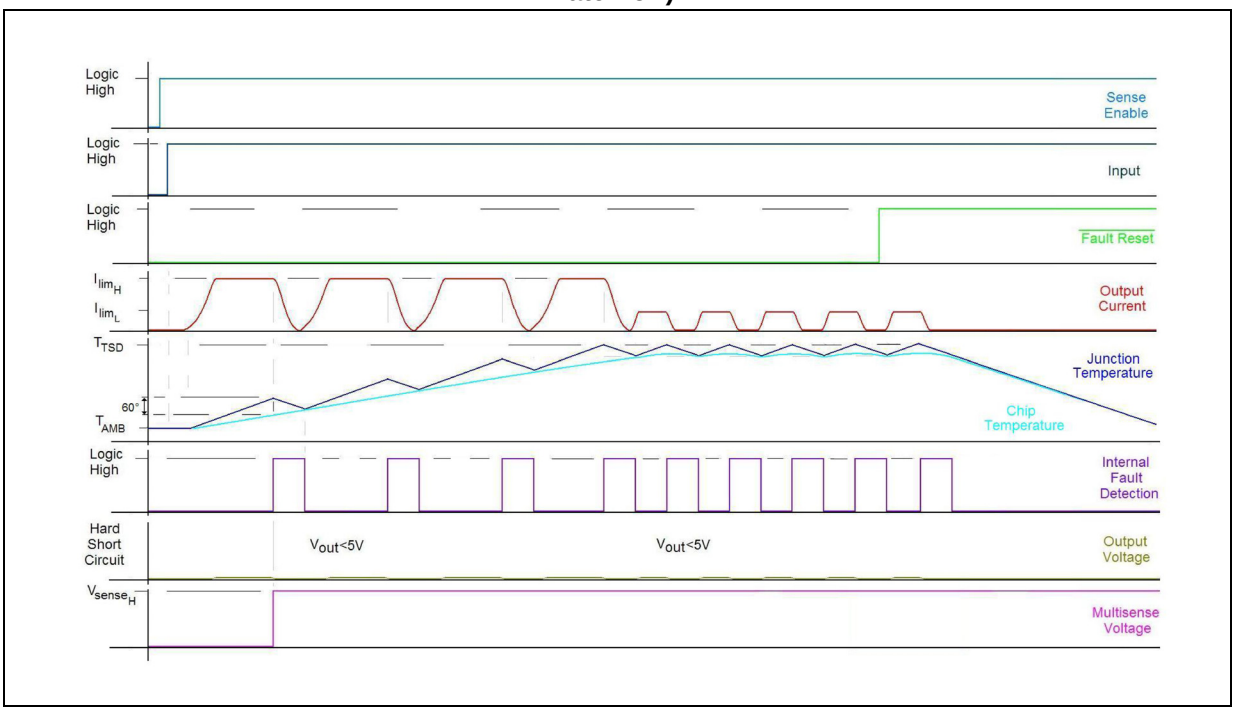


Figure 28. Latch functionality - behavior in hard short circuit condition (autorestart mode and latch-off)



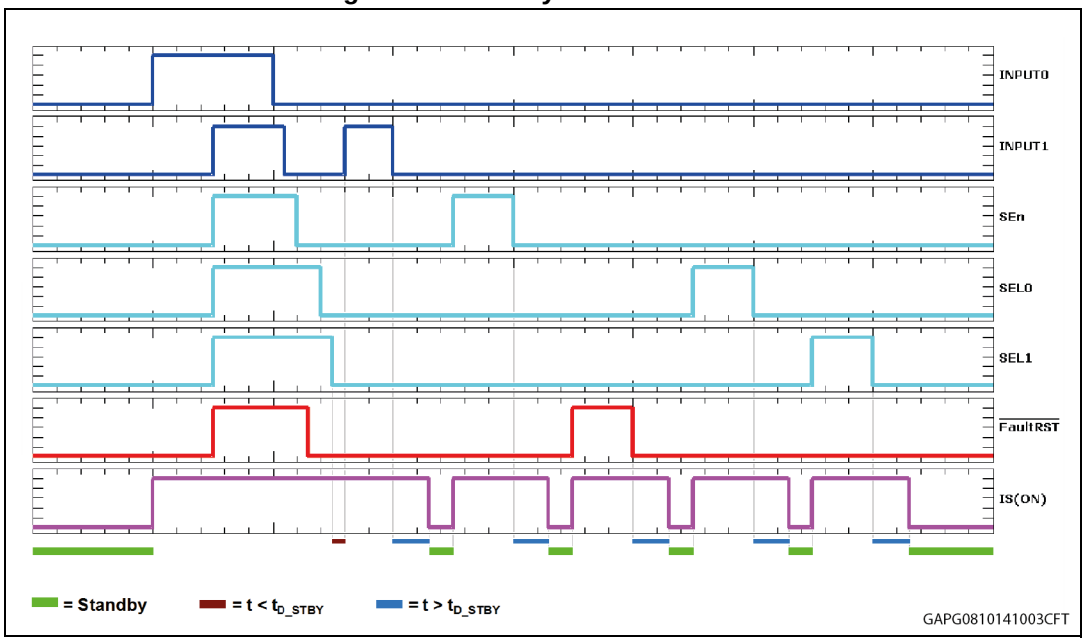
4.2 Standby mode

The standby mode is available when the FaultRST pin, SE_n pin, SEL_x pin and all IN_x pins are set low or open and kept in this condition for a duration corresponding to the maximum t_{D_STBY}. This time, t_{D_STBY}, has been introduced in order to avoid entering the standby condition in case all generic input pins are low during a commutation, so no accidental standby can occur (see *Figure 29*). In standby condition the supply current drops down to 0.5 µA (max at 85 °C).

As soon as the device enters the standby mode, all diagnostic latches are reset. This is also caused by the fact that the FaultRST pin is set low for a time $t_{D\_STBY} > t_{LATCH\_RST}$.

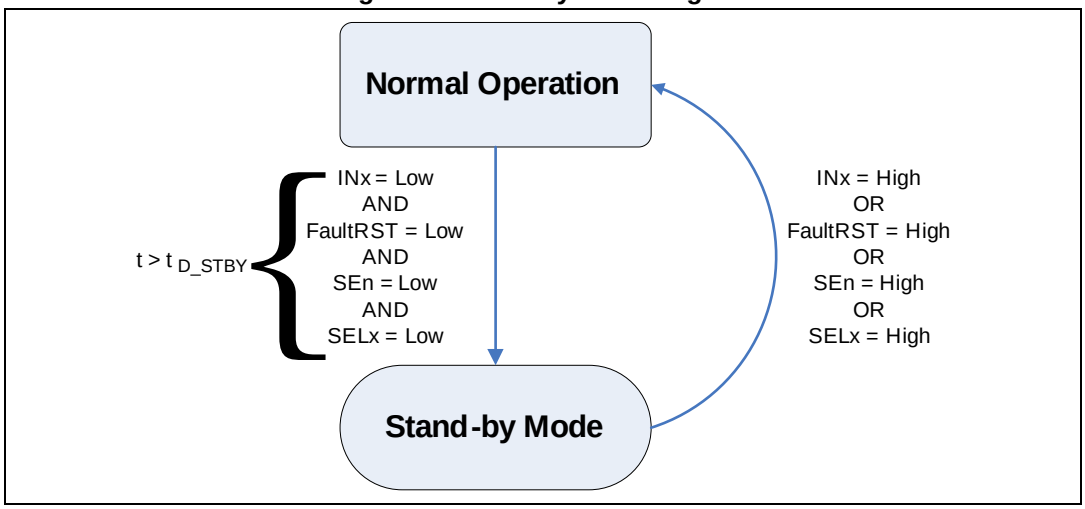
The device exits the standby condition as soon as anyone of FaultRST pin, SE_n pin, SEL_x pin or one of the INx pins is set high.

Figure 29. Standby mode activation



The device leaves the Standby mode when any of the above mentioned pins is set high (see *Figure 30*).

Figure 30. Standby state diagram



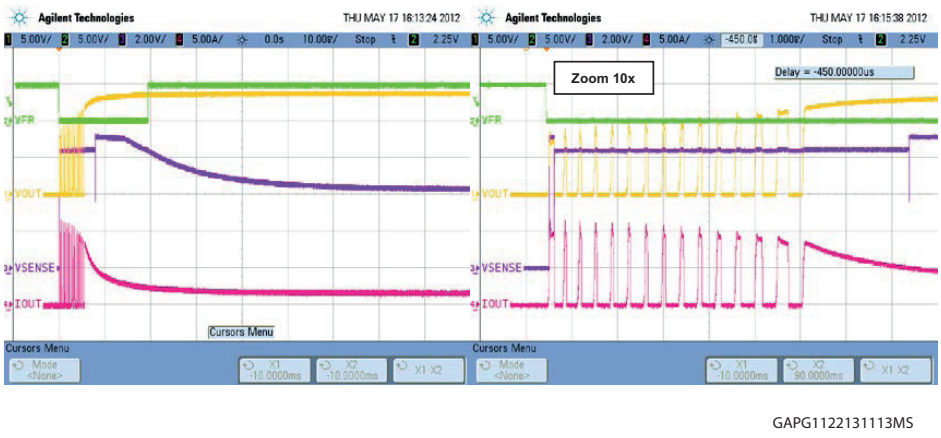
4.3 Flexible blanking time (fault reset management)

On one hand the use of the latch-off functionality provides significant benefits to the application in terms of safety and reliability due to the very fast reaction and protection against hazardous conditions induced by heavy overload or short circuit events. On the other hand it requires from the user a proper selection of the suitable high-side driver for a given load, in example through load compatibility studies (refer to *Chapter 6: Load compatibility*). Concretely, the latch-off functionality might interfere with the load, in case it has an inrush characteristic as for example an incandescent bulb, a DC motor or a capacitive load. The transient current, which typically has the highest peak at low ambient

temperature and high battery voltage, may trigger the power limitation, leading to latch-off of the HSD. In consequence the load will not be turned on. Even though the device could be restarted again by toggling FaultRST pin low for a time longer than t_{LATCH_RST}, so that all latches are reset, the latch will occur again as long as the device is maintained in latch-off mode.

A possible way to overcome this issue is managing the FaultRST pin in such a way that the latch-off functionality is blanked out for a time longer than the time of the inrush of the bulb. The following figure is giving an example, on how the correct turn-on of an incandescent bulb is ensured by means of a 20 ms blanking pulse on FaultRST pin. Despite the device toggles in Power Limitation for approximately 10 ms, the load is correctly activated with negligible delay.

Figure 31. FR handling example - bulb inrush blanking (VNQ7140AJ)



Even more, the FaultRST pin can be managed as a global system pin, connecting this pin of several high-side drivers in parallel to a specific microcontroller I/O port (refer to example in *Figure 32* and *Section 8.1: Paralleling of logic input pins* for advice on how to parallel pins). This signal is always kept high, means all connected devices are configured in latch-off mode, except

- For a periodical “unlatch” pulse for duration longer than t_{LATCH_RST} max, once per diagnostic period. This “unlatch” pulse aims at restarting all latched channels, which are supposed to be restarted, i.e. when the debouncing strategy for short circuit detection is not yet elapsed.
- For a blanking pulse (FaultRST low for i.e. 10 ms) generated at every activation of any channel.

Figure 33 illustrates the described FaultRST pin handling concept.

Figure 32. Common FaultRST pin handling example – basic schematic (without decoupling components)

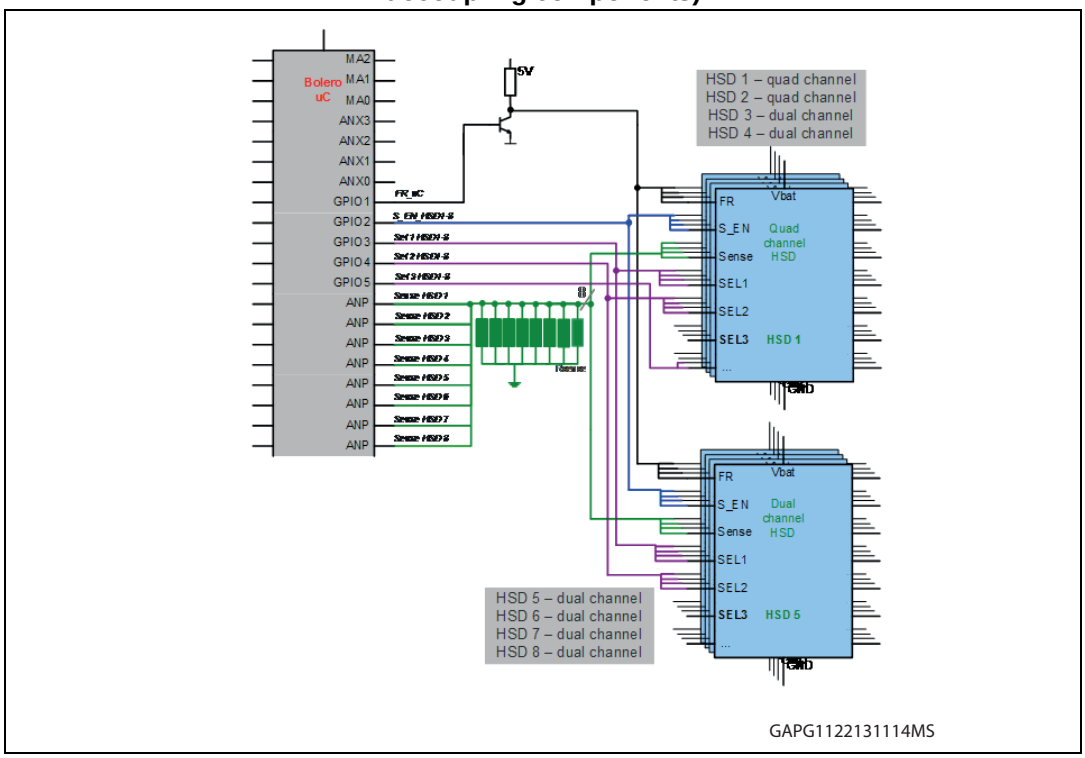
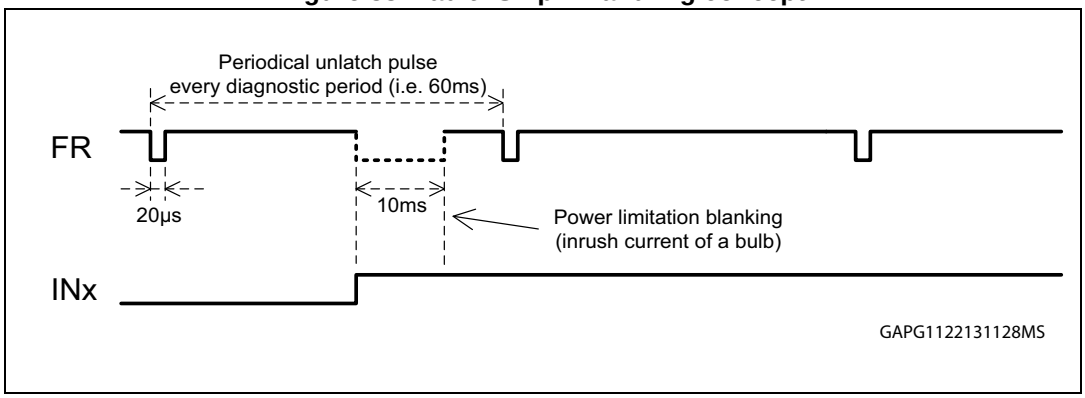


Figure 33. FaultRST pin handling concept



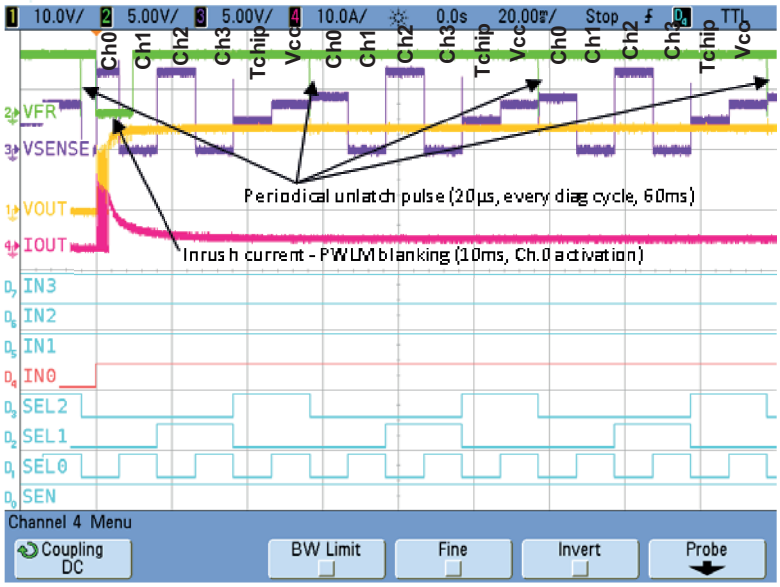
A practical example shall further clarify the concept. A quad channel device is used in the following conditions:

- OUT0: bulb (start-up)
- OUT1: floating
- OUT2: short to GND (permanent on)
- OUT3: floating

Channel 0 is switched on. Channel 1-3 are permanently on. The MultiSense multiplexer is switched every 10 ms in order to monitor sequentially the current sense information on channels 0-3, the T_{CASE} temperature information and the V_{CC} local supply voltage information. Consequently it takes 60ms to sample once each diagnostic source. On the FaultRST pin a 20 µs “unlatch” pulse is forced once per diagnostic period and 10 ms

blanking pulse is imposed synchronously with the rising edge on IN0. During bulb inrush Channel 0 operates in power limitation for a few ms.

Figure 34. FaultRST pin handling example - overview



While *Figure 34* shows an overview about the sequence of periodical unlatch pulses and the blanking pulse on FaultRST pin over several diagnostic periods, *Figure 35* provides the detail of one diagnostic period. CurrentSense on channel 0 rises to V_{SENSEH} failure flag as soon as the channel enters in power limitation. Thanks to the blanking pulse the channel is able to turn on the bulb correctly in autorestart mode. CurrentSense on channel 1 and channel 3 report open load failures. CurrentSense on channel 2 indicates the channel is latched-off due to a power limitation or overtemperature event.

Figure 36 shows the effect of the regular “unlatch” pulse on the shorted channel 2, as long as its input is kept high. After elapse of t_{LATCH_RST} the channel is turning on into the short circuit and latching off again as soon as ΔT_{j_SD} dynamic temperature threshold (power limitation) is reached. This fast device intervention protects the device and the system, including connectors and wire harness, from short circuit stress induced degradation. For details regarding device endurance in short circuit conditions, refer to the relevant AEC-Q100-012 characterization reports.

Figure 35. FaultRST pin handling example – detail of diagnostic period

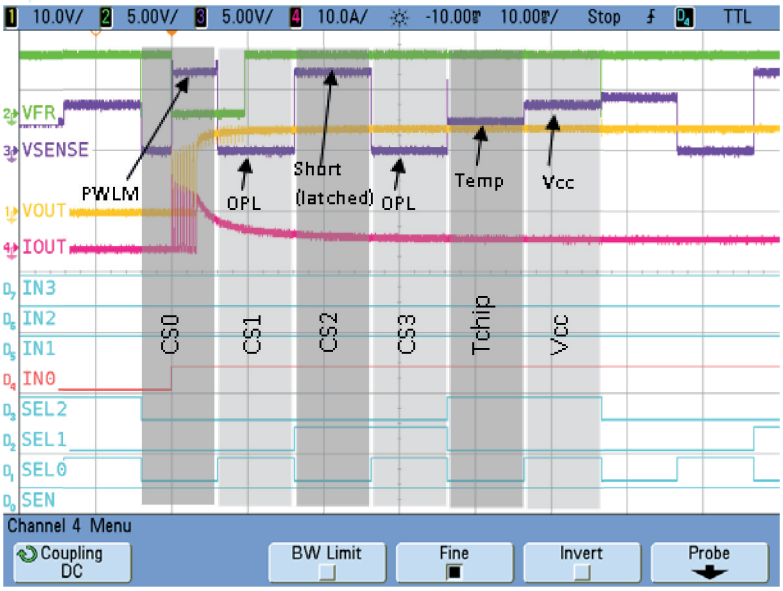
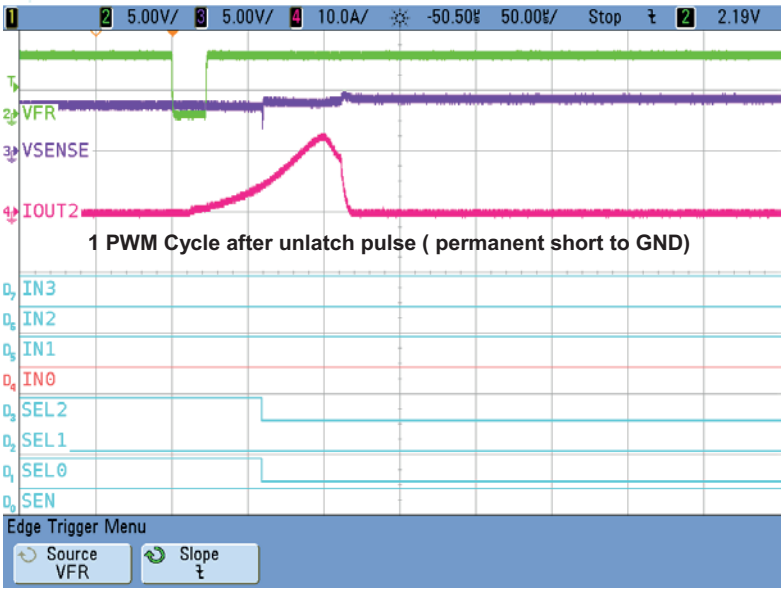


Figure 36. FaultRST pin handling example – detail of unlatch pulse (Ch. 2)



5 Usage and handling of MultiSense SEL pin

For diagnostic of M0-7 devices one analog monitoring output signal is used. It is capable to provide current sense signal reflecting channel output current or digital failure flag in off state signaling open load (provided by the presence of an external pull-up resistor) or short to V_{CC} diagnostic. Information about device temperature or V_{CC} voltage can be also selected. Signal output is controlled by SE_n pin (enable/disable MultiSense output signal) and a set of SEL pins (used for diagnostic signal selection). The number of control pins depends on implementation and number of channels applied on device.

5.1 Classification of M0-7 HSDs

As preamble of this chapter, we can consider the M0-7 high-side drivers as belonging to two main groups:

- Monolithic HSDs: one chip is present inside the package
- Hybrid HSDs: two chips are present inside the package, one acting as power stage and the other one acting as drive, control and protection stage.

The main difference between the two categories from an application standpoint is that the Hybrid HSDs have an additional integrated protection against the reverse battery event (please refer to *Chapter 2: Reverse battery protection*).

In *Table 13* the current M0-7 set of high-side drivers according to the above classification is presented. The assembly package to which the final suffix in the part number is referring to is indicated as well.

Table 13. Classification of M0-7 HSDs

Typical R_{ON}	1 channel	2 channels	4 channels
4 mΩ	VN7004AH-E(1)	VND7004AY(1)	
7 mΩ	VN7007AH(1)		
10 mΩ	VN7010AJ(2)		
12 mΩ		VND7012AY(1)	
16 mΩ	VN7016AJ(2)		
20 mΩ	VN7020AJ(2)	VND7020AJ(2)	
30 mΩ		VND7030AJ(2)	
40 mΩ	VN7040AJ VN7040AS(2)	VND7040AJ(2)	VNQ7040AY(1)
50 mΩ	VN7050AJ VN7050AS(2)	VND7050AJ(2)	VNQ7050AJ(2)
140 mΩ	VN7140AJ VN7140AS(2)	VND70140AJ(2)	VNQ7140AJ(2)

1. Hybrid HSD.
2. Monolithic HSD.

Note: Final suffix: J = PowerSS0-16; H = OctaPAK; S = SO-8; Y = PowerSSO-36.

5.2 SEL pins truth table (device dependant)

There are defined two main categories:

- Full logic implementation - provide output current sense, V_{CC} and T_{CHIP} sensing
- Reduced logic implementation - only current sense of output(s)

Complete encoding and its mapping to devices can be found in the following tables (different colors show mapping between device and SEL pins used)

Table 14. Full logic implementation

SEL_2	SEL_1	SEL_0	SE_n	MultiSense output signal		
Quad channel control signals						
	Double channel control signals					
	Single channel control signals					
X	X	X	L	Hi-Z	Hi-Z	Hi-Z
L	L	L	H	Current Sense	Current Sense Ch0	Current Sense Ch0
L	L	H	H		Current Sense Ch1	Current Sense Ch1
L	H	L	H	T_{CHIP} Sense	T_{CHIP} Sense	Current Sense Ch2
L	H	H	H	V_{CC} Sense	V_{CC} Sense	Current Sense Ch3
H	L	L	H			T_{CHIP} Sense
H	L	H	H			V_{CC} Sense
H	H	L	H			T_{CHIP} Sense
H	H	H	H			V_{CC} Sense

Only quad channel devices have SEL_2

Devices list		
	VND7004AY	
VN7010AJ	VND7012AY	VNQ7040AY
VN7016AJ	VND7020AJ	
VN7020AJ	VND7030AJ	
VN7040AJ	VND7040AJ	VNQ7040AY
VN7050AJ	VND7050AJ	
VN7140AJ	VND7140AJ	VNQ7140AJ

Table 15. Reduced logic implementation (only current sense signal, no T_{CHIP}, no V_{CC})

SEL_1	SEL_0	SE_n	MultiSense output signal	
Quad channel control signals				
		Single channel control signal		
X	X	L	High Z	High Z
L	L	H	Current Sense	Current Sense Ch0
L	H	H	—	Current Sense Ch1
H	L	H	—	Current Sense Ch2
H	H	H	—	Current Sense Ch3
Only quad channel device has SEL_0, SEL_1			Devices list	
			VN7004AH-E	VNQ7050AJ
			VN7007AH	
			VN7040AS	
			VN7050AS	
			VN7140AS	

5.3 Connection of SEL pins with control logic (Microcontroller)

SEL pins are usually driven by microcontroller in order to select MultiSense output signal (for diagnostic purposes). In order to save microcontroller pins, multiple devices SEL pins can be driven in parallel, sharing the same Microcontroller pins. To protect devices and Microcontroller from disturbances or possible damage, there are valid recommendations for paralleling of SEL pins (for details, see *Chapter 11: Usage in "H-Bridge" configurations*).

The following examples show possible combinations and influence to a hardware connection scheme.

Example 1

- VN7020AJ + VND7020AJ + VNQ7140AJ
- Common power supply, common GND network
- Common SE_n, $SEL_{0...2}$ (separate MultiSense)

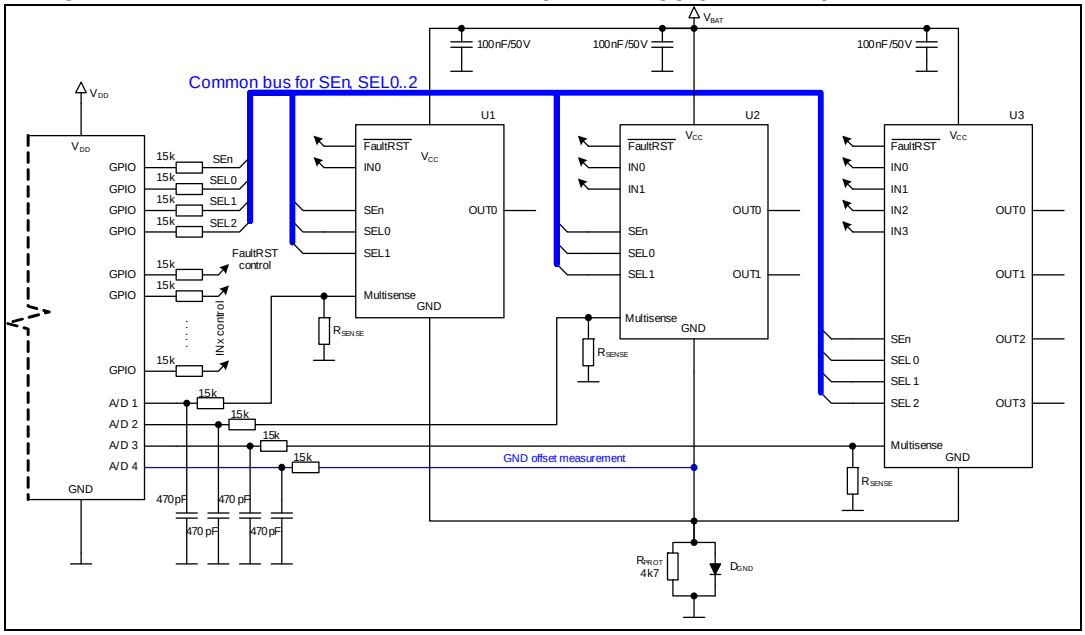
All three devices are designed in monolithic technology. Devices have different number of SEL pins. In order to use only one protection resistor on the side of microcontroller, there must be used common V_{BAT} power supply as well as the same ground protection network (fulfilling conditions for paralleling SELn on monolithic devices). Each HSD's MultiSense output is mapped to separate A/D input.

Additional A/D channel is used for measurement of GND protection network offset. While MultiSense is switched to voltage mode (V_{BAT} or T_{CASE}), output level is referred to device ground (not to global GND).

To adjust measured MultiSense value of V_{BAT} or T_{CASE}, GND offset measured value can be used accordingly:

V_{BAT} or T_{CHIP} corrected value = $V_{SENSE} - V_{GND}$

Figure 37. Monolithic devices, common power supply rails, separate MultiSense



Truth table shows signals mapping.

Table 16. Truth table for monolithic devices, separate MultiSense

SEL_2	SEL_1	SEL_0	SE_n	A/D 1 MultiSense U1 VN7020AJ	A/D 2 MultiSense U2 VND7020AJ	A/D 3 MultiSense U3 VNQ7140AJ
X	X	X	L	Hi-Z	Hi-Z	Hi-Z
L	L	L	H	Current Sense	Current Sense Ch0	Current Sense Ch0
L	L	H	H		Current Sense Ch1	Current Sense Ch1
L	H	L	H	T_{CHIP} Sense	T_{CHIP} Sense	Current Sense Ch2
L	H	H	H	V_{CC} Sense	V_{CC} Sense	Current Sense Ch3
H	L	L	H	Current Sense(1)	Current Sense Ch0(1)	T_{CHIP} Sense
H	L	H	H		Current Sense Ch1(1)	V_{CC} Sense
H	H	L	H	T_{CHIP} Sense(1)	T_{CHIP} Sense(1)	T_{CHIP} Sense
H	H	H	H	V_{CC} Sense(1)	V_{CC} Sense(1)	V_{CC} Sense

1. SEL_2 not applicable - output according SEL_1, SEL_0 and SE_n.

Example 2

- VN7020AJ + VND7020AJ + VNQ7140AJ
- Common power supply, common GND network
- Common MultiSense (separate SE_n control)

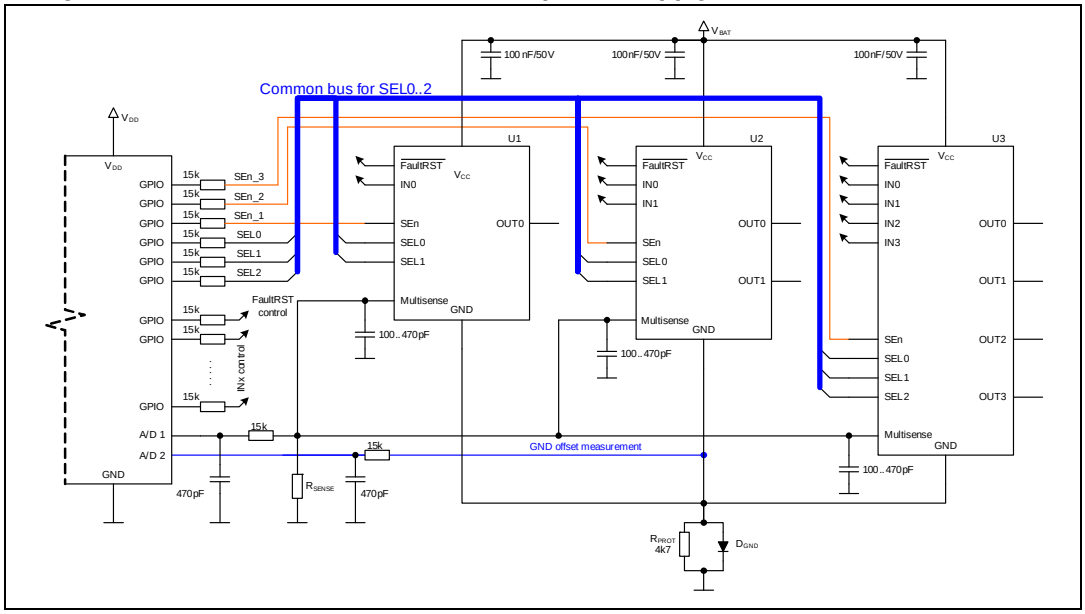
The same HSDs are used like in *Example 1*, but different topology is used - separate SE_n, common MultiSense signal. This option uses only one A/D channel for all HSDs.

On the other hand, a decreased number of analogue channels increases the number of control signals - separate SE_n Pins control. In total, pin count is the same as in *Example 1*.

The same strategy as GND offset measurement is used in this example.

Improper configuration on SEn_1...2 outputs causes no valid V_{SENSE} result (multiple MultiSense outputs can be activated - applied into common R_{SENSE}).

Figure 38. Monolithic devices, common power supply rails, common MultiSense



Truth table shows signals mapping.

Table 17. Truth table for monolithic devices, common MultiSense

SEL_2	SEL_1	SEL_0	SEn_U1	SEn_U2	SEn_U3	A/D (MultiSense)	
X	X	X	L	L	L	Hi-Z	
N/A	L	L	H	L	L	Current Sense	MultiSense U1 VN7020AJ
	L	H	H	L	L		
	H	L	H	L	L	T_{CHIP} Sense	
	H	H	H	L	L	V_{CC} Sense	
N/A	L	L	L	H	L	Current Sense Ch0	MultiSense U2 VND7020AJ
	L	H	L	H	L	Current Sense Ch1	
	H	L	L	H	L	T_{CHIP} Sense	
	H	H	L	H	L	V_{CC} Sense	

Table 17. Truth table for monolithic devices, common MultiSense (continued)

SEL_2	SEL_1	SEL_0	SEn_U1	SEn_U2	SEn_U3	A/D (MultiSense)	
L	L	L	L	L	H	Current Sense Ch0	MultiSense U3 VNQ7140AJ
L	L	H	L	L	H	Current Sense Ch1	
L	H	L	L	L	H	Current Sense Ch2	
L	H	H	L	L	H	Current Sense Ch3	
H	L	L	L	L	H	Hi-Z	
H	L	H	L	L	H	Hi-Z	
H	H	L	L	L	H	T_{CHIP} Sense	
H	H	H	L	L	H	V_{CC} Sense	
x	x	x	Other combinations of SE_n			Hazard states	

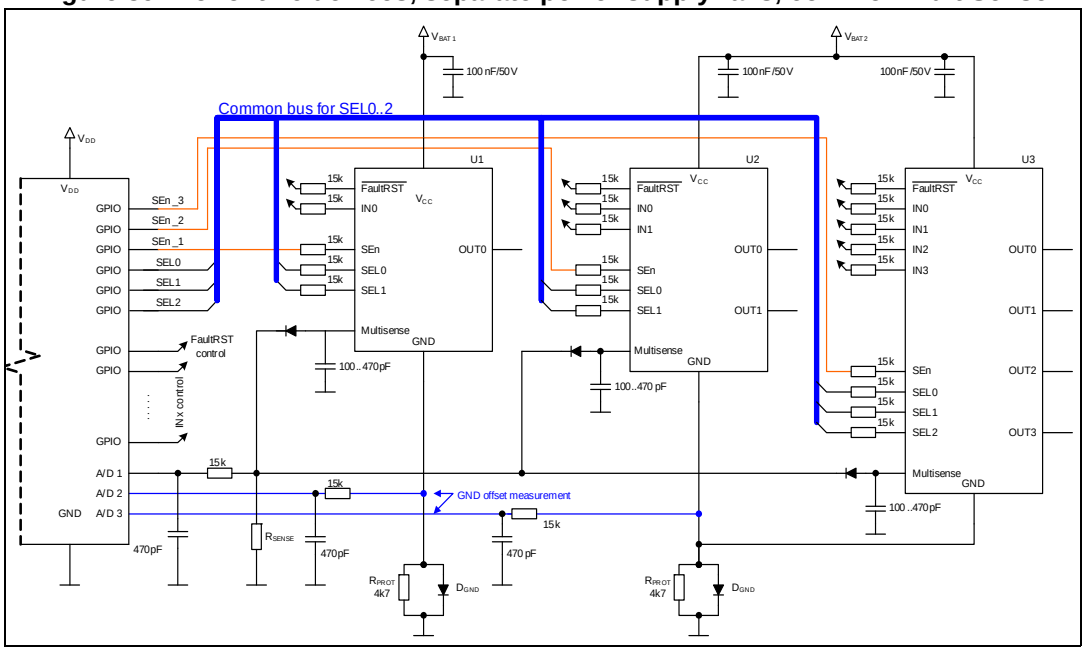
Example 3

- VN7020AJ + VND7020AJ + VNQ7140AJ
- Separate power supply lines, common GND network
- Common MultiSense (Separate SE_n control)

Topology of control part (SEn, $SEL_{0...2}$) is similar to *Example 2*. The main difference consists of using separate power supply lines on HSDs. Due to this fact, recommendations of paralleling SEL signals are implemented as well as MultiSense input (described in *Chapter 8: Paralleling of devices*):

- MultiSense monitor is using diode in series to on MultiSense outputs
- Each HSD control signal is using own protection resistor

Figure 39. Monolithic devices, separate power supply rails, common MultiSense



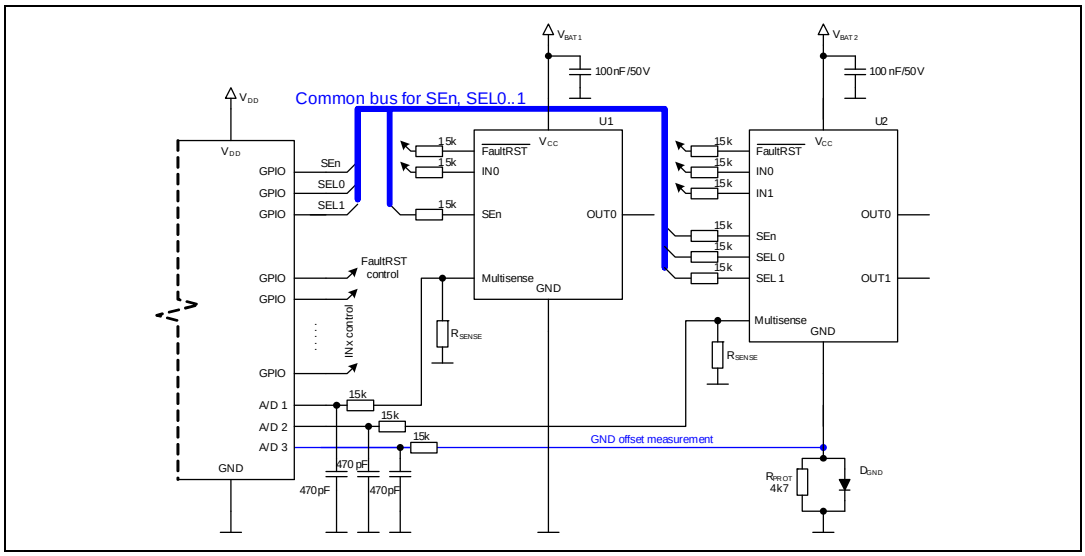
Signals mapping truth table is the same as in *Example 2*.

Example 4

- VN7004AH-E + VND7020AJ
- Separate power supply lines
- Common control pins (SE_n), separate MultiSense

Depicted is a combination of hybrid and monolithic HSDs. In order to use common control signals for both HSDs, protection resistor is used for each device separately (see *Chapter 8: Paralleling of devices* , paralleling monolithic and hybrid HSDs). Additional A/D is used for GND shift offset compensation of T_{CHIP} and V_{BAT} signals.

Figure 40. Monolithic and hybrid device, separate power supply rails, separate MultiSense



Truth table shows signals mapping.

Table 18. Truth table monolithic + hybrid, separate MultiSense

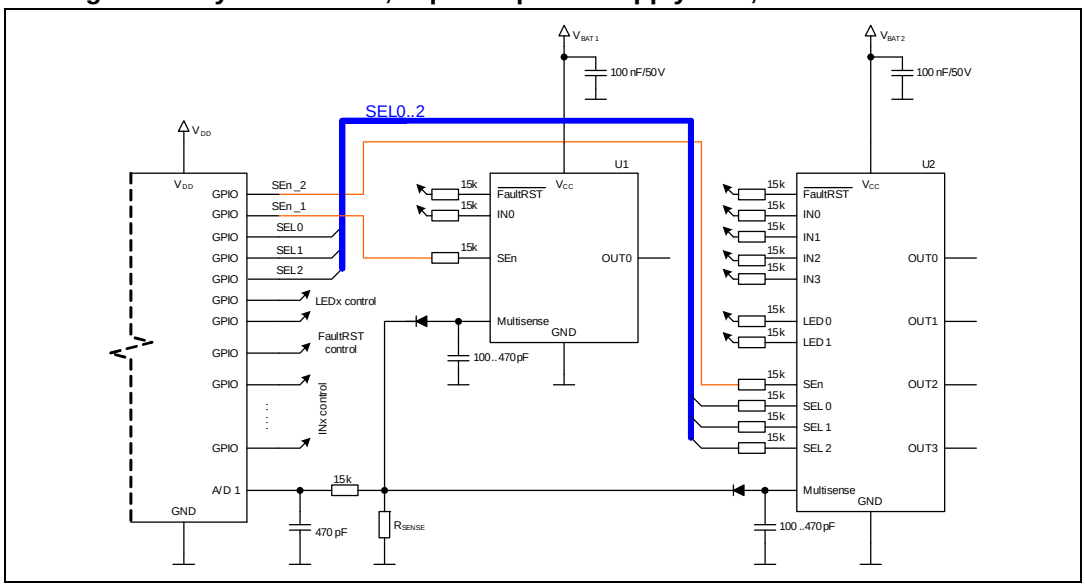
SEL_1	SEL_0	SEn	A/D 1 MultiSense U1 VN7004AH-E	A/D 2 MultiSense U2 VND7020AJ
X	X	L	Hi-Z	Hi-Z
L	L	H	Current Sense	Current Sense Ch0
L	H	H		Current Sense Ch1
H	L	H		T_{CHIP} Sense
H	H	H		V_{CC} Sense

Example 5

- VN7004AH-E + VNQ7040AY
- Separate power supply lines
- Separate SE_n control pins (common MultiSense)

Because of both hybrid HSDs share common MultiSense and different power supply lines are used on each HSD, serial protection diode is used on each device MultiSense output.

Figure 41. Hybrid devices, separate power supply rails, common MultiSense



Truth table shows signals mapping.

Table 19. Truth table hybrid devices separate supply rails, common MultiSense

SEL_2	SEL_1	SEL_0	SEn_U1	SEn_U2	A/D (MultiSense)	
X	X	X	L	L	Hi-Z	
N/A			H	L	Current Sense	MultiSense U1 VN7004AH-E
L	L	L	L	H	Current Sense Ch0	MultiSense U2 VNQ7040AY
L	L	H	L	H	Current Sense Ch1	
L	H	L	L	H	Current Sense Ch2	
L	H	H	L	H	Current Sense Ch3	
H	L	L	L	H	T_{CHIP} Sense	
H	L	H	L	H	V_{CC} Sense	
H	H	L	L	H	T_{CHIP} Sense	
H	H	H	L	H	V_{CC} Sense	
X	X	X	H	H	Hazard states	

6 Load compatibility

6.1 Bulbs

This chapter is intended to suggest drivers that can be used for typical automotive bulb loads or typical combinations of bulbs. A major consideration when driving bulbs is the inrush current generated when starting up a cold filament.

A properly selected driver should allow the safe turn on of the bulb without any restrictions under normal conditions. Under worst case conditions the driver should still be able to turn on the bulb even if some protection of the driver may be triggered temporarily. However, the drivers´ long term integrity should not be jeopardized. Typical combinations of bulbs and M0-7 devices (R_{ON} classes), are shown in the following *Table 20*.

Table 20. Typical bulb loads for given M0-7 R_{ON} class

Device R_{DSON} class [mΩ]	Suggested bulb types and combinations in the given *1.*, *2.* and *3.* conditions
4	2 x H1 (2 x 55 W) 2 x H4 (2 x 55 W/60 W) 2 x H7 (2 x 55 W) 2 x H9 (2 x 65 W)
7	H1 (55 W) H4 (55 W/60 W) H7 (55 W) H9 (65 W)
10	H1 (55 W) H4 (55 W/60 W) H7 (55 W) H9 (65 W)
12	3 x P27 W + R5 W H1 (55 W) H4 (55 W/60 W) H7 (55 W) H9 (65W)
16	H1 (55 W) H4 (55 W/60 W) H7 (55 W) H9 (65 W)
20	2 x P21 W 2 x P27 W 2 x P21 W + R5 W 2 x P27 W + R5 W
30	2 x P21 W + R5 W 2 x P27 W
40	P21 W + R5 W P27 W + R5 W

Table 20. Typical bulb loads for given M0-7 R_{ON} class (continued)

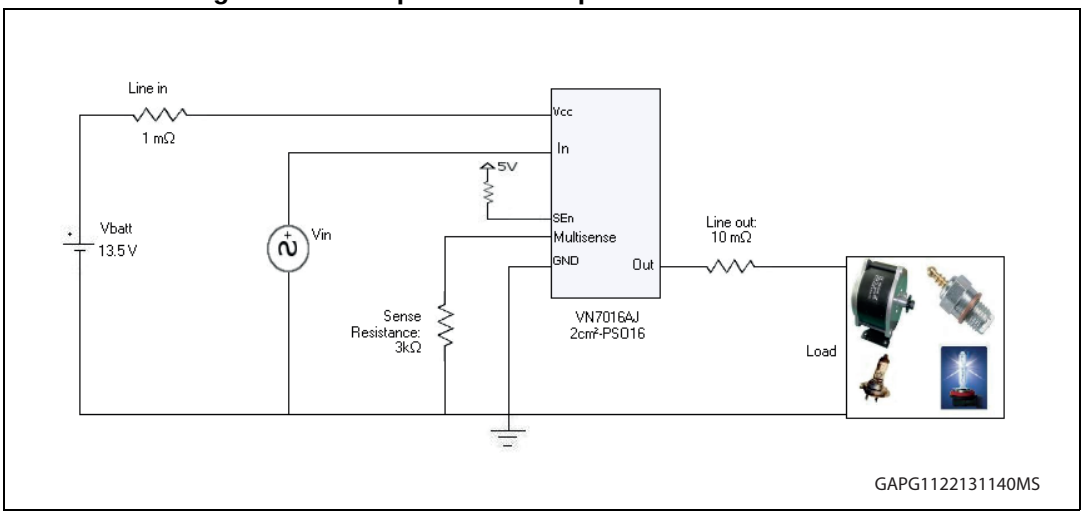
Device R_{DSON} class [mΩ]	Suggested bulb types and combinations in the given *1.*, *2.* and *3.* conditions
50	P21 W P27 W(1)
140	2 x R5 W R10 W(2)

1. Condition *3.* applied to VNQ7050AJ is fulfilled with T_{CASE} = 90 °C
2. Condition *3.* applied to VNQ7140AJ is fulfilled with T_{CASE} = 95 °C

Simulation example – VN7016AJ with H4 bulb (60 W)

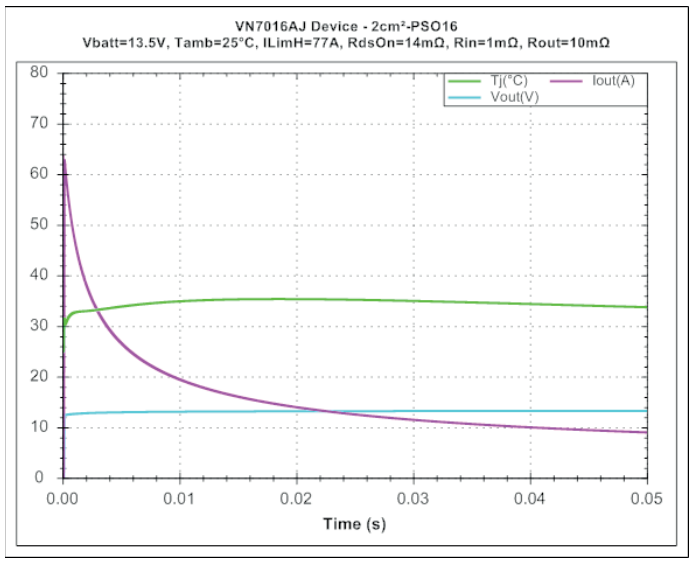
A simulation is performed in order to verify if the driver is able to turn on the bulb and matches the requirements under the defined conditions – see *1.: Normal condition*, *2.: Cold condition* and *3.: Hot condition* below. The tool used for this simulation is based on Matlab/Simulink.

Figure 42. Principle of the setup used for the simulation



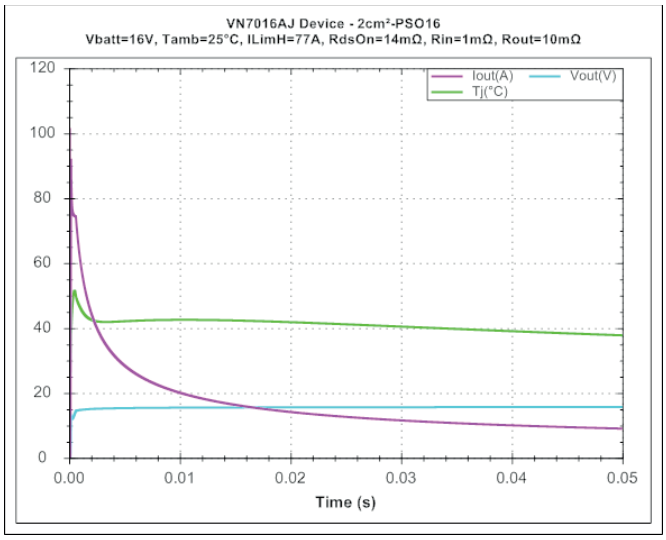
1. Normal condition
   - V_{BAT}: 13.5 V
   - T_{CASE}: 25 °C
   - T_{BULB}: 25 °C
   - Requirement: none of the protection functions must be triggered.

Figure 43. Simulation result–normal condition



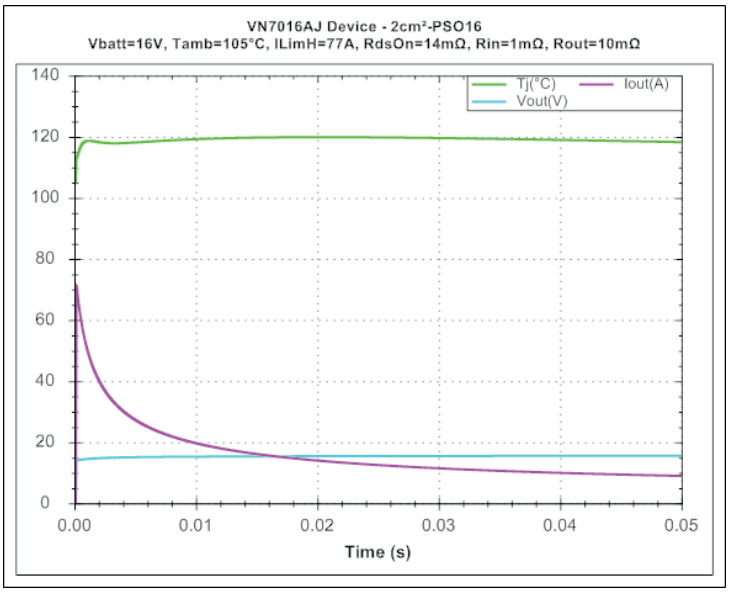
2. Cold condition
   - V_{BAT}: 16 V
   - T_{CASE}: 25 °C
   - T_{BULB}: 25 °C
   - Requirement: power limitation allowed for durations of less than 20 ms (autorestart mode considered).

Figure 44. Simulation result–cold condition



3. Hot condition
   - V_{BAT}: 16 V
   - T_{CASE}: 105 °C
   - T_{BULB}: 25 °C
   - Requirement: thermal shutdown is allowed for a duration below 20 ms (autorestart mode considered).

Figure 45. Simulation result–hot condition



Conclusion

The device is able to turn-on a H4 bulb (60 W) under specified conditions *1.: Normal condition*, *2.: Cold condition* and *3.: Hot condition* without triggering the device protection functions (Power Limitation, Thermal shutdown).

Note: The mentioned simulation example only refers to the inrush current at turn-on of a cold bulb. Still the steady state power dissipation and, in case of PWM is applied, the additional switching losses of the driver have to be considered in order not to exceed the maximum. possible power dissipation. This obviously becomes more important with a larger number of channels per package (i.e. dual or quad channel drivers) and high power loads applied to more than one channel. In case the application requires latch mode configuration of the HSD, in order to avoid unwanted turning off of the bulb during the inrush phase it is suggested to implement a proper software strategy, in order to set up a blanking time whenever the inrush of the bulb occurs. Blanking time length depends on environmental conditions, bulb type and device type.

6.2 Power loss calculations

The power loss calculation is an important step during the application design as it is a basis for further thermal considerations and PCB design.

This chapter is intended to provide guidelines for calculation and estimation of power dissipation in the device in combination with different kind of loads (resistive, inductive, capacitive etc.) and with different modes of operation (steady state, PWM).

All next evaluations are focused on power losses in the power MOSFET of the device. The power dissipation of other parts (control logic, charge pump) is in most cases negligible. If needed, it can be calculated from the device supply current (I_S) and supply voltage value (V_{CC}):

Device control part power dissipation [W]:

$$P_{CTRL} = V_{CC} \cdot I_{GND(ON)}$$

Example 1: For VND7020AJ

Figure 46. Control stage current consumption in ON state, all channels on driving nominal load - datasheet value)

$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{FR} = $V_{SEL0,1}$ = 0 V; V_{IN0} = 5 V; V_{IN1} = 5 V; I_{OUT0} = 3 A; I_{OUT1} = 3 A	—	—	12	mA

$$P_{CTRL} = V_{CC} \cdot I_{GND(ON)} = 13V \cdot 12mA = 156mW$$

The next description is divided into 2 sub-chapters:

- Conduction losses: steady-state losses (during the ON state)
- Switching losses: losses during switching phases

6.2.1 Conduction losses

The conduction losses are given by the power dissipation of the MOSFET switch due to the ON state resistance (R_{ON}).

ON state power dissipation [W]:

$$P_{ON} = R_{ON} \cdot I^2_{OUT}$$

ON state energy loss [J]:

$$W_{RON} = P_{ON} \cdot t_{ON}$$

where t_{ON} = ON state duration

Example 2: For VND7020AJ

Figure 47. Steady state condition, datasheet values I_{OUT} = 3 A, R_{ON} at 150 ºC = 44 mΩ

R_{ON}	ON-state resistance	I_{OUT} = 3 A; T_j = 25 °C		22		mΩ
		I_{OUT} = 3 A; T_j = 150 °C			44	
		I_{OUT} = 3 A; V_{CC} = 4 V; T_j = 25 °C			30	

$$P_{ON} = R_{ON} \cdot I^2_{OUT} = 44m\Omega \cdot 3A^2 = 396mW$$

The R_{ON} parameter depends mainly on temperature (see measurement on *Figure 48*). This should be taken into account during the calculations.

In most cases, it is not necessary to consider the dependency on V_{CC} or I_{OUT}. The R_{ON} is almost independent of V_{CC} down to ~4 V (see *Figure 49*) and almost independent of I_{OUT} for a Drain Source voltage range above the output voltage drop limitation (given in the datasheet as V_{ON} = 20 mV typical - see *Figure 49*).

Figure 48. R_{ON} dependency on temperature (measured on a VND7140AJ sample)

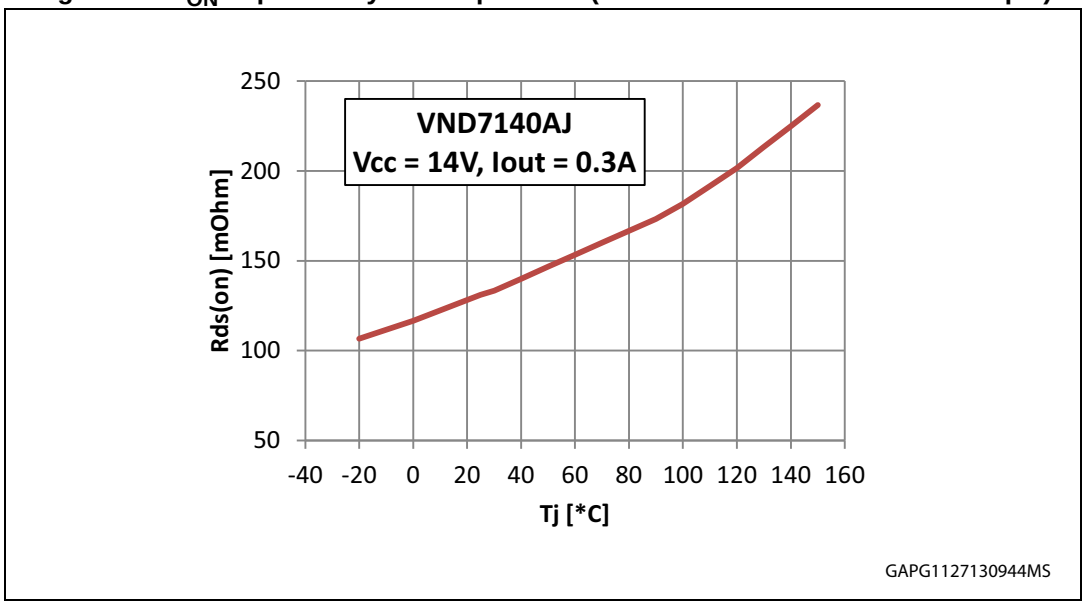
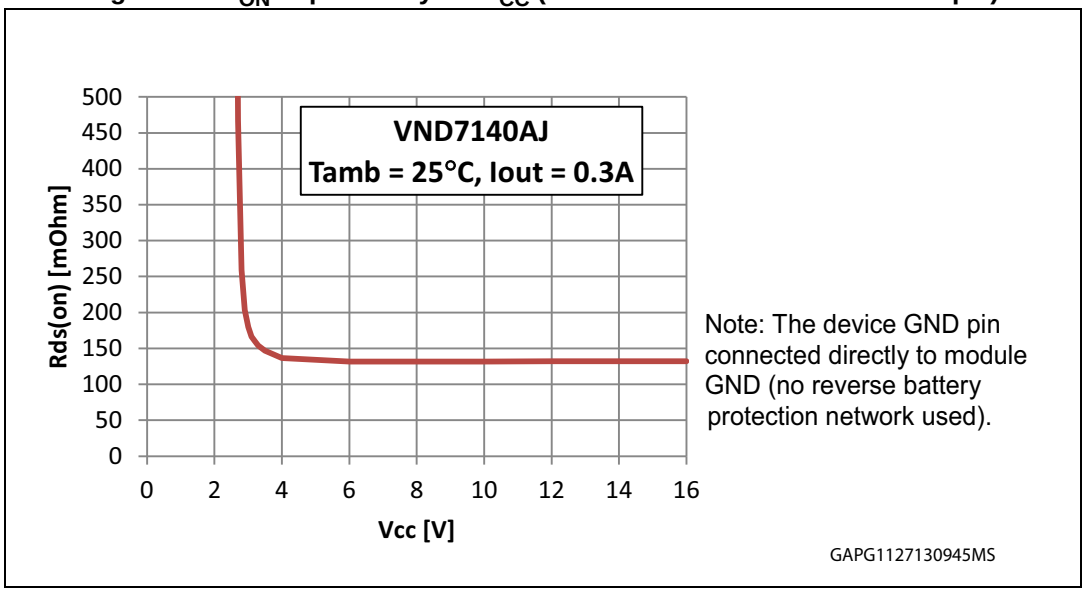
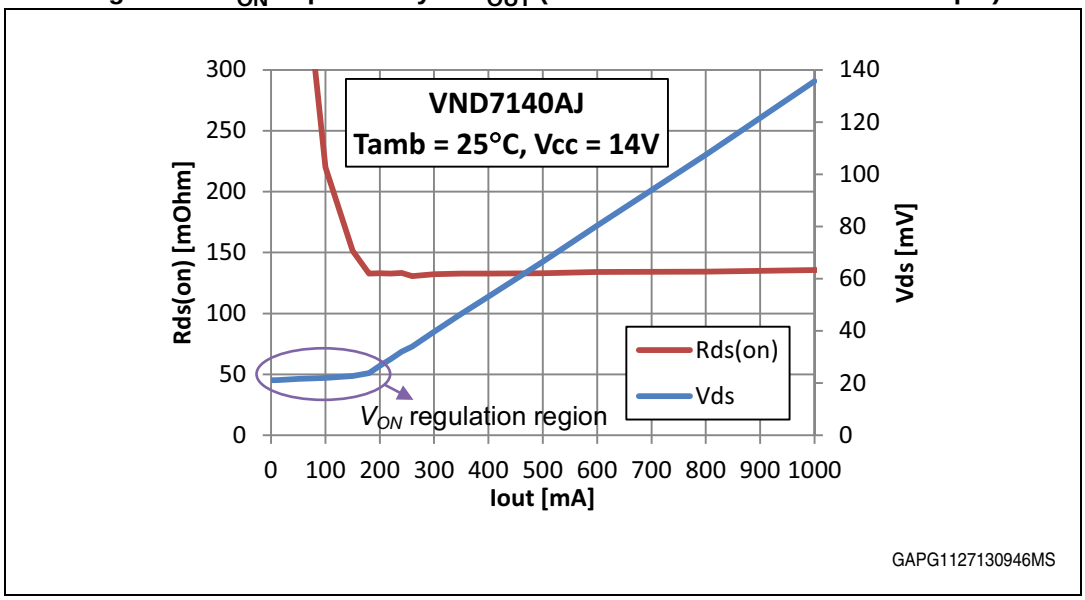


Figure 49. R_{ON} dependency on V_{CC} (measured on a VND7140AJ sample)



Note: The device GND pin connected directly to module GND (no reverse battery protection network used).

Figure 50. R_{ON} dependency on I_{OUT} (measured on a VND7140AJ sample)



The calculation of conduction losses in PWM mode is based on similar consideration as in case of steady state losses (focusing on R_{ON}, I_{OUT}, t_{on}), however it is important to consider right PWM on time (corrected with the turn-on/off switching delays and switching times) and right current in on state (for instance in case of bulb it depends on actual duty cycle):

Corrected duty cycle [-]:

$$D_{COR} = D - \frac{t_{dON} - t_{dOFF} - t_{WON}}{t_{period}}$$

where:

$$D = \frac{t_{IN\_high}}{t_{period}} \text{ [-]}$$

Duty cycle applied on input pin

$$\frac{t_{dON}}{t_{dOFF}} \text{ [s]}$$

Turn on/off delay time

$$t_{won\ [s]}$$

Turn on switching time

ON state power dissipation [W]

$$P_{ON} = R_{ON} \cdot I^2_{OUT(ON)}$$

Note: In case of bulb, the load current in on state depends on actual duty cycle.

Average power dissipation: [W]:

$$P_{AVG} = P_{ON} \cdot D_{COR}$$

6.2.2 Switching losses

The switching losses are important especially in PWM operation. Compared to conduction losses, the calculation depends on many factors like the load characteristic (resistive, capacitive or inductive), device characteristics (switching times) and environmental conditions (ambient, temperature, battery voltage).

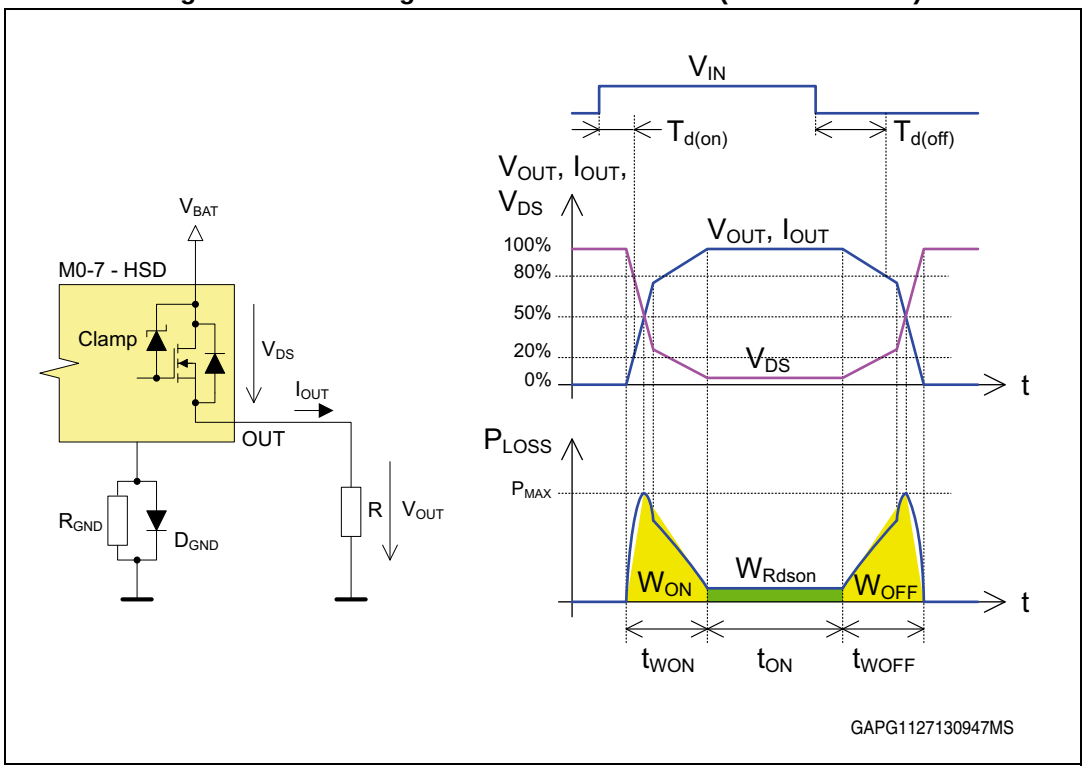
The switching shapes of M0-7 devices are optimized to fulfill the EMC requirements with minimum switching losses. Moreover, the turn-on and turn-off shapes are symmetrical to ensure minimum duty cycle error.

Switching losses-resistive loads, bulbs

This sub chapter deals with all kind of loads with resistive character (such as bulbs, heating elements etc.). The inductivity of wire harness is neglected (< 5 µH considered). The next calculations are simplified assuming constant resistance of the load. However, it is applicable also for non-linear resistive loads (bulbs) driven in PWM mode. The PWM frequency is usually high enough (>50 Hz) to minimize the filament temperature (resistance) variation over the PWM period so it behaves like constant resistor.

The instantaneous power dissipation in the switch during the switching phase is equal to drain to source voltage (V_{DS}) multiplied by the output (load) current (I_{OUT}). With given switching shapes and resistive load, the instantaneous power dissipation can be approximated by triangular waveform (see yellow area on *Figure 51*).

Figure 51. Switching and conduction losses (resistive loads)



Considering resistive load, the maximum instantaneous power dissipation occurs at half of the nominal output voltage and half of the nominal load current. It is the point where the switch resistance matches the load resistance (maximum power transfer theorem, impedance matching).

Peak power dissipation [W]:

$$P_{MAX} = \frac{V_{OUT}}{2} \cdot \frac{I_{OUT}}{2} \approx \frac{V_{BAT}}{2} \cdot \frac{V_{BAT}}{2 \cdot R} = \frac{V_{BAT}^2}{4 \cdot R}$$

Turn-on (Turn-off) energy loss [J]:

$$W_{ON} = W_{OFF} = \frac{1}{6} \cdot \frac{V_{BAT}^2}{R} \cdot t_{WON} \qquad (t_{WON} = t_{WOFF})$$

Note: Linear shape of the switching phase and symmetrical turn-on/off shapes considered

Same calculations are applicable also on the bulb in PWM mode. If the PWM frequency is high enough (> 50 Hz) the filament temperature (resistance) variation over the PWM period is negligible so it behaves like constant resistor.

Note: Typical and maximum switching losses on nominal resistive loads are specified in the datasheet with parameters W_{ON} and W_{OFF} (considering V_{CC} = 13 V, -40 °C < T_j < 150 °C). The switching losses vary with battery voltage. If we suppose constant switching times at varying the battery voltage, this yields:

$$W_{ONatVBAT2} = W_{ONatVBAT1} \cdot \frac{P_{LOADatVBAT2}}{P_{LOADatVBAT1}}$$

$$W_{OFFatVBAT2} = W_{OFFatVBAT1} \cdot \frac{P_{LOADatVBAT2}}{P_{LOADatVBAT1}}$$

Experimental measurements on M0-7 HSDs have highlighted that switching times are slightly decreasing with increasing V_{CC} so the above formulas are approximated.

Calculation example: VND7040AJ

- Load: 4.5 Ω resistor
- V_{BAT}: 16 V
- t_{WON}, t_{WOFF}: 60 µs → this parameter is not explicitly specified in the datasheet. The value can be obtained by the measurement (this case) or estimated from dV_{OUT}/dt datasheet parameter
- Requirement: driver must not run into thermal shutdown

Peak power dissipation [W]:

$$P_{MAX} = \frac{V_{BAT}^2}{4 \cdot R} = \frac{16V^2}{4 \cdot 4.5\Omega} = 14.2W$$

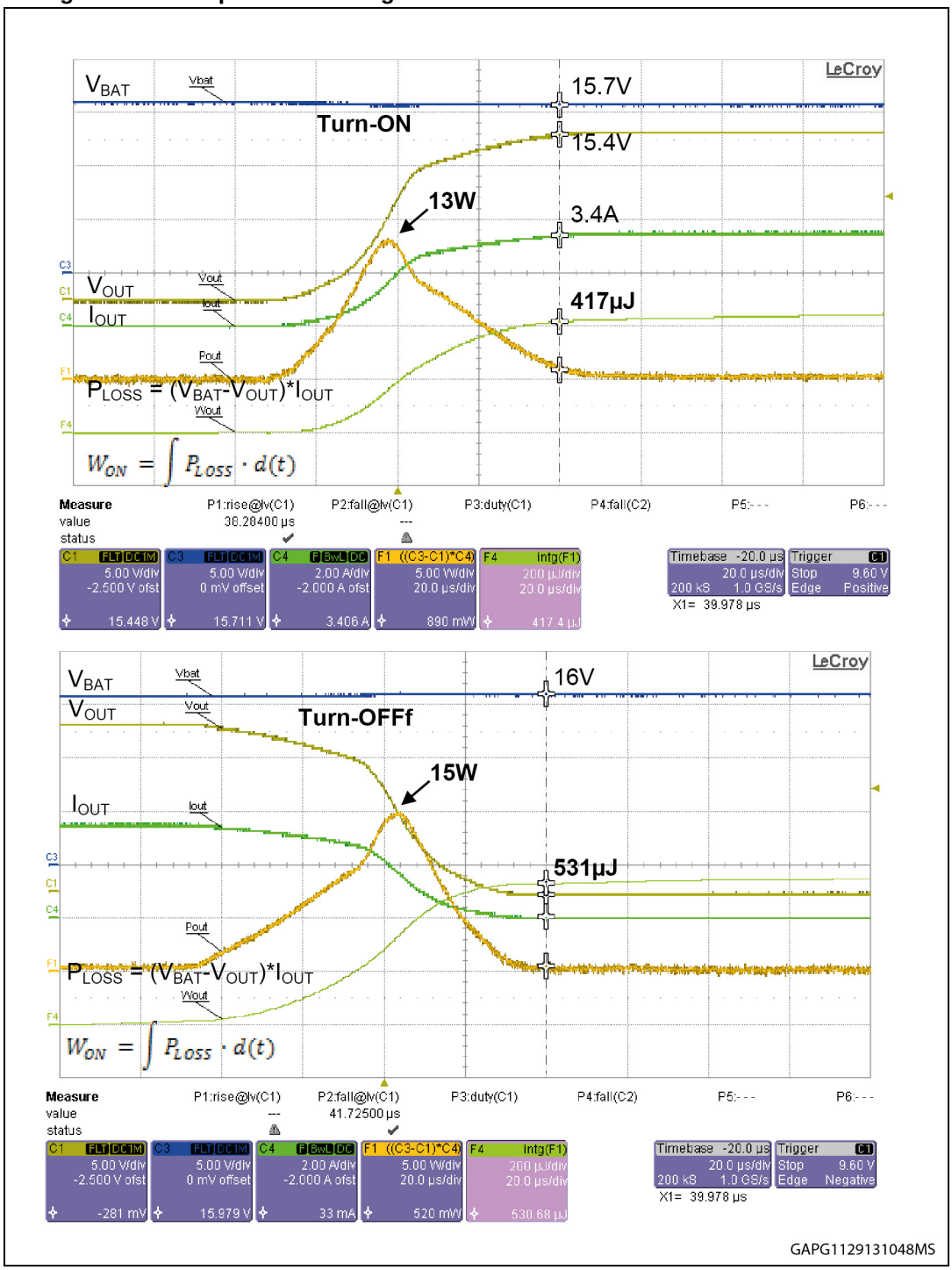
Turn-on/Turn-off energy loss [J]:

$$W_{ON} = W_{OFF} = \frac{1}{6} \cdot \frac{16V^2}{4.5\Omega} = 60\mu s = 569\mu J$$

Switching losses measurement–comparison with calculation

The switching losses in the HSD are measured by an oscilloscope with mathematical functions. The first function F1 shows the actual power dissipation on the HSD $(V_{BAT} - V_{OUT}) * I_{OUT}$, the second function F4 shows the HSD energy (integral of F1).

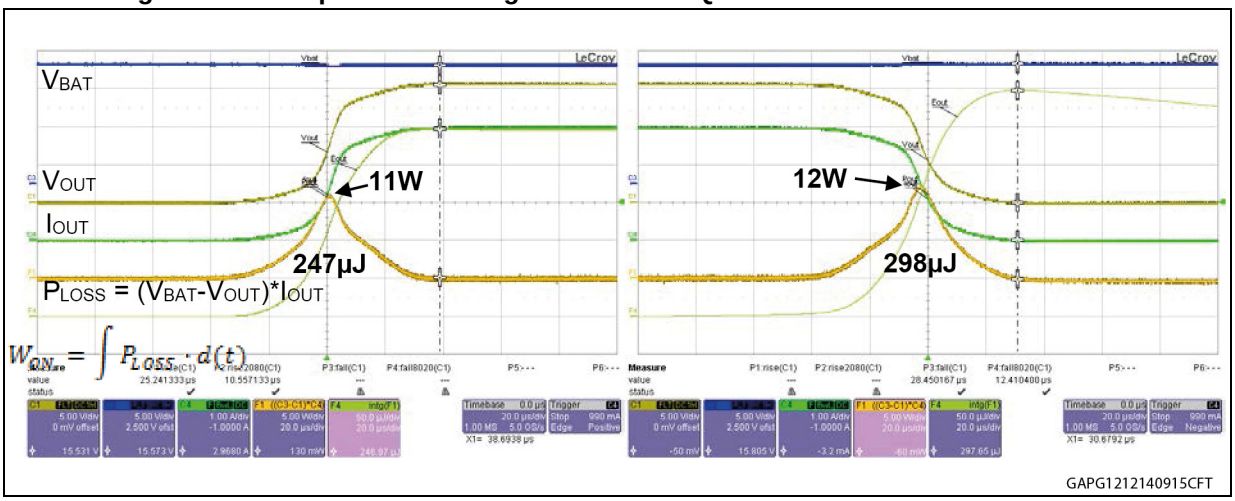
Figure 52. Example of switching losses on VND7040AJ with 4.5Ω resistive load



As seen from the measurement, in this case the switching shapes are not absolutely symmetrical so the turn-off loss is slightly higher (531 µJ turn-off versus 417 µJ turn-on). Measured values are slightly below the calculated value (569 µJ).

Another measurement example shows switching shapes and losses of VNQ7040AY on channel 0 configured in bulb mode, V_{BAT} = 16 V, Temperature = 25 ºC, resistive load 5.2Ω:

Figure 53. Example of switching losses on VNQ7040AY with 5.2 Ω resistive load



Switching losses - LED clusters

The switching losses evaluation in combination with LED loads is a much more complex task compared with resistive loads. Since there are many different types of the LED string, it is almost impossible to cover all cases with one general calculation formula (like in case of resistive loads). Exact calculation is problematic even for specific LED load (with known behavior) due to its non-linear V/A characteristic (see examples in the next figures). Therefore, it is usually more efficient to do the estimation only or switching losses measurement as shown in this chapter.

Figure 54. LED cluster example 1–LED test board (6 x 3 LEDs OSRAM LA E67-4)

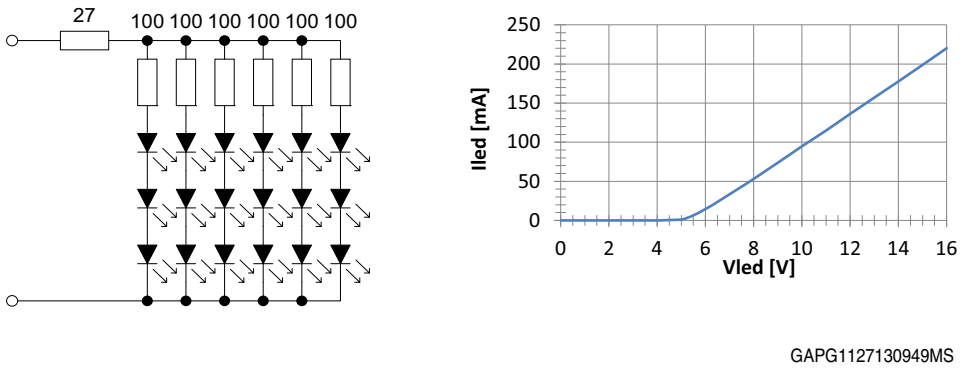
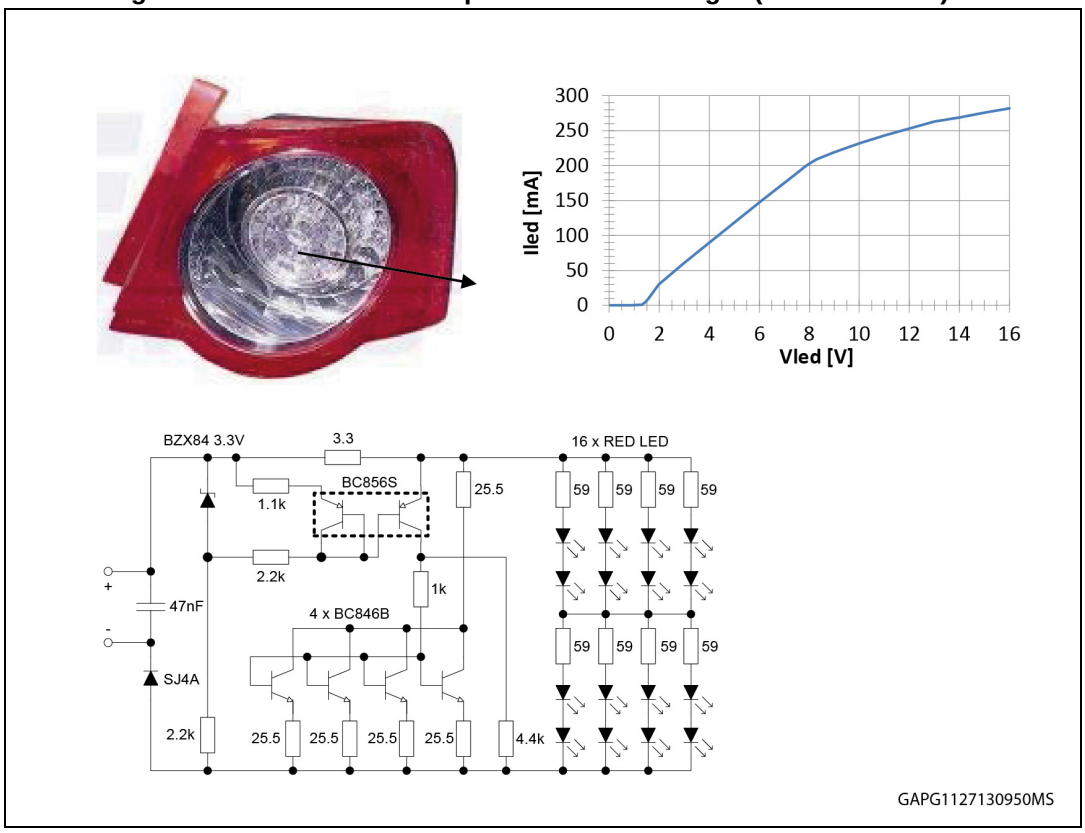


Figure 55. LED cluster example 2–tail & brake light (VW Passat B6)



The first example shows a simple LED cluster with serial-parallel combination of LEDs and resistors. In the second example there is a schematic and V/A characteristic measured on a real LED lamp (VW Passat B6). As seen on schematic, on top of the serial-parallel LED/resistor strings there is a reverse battery protection diode, ESD capacitor on input terminal and “dummy load” circuitry with bipolar transistors. This circuitry is used to adapt the LED string behavior (V/A characteristic) according to diagnostic requirements (open load in on-state, open load in off-state).

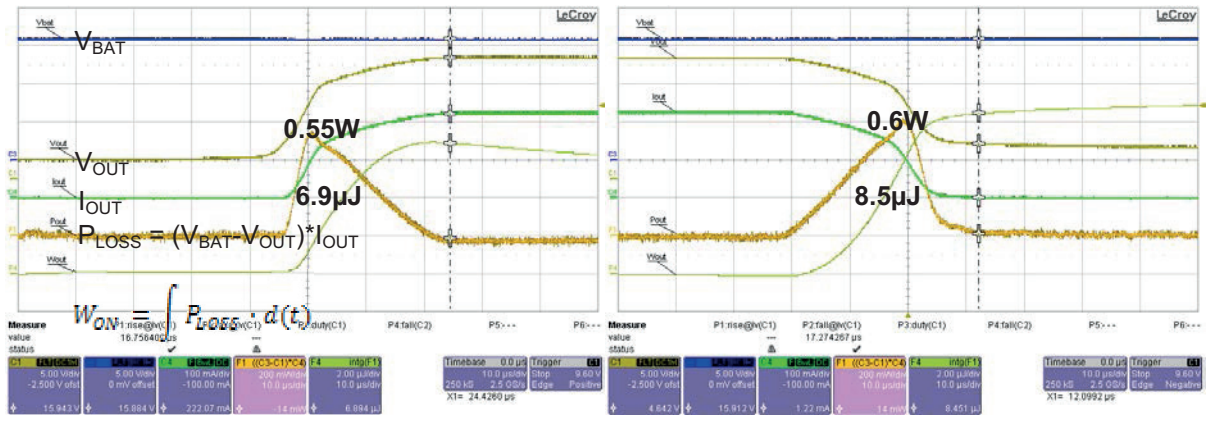
Example 1: Switching losses–measurement

The following example shows the switching losses measurement on VND7140AJ with LED cluster example 1 (LED test board - 6 x 3 LEDs OSRAM LA E67-4) using an oscilloscope with mathematical functions. The first function F1 shows the actual power dissipation on the HSD (V_{BAT} - V_{OUT}) * I_{OUT}, the second function F4 shows the HSD energy (integral of F1).

Conditions:

- V_{BAT}: 16 V
- Temperature: 23 °C
- PWM: 200 Hz, 70 %
- Load: test board with 6 x 3 LED OSRAM LA E67-4 (see *Figure 54*)
- Device: VND7140AJ

Figure 56. Slew rate and switching losses (VND7140AJ, LED test board)



Measured losses: W_{ON} ~ 6.9 µJ, W_{OFF} ~ 8.5 µJ

Contribution to total average power dissipation:

$$P_{SW} = \frac{W_{ON} + W_{OFF}}{T_{PWM}} = \frac{6.9\mu J + 8.5\mu J}{\frac{1}{200Hz}} = 3.1mW$$

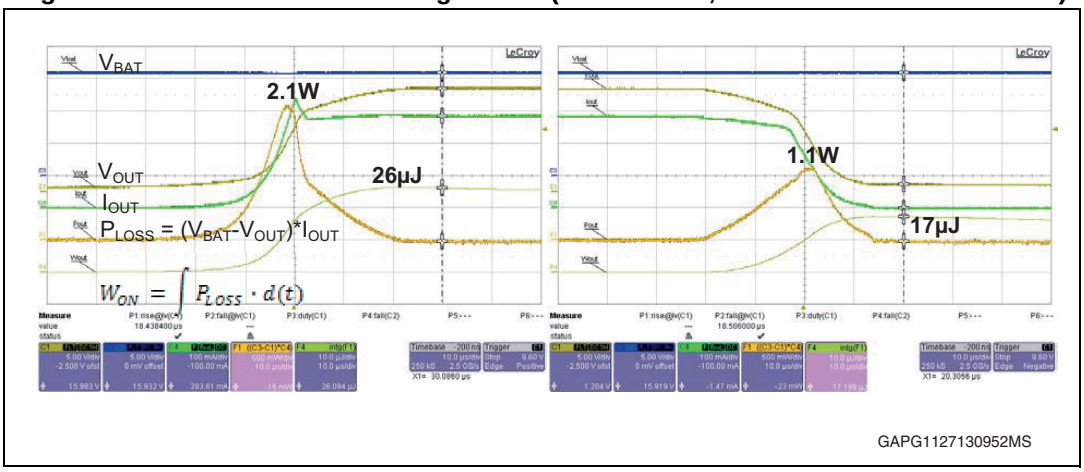
Example 2: Switching losses – measurement

This example shows the switching losses measurement on VND7140AJ with LED cluster example 2 (VW Passat B6–tail & brake light) using an oscilloscope with mathematical functions. The first function F1 shows the actual power dissipation on the HSD (V_{BAT} - V_{OUT}) * I_{OUT}, the second function F4 shows the HSD energy (integral of F1).

Conditions:

- V_{BAT}: 16 V
- Temperature: 23 °C
- PWM: 200 Hz, 70 %
- Load: VW Passat B6 – Tail & Brake (see *Figure 55*)
- Device: VND7140AJ

Figure 57. Slew rate and switching losses (VND7140AJ, VW Passat B6–tail & brake)



Measured losses: W_{ON} ~ 26 µJ, W_{OFF} ~ 17 µJ

Contribution to total average power dissipation:

$$P_{SW} = \frac{W_{ON} + W_{OFF}}{T_{PWM}} = \frac{26\mu J + 17\mu J}{\frac{1}{200Hz}} = 8.6mW$$

Switching losses - inductive loads

A typical characteristic of inductive loads is the tendency to maintain the direction and value of the actual current flow. Applying nominal voltage on inactive load (turn-on), it takes a certain time (depending on time constant τ = L/R) to reach nominal current. Removing the voltage source from the active load (turn-off), the load inductance tends to continue to drive the current via any available path (i.e. clamp of the HSD) by reversing its voltage (acts as a source) until the stored energy (E_L=1/2 L I_0^2) is dissipated. Time needed to dissipate this energy is called demagnetization time (T_{DEMAG}). This time is strongly dependent on the voltage across the load (V_{DEMAG}) at which the demagnetization is performed (higher $|V_{DEMAG}| \rightarrow$ shorter T_{DEMAG}). A typical V_{DEMAG} for M0-7 devices is equal to V_{CC} – 46 V.

Corresponding T_{DEMAG} can be calculated as $T_{DEMAG} = \frac{L}{R} \cdot \ln\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}$

(neglecting the turn-off switching time of the HSD) where L = load inductance; R = load resistance and I_0 = load current at the beginning of turn-off event.

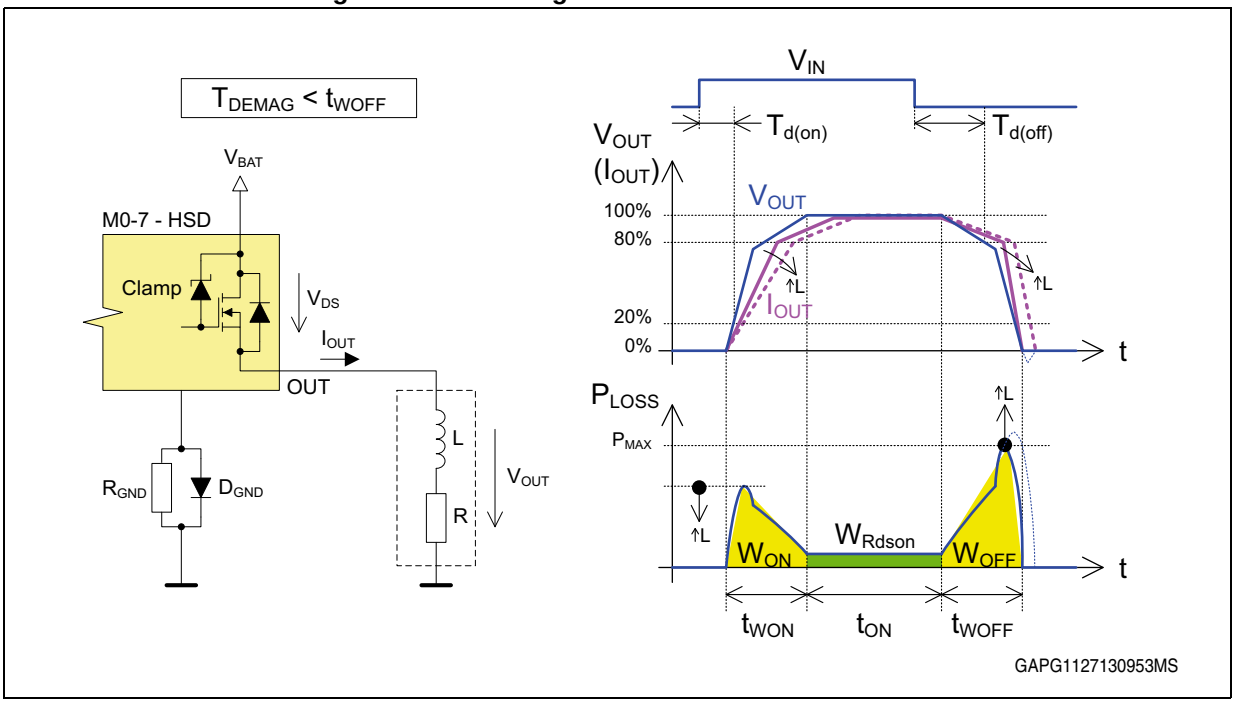
From these considerations it is obvious that instant power dissipation and switching losses in the HSD are usually higher at turn-off phase. Since the HSD output behavior (voltage/current waveforms) depends on several factors (mainly on the ratio between the demagnetization time and turn-off switching time t_{WOFF}), the next analysis of switching losses is divided into the following parts:

- Low inductance ($T_{DEMAG} < t_{WOFF}$)
- High inductance ($T_{DEMAG} > t_{WOFF}$)
- High inductance ($T_{DEMAG} > t_{WOFF}$) with external freewheeling diode
  - Steady state operation (single turn-on / turn-off)
  - PWM operation

Low inductance (T_{DEMAG} < t_{WOFF})

If the load inductance is relatively low (so the stored energy is dissipated within the HSD turn-off time t_{WOFF}), the output voltage decays down to 0 (or slightly in negative) without the activation of the output clamp (see *Figure 58*).

Figure 58. Switching losses with low inductance



In this case, the switching losses can be roughly estimated from equivalent losses with pure resistive load (see calculation in previous chapter). Since the output current is delayed from the output voltage, the losses at turn-on phase (W_{ON}) will be lower, while the losses at turn-off phase (W_{OFF}) will be higher (up to factor of 5) in comparison with pure resistive load. This factor was found experimentally in condition when the demagnetization time (T_{DEMAG}) is matching with turn-off switching time (t_{WOFF}).

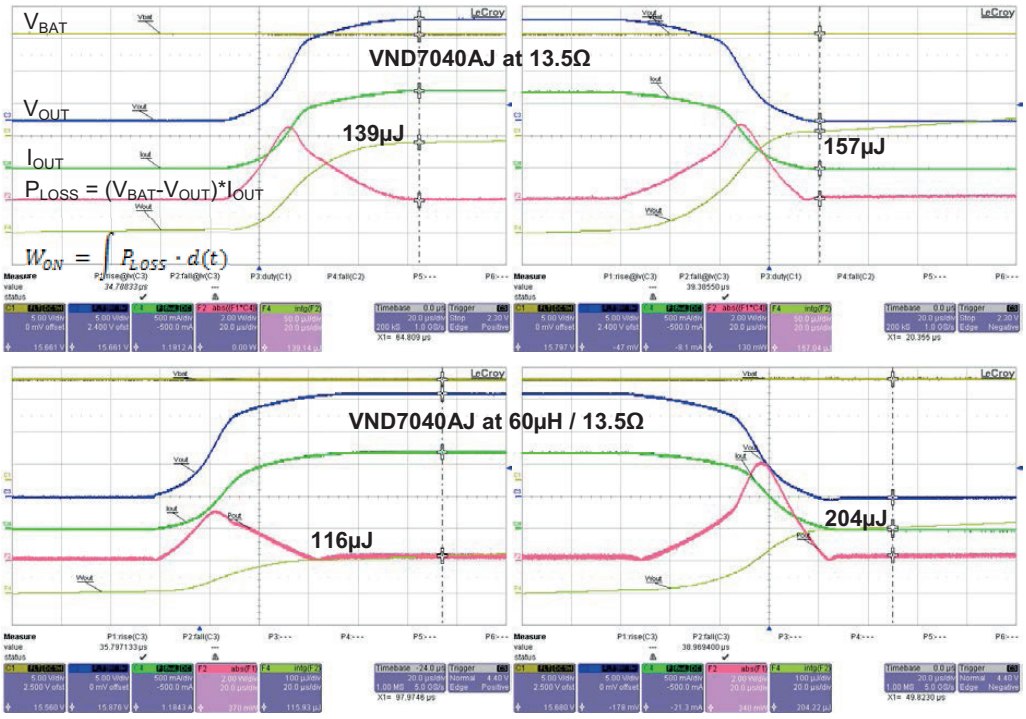
Measurement example – Low inductance (T_{DEMAG} < t_{WOFF})

This measurement example compares the switching losses in the VND7040AJ with two different loads – pure resistive 13.5 Ω and 60 µH at 13.5 Ω.

Conditions:

- V_{BAT}: 16 V
- Temperature: 23 °C
- PWM: 200 Hz, 70 %
- Load: 13.5 Ω; 60 µH at 13.5 Ω (calculated T_{DEMAG} = 1.9 µs)
- Device: VND7040AJ

Figure 59. Low inductance (T_{DEMAG} << t_{WOFF}) – measurement example

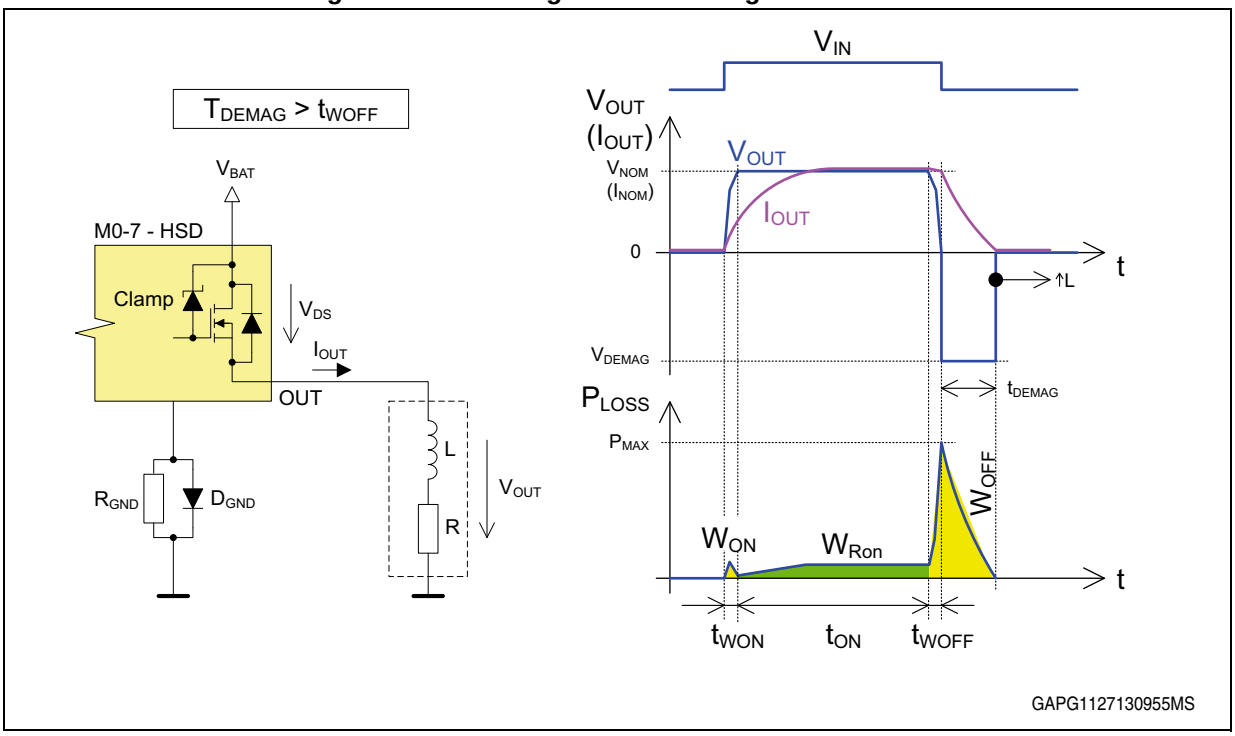


Measured losses (pure resistive 13.5 Ω): W_{ON} ~ 139 µJ, W_{OFF} ~ 157 µJ
Measured losses (60 µH at 13.5 Ω): W_{ON} ~ 116 µJ, W_{OFF} ~ 204 µJ
W_{ON} ratio (60 µH versus pure resistive): 116 / 139 = 0.83x
W_{OFF} ratio (60 µH versus pure resistive): 204 / 157 = 1.30x

High inductance (T_{DEMAG} > t_{WOFF})

If the load inductance is relatively high (so the time needed for the load demagnetization is much higher than the HSD turn-off time t_{WOFF}), the output voltage at turn-off phase is forced negative so the load current continues via the HSD output clamp (see *Figure 60*).

Figure 60. Switching losses with high inductance



The above example explains a single turn-on / turn-off event. This means that zero load current is considered at the beginning of turn-on phase and nominal load current is considered at the beginning of turn-off phase.

Assuming $T_{DEMAG} >> t_{WOFF}$, the switching losses can be calculated as follows:

Turn-on energy loss [J]:

$$W_{ON} \approx 0$$

Turn-off energy loss [J]:

$$W_{OFF} = \frac{|V_{DEMAG}| + V_{BAT}}{R^2} \cdot L \cdot \left(R \cdot I_0 - |V_{DEMAG}| \cdot \ln \frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right)$$

(Losses during transition phases t_{WON} and t_{WOFF} neglected)

Calculation example (single turn-on / off event):

- Load: 20 mH at 13.5 Ω
- V_{BAT}: 16 V
- V_{DEMAG}: -30 V (V_{BAT} – 46)
- I_0: 1.185 A (V_{BAT} / 13.5 Ω)

$$T_{DEMAG} = \frac{L}{R} \cdot \ln \frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} = \frac{0.02}{13.5} \cdot \ln \frac{|-30| + 1.185 \cdot 13.5}{|-30|} = 633\mu s$$

$W_{ON} \approx 0$ ($T_{DEMAG} >> T_{WON} \rightarrow$ 633 µs >> ~60 µs → condition fulfilled)

$$W_{OFF} = \frac{|V_{DEMAG}| + V_{BAT}}{R^2} \cdot L \cdot \left(R \cdot I_0 - |V_{DEMAG}| \cdot \ln \frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right) =$$

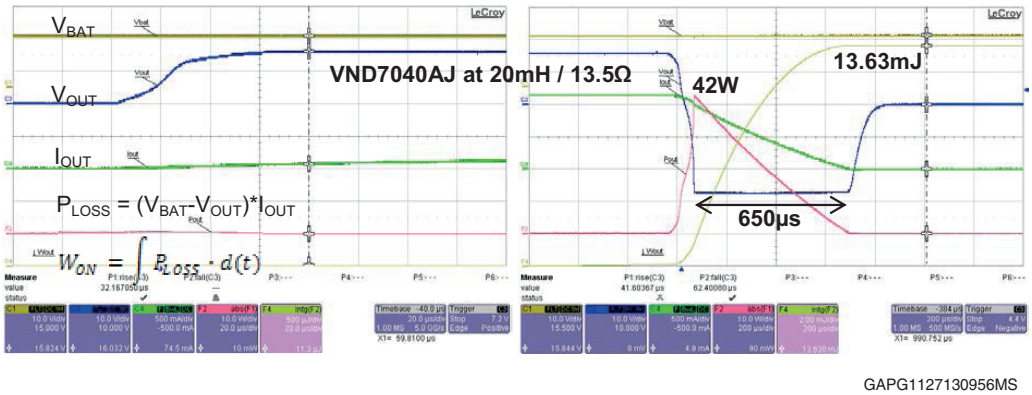
$$= \frac{|-30| + 16}{13.5^2} \cdot 0.02 \cdot \left(13.5 \cdot 1.185 - |-30| \cdot \ln \frac{|-30| + 1.185 \cdot 13.5}{|-30|} \right) = 16\text{mJ}$$

Measurement example, comparison with calculation – high inductance (T_{DEMAG} > t_{WOFF})

Conditions:

- V_{BAT}: 16 V
- Temperature: 23 °C
- Load: 20 mH at 13.5 Ω
- Device: VND7040AJ

Figure 61. High inductance (T_{DEMAG} >> t_{WOFF}) – measurement example



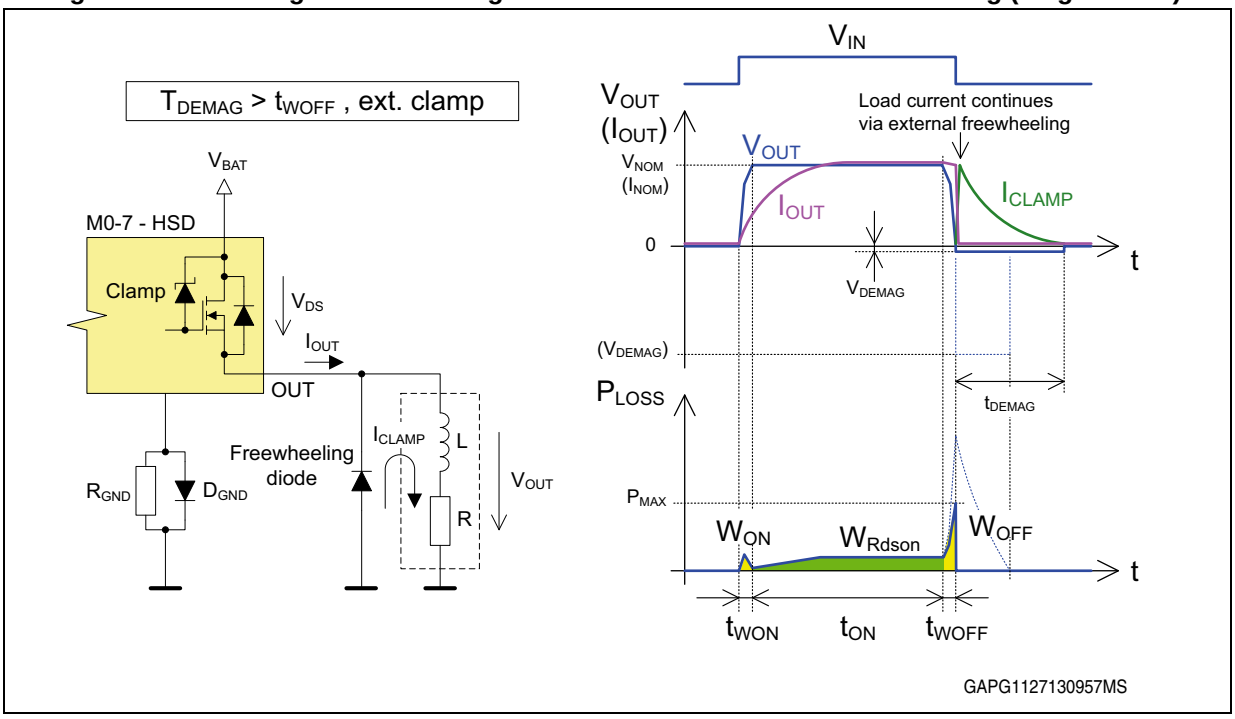
Measured T_{DEMAG}: 6500 µs (633 µs calculated)
Measured W_{ON}: 11 µJ (0 estimated)
Measured W_{OFF}: 13.63 mJ (16 mJ calculated)
Measured losses (pure resistive 13.5 Ω): W_{ON} ~ 139 µJ, W_{OFF} ~ 157 µJ
W_{ON} ratio (20 mH versus pure resistive): 11/139 = 0.08x
W_{OFF} ratio (20 mH versus pure resistive): 13630/157 = 86.8x

The measured values correspond to theoretical assumptions and calculations:

High inductance (T_{DEMAG} > t_{WOFF}) with external freewheeling diode

An external clamping circuitry (i.e. freewheeling diode) is usually used to protect the HSD in case the demagnetization energy is exceeding the energy capability of a given HSD. By using a standard freewheeling diode, the demagnetization voltage is reduced from –32 V (a typical V_{DEMAG} of M0-7 device at V_{BAT} = 14 V) to approximately –1 V (depending on forward voltage of the diode - see *Figure 62*). This has an influence to the demagnetization time (lowering $|V_{DEMAG}|$ → increasing T_{DEMAG}), as can be derived from the T_{DEMAG} equation.

Figure 62. Switching losses with high inductance and external freewheeling (single event)



The above example explains a single turn-on / turn-off event. This means that zero load current is considered at the beginning of turn-on phase and nominal load current is considered at the beginning of turn-off phase.

Assuming $T_{DEMAG} >> t_{WOFF}$, the switching losses can be estimated as follows:

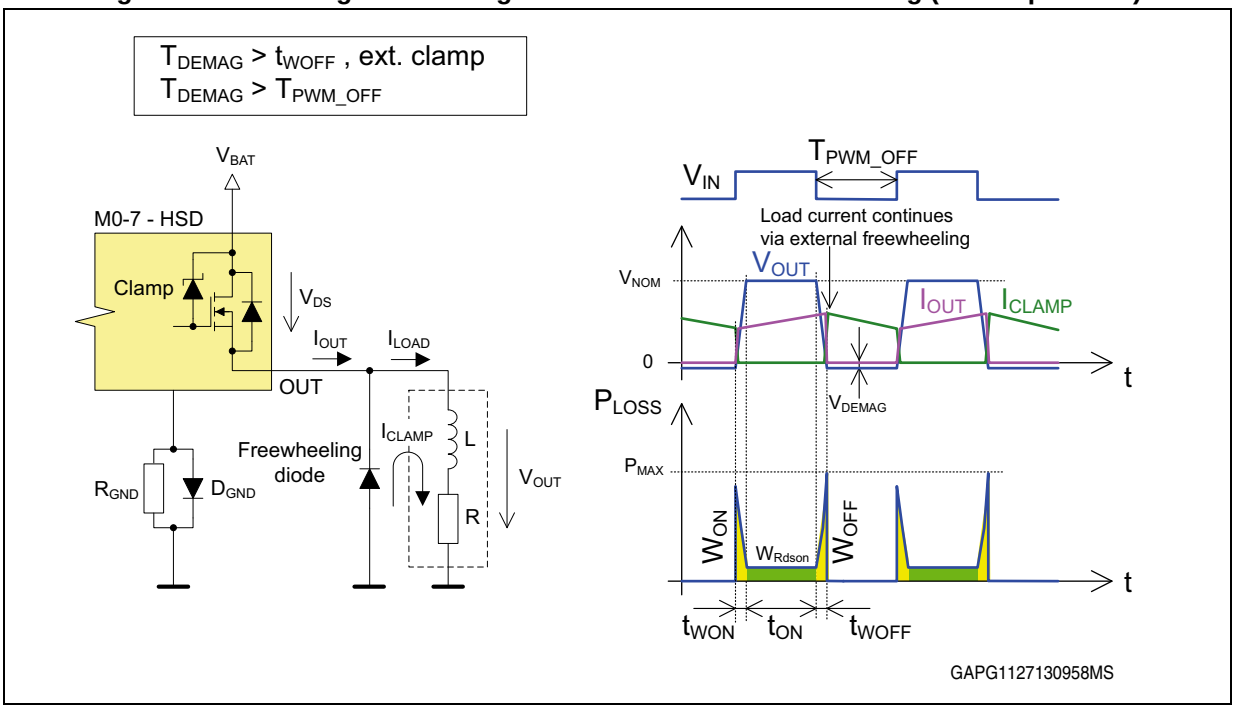
Turn-on energy loss [J]: $W_{ON} \sim 0$

Turn-off energy loss [J]: W_{OFF} 3x higher versus pure resistive load

Note: The factor 3 is the result of experiment (see Table 21 and Table 22)

In PWM operation (or at turn-on with a small delay after the last turn-off) there is a possibility that the turn-on event comes before the end of the demagnetization phase (if the PWM off-state time is shorter that the load demagnetization time: ($T_{DEMAG} > T_{PWM\_OFF}$). This means that turn-on phase is starting while the current is still forced via the freewheeling diode. This makes the turn-on switching loss significant if compared with the case of zero starting current. As a rough estimation a ~3x higher value can be considered versus equivalent resistive load. This way of the operation is frequently used on purpose – i.e. for the load current regulation by PWM duty cycle (see *Figure 63*).

Figure 63. Switching losses – high inductance + ext. freewheeling (PWM operation)



Assuming T_{DEMAG} >> T_{PWM_OFF}, the switching losses can be estimated as follows:

V_{BAT}: 16 V

Temperature: 23 °C

Turn-on energy loss [J]: W_{ON} ~3x higher versus equivalent resistive load

Turn-off energy loss [J]: W_{OFF} ~3x higher versus equivalent resistive load

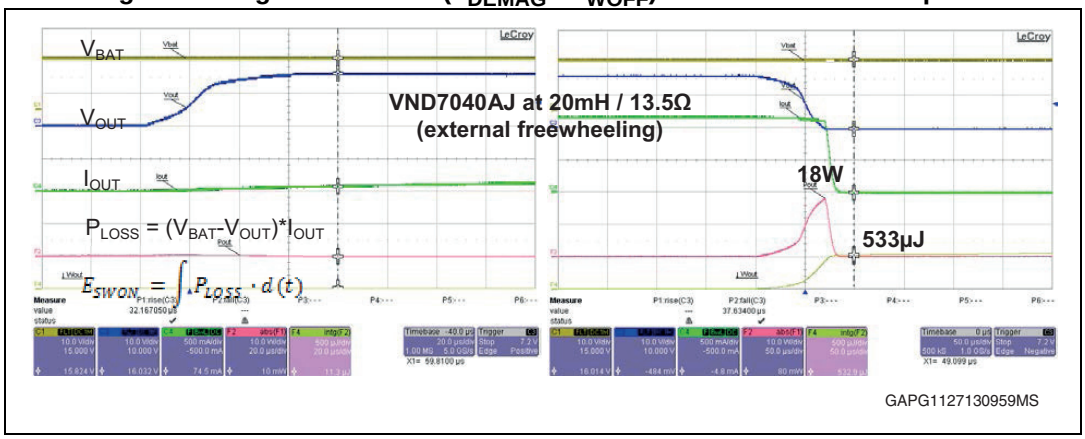
Note: The factor 3 is the result of experiment (see Table 21 and Table 22)

Measurement example 1 – high inductance with external freewheeling (single event)

Conditions:

- V_{BAT}: 16 V
- Temperature: 23 °C
- Load: 20 mH at 13.5 Ω
- External freewheeling diode: STPS2H100
- Device: VND7040AJ

Figure 64. High inductance (T_{DEMAG} > t_{WOFF}): measurement example 1



Measured losses (20 mH at 13.5 Ω): W_{ON} ~ 11 µJ, W_{OFF} ~ 533 µJ
Measured losses (pure resistive 13.5 Ω): W_{ON} ~ 139 µJ, W_{OFF} ~ 157 µJ
W_{ON} ratio (20 mH versus pure resistive): 11 / 139 = 0.08x
W_{OFF} ratio (20 mH versus pure resistive): 533 / 157 = 3.39x

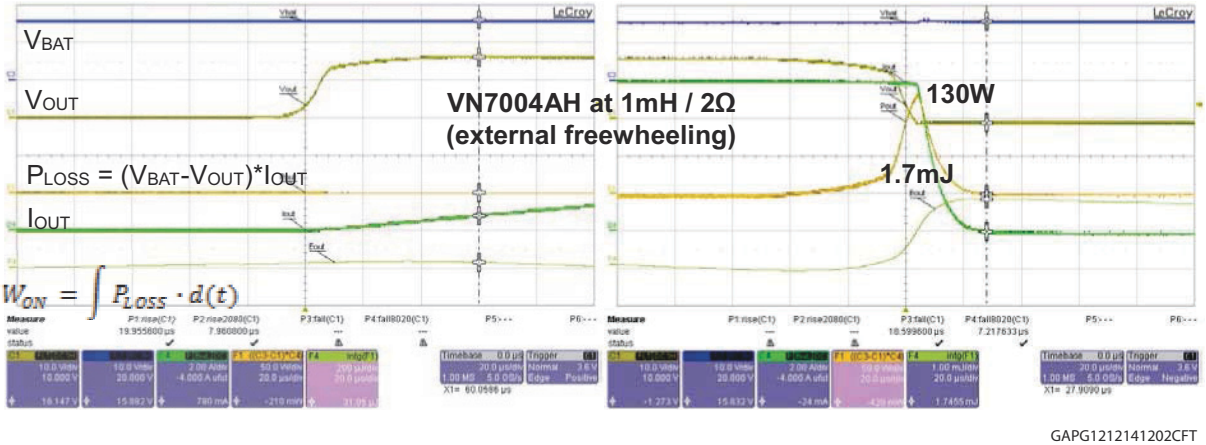
The measured values confirm that the turn-on switching loss is negligible (zero starting current) while the turn-off switching loss is ~3x higher in comparison with pure resistive load.

Measurement example 2 – High inductance with external freewheeling (single event)

Conditions

- V_{BAT}: 16 V
- Temperature: 23 °C
- Load: 1 mH at 2 Ω
- External freewheeling diode: STPS2H100
- Device: VN7004AH-E

Figure 65. Figure 62: High inductance (T_{DEMAG} > t_{WOFF}) – measurement example 2



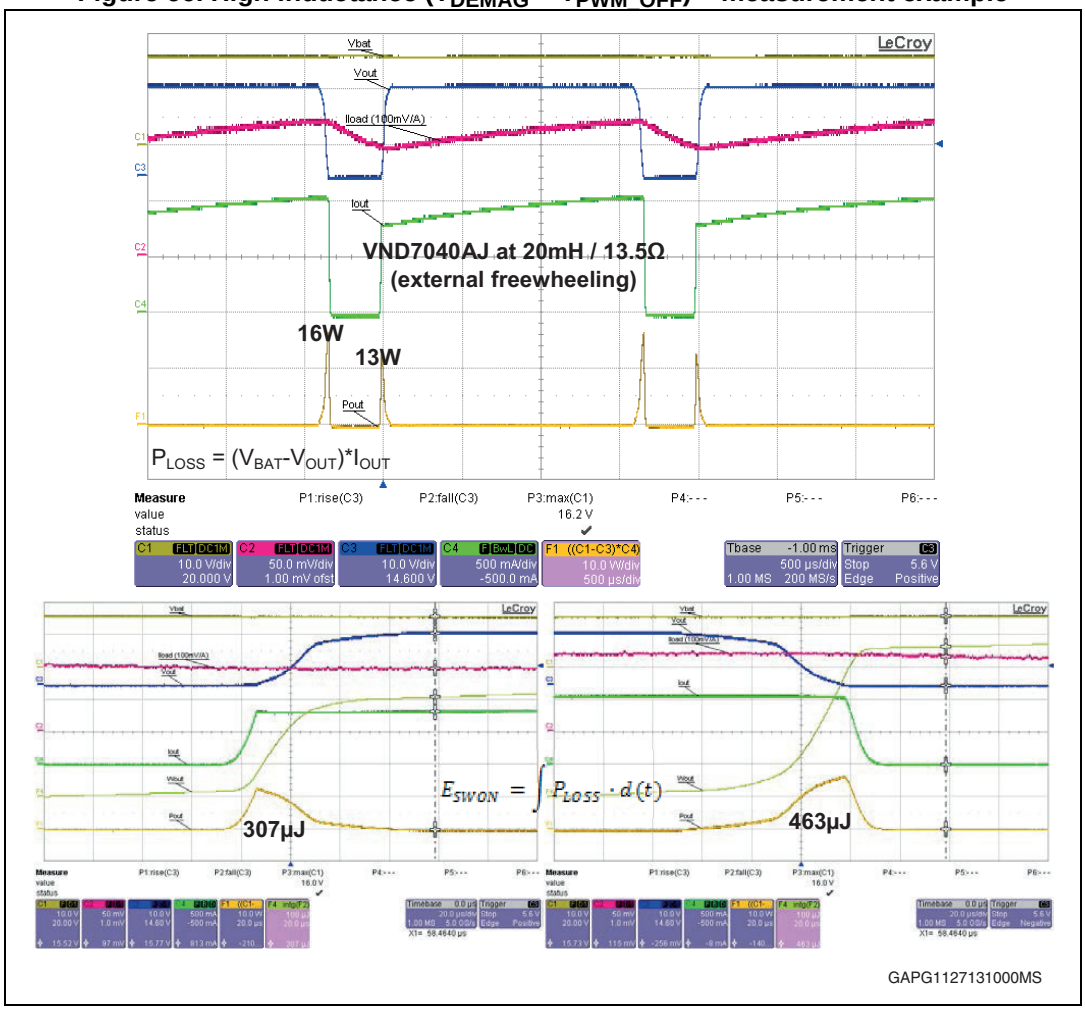
Measured losses (1 mH at 2 Ω): W_{ON} ~ 0.04 mJ, W_{OFF} ~ 1.75 mJ

Measurement example 3 – High inductance with external freewheeling (PWM operation)

Conditions:

- V_{BAT}: 16 V
- Temperature: 23 °C
- Load: 20 mH at 13.5 Ω
- External freewheeling diode: STPS2H100
- Device: VND7040AJ
- PWM: 80 % at 500 Hz

Figure 66. High inductance (T_{DEMAG} > T_{PWM_OFF}) – measurement example



Measured losses (20 mH at 13.5 Ω): W_{ON} ~ 307 µJ (I_{OUT} ~ 1 A)

W_{OFF} ~ 463 µJ (I_{OUT} ~ 1.2 A)

Measured losses (resistive 13.5 Ω): W_{ON} ~ 139 µJ (I_{OUT} = 1.2 A)

W_{OFF} ~ 157 µJ (I_{OUT} = 1.2 A)

W_{ON} ratio (20 mH versus resistive equivalent): $307/(139 * 1^2/1.2^2) = 3.18x$

W_{OFF} ratio (20 mH versus resistive equivalent): 463/157 = 2.95x

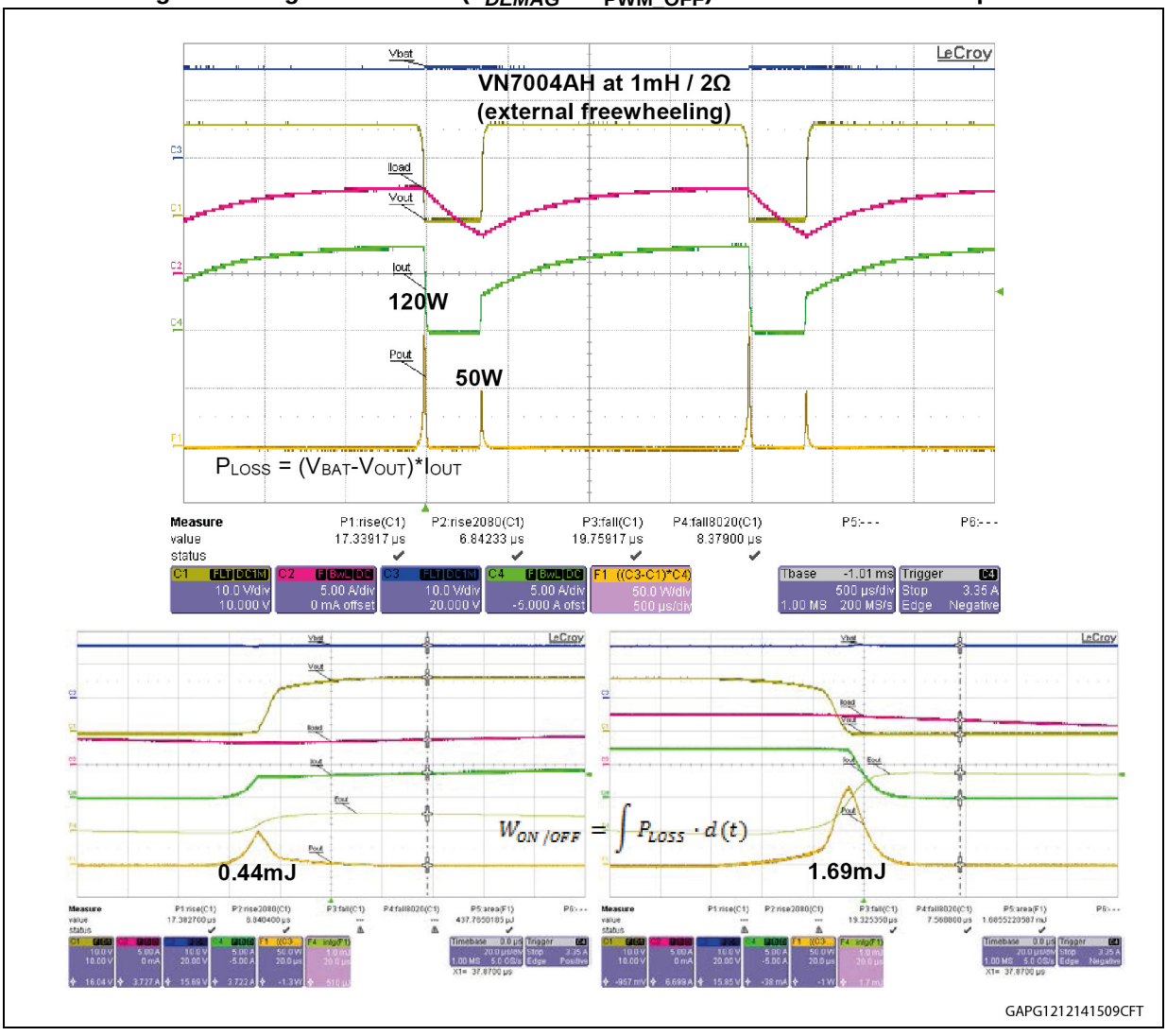
The measured values confirm that the turn-on and turn-off losses are ~3x higher in comparison with equivalent resistive load.

Measurement example 4 – High inductance with external freewheeling (PWM operation)

Conditions:

- V_{BAT}: 16 V
- Temperature: 23 °C
- Load: 1 mH at 2 Ω
- External freewheeling diode: STPS2H100
- Device: VN7004AH-E
- PWM: 80 % at 500 Hz

Figure 67. High inductance (T_{DEMAG} > T_{PWM_OFF}) – measurement example 4



Measured losses (1 mH at 2 Ω): W_{ON} ~ 0.44 mJ, W_{OFF} ~ 1.69 mJ

Measurement example – switching losses versus L (VND7040AJ)

In order to get a better idea about the switching losses dependency on the value of the inductance, a comparative measurement with different load inductances was performed on VND7040AJ. The summary of this measurement is shown in the tables below. The *Table 21* describes the steady state operation (single turn-on / off event), with or without an external freewheeling diode. For each load inductance, there is a measurement of switching losses and switching times (time between 10-90 % of nominal V_{OUT} considered). All switching losses are compared versus the resistive load. In the last column there is a calculation of demagnetization time (considering V_{DEMAG} = -28 V).

V_{BAT} = 16 V Single turn-on (I_{LOAD} = 0), single turn-off (I_{LOAD} = nominal = 1.2 A)

Table 21. VND7040AJ measurement of switching losses versus L in steady state

Load		W_{ON}		W_{OFF}		W_{OFF} (with external freewheeling)		t_{ON} [µs]	t_{OFF} [µs]	T_{DEMAG} (calculated)
L [µH]	R [Ω]	[µJ]	Ratio vs res. load	[µJ]	Ratio vs res. load	[µJ]	Ratio vs res. load	10-90% of V_{OUT}	90-10% of V_{OUT}	(at -28 V) [µs]
1.5	13.5	139	1.00 x	157	1.00 x	157	1.00 x	35	39	0.0
15	13.5	130	0.94 x	173	1.10 x	173	1.10 x	35	38	0.5
60	13.5	116	0.83 x	204	1.30 x	204	1.30 x	35	38	1.9
300	13.5	69	0.50 x	382	2.43 x	321	2.04 x	34	35	9.5
1 000	13.5	54	0.39 x	785	5.00 x	438	2.79 x	33	36	32
3 500	13.5	52	0.37 x	2 370	15.1 x	492	3.13 x	31	36	111
5 400	13.5	50	0.36 x	3 470	22.1 x	487	3.10 x	31	36	171
20 000	13.5	11	0.08 x	13 630	86.82 x	533	3.39 x	30	36	633

The *Table 22* describes the PWM operation with high duty cycle (shortest possible PWM off-time adjusted to have complete turn-off / on phase). The measurement was done with external freewheeling only (Schottky diode). In the last column there is a calculation of demagnetization time (considering V_{DEMAG} = -0.6 V).

V_{BAT} = 16 V PWM 94 % at 500 Hz (120 µs off-time) → shortest possible for complete turn-off/on phase

Table 22. VND7040AJ measurement of switching losses versus L in PWM mode (with external freewheeling)

Load		W_{ON} (with external freewheeling)		W_{OFF} (with external freewheeling)		t_{ON} [µs]	t_{OFF} [µs]	T_{DEMAG} (calculated)
L [µH]	R [Ω]	[µJ]	Ratio vs res. load	[µJ]	Ratio vs res. load	(10-90% of V_{OUT})	(90-10% of V_{OUT})	(at -0.6V) [µs]
1.5	13.5	139	1.00	157	1.00	35	39	0.0
15	13.5	130	0.94	173	1.10	35	38	4
60	13.5	118	0.85	205	1.31	35	38	15

Table 22. VND7040AJ measurement of switching losses versus L in PWM mode (with external freewheeling) (continued)

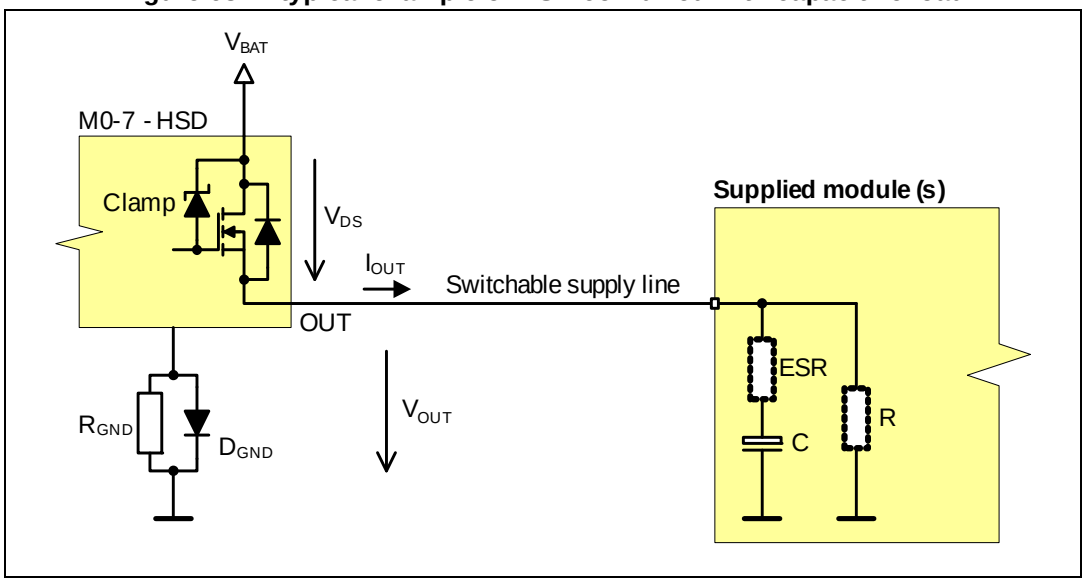
Load		W_{ON} (with external freewheeling)		W_{OFF} (with external freewheeling)		t_{ON} [µs]	t_{OFF} [µs]	T_{DEMAG} (calculated)
L [µH]	R [Ω]	[µJ]	Ratio vs res. load	[µJ]	Ratio vs res. load	(10-90% of V_{OUT})	(90-10% of V_{OUT})	(at -0.6V) [µs]
300	13.5	65	0.47	315	2.01	34	37	74
1 000	13.5	162	1.17	450	2.87	33	38	246
3 500	13.5	302	2.17	490	3.12	32	37	861
5 400	13.5	360	2.59	505	3.22	31	36	1328
20 000	13.5	398	2.86	490	3.12	31	35	4919

Note: Used inductors: 1.5 µH ÷ 5.4 mH: Air coil (1.5 mm^2 cable)
20 mH: Iron powder core inductor (I_{SAT} ~ 3 A)
The coil resistance compensated by adding a serial resistor to reach 13.5 Ω in total.

Switching losses - capacitive loads

This chapter deals with the switching losses in combination with capacitive loads. A typical application example is the usage of the HSD as a supply voltage switch for other modules (see *Figure 68*).

Figure 68. A typical example of HSD combined with capacitive load



A capacitive character of the load creates an inrush current during turn-on phase, depending mainly on the load capacitance, switching time and the load resistance (i.e. capacitor ESR). A typical requirement for the HSD in such applications is ability to handle the worst case inrush current without activation of the protection mechanisms (power limitation or thermal shutdown) to ensure correct operation of connected load (module). Since there are several variables and conditions depending on application, there is no calculation provided in this chapter.

The following measurement was performed on several different parts (R_{DSON} classes) in order to determine the turn-on switching loss, slew rate and maximum possible capacitance which don't trigger the device protection. The devices were loaded by an electrolytic capacitor (or parallel combination of capacitors) and 10 kΩ resistor (for the discharge).

Conditions:

- V_{BAT}: 16 V
- Temperature: 23 °C
- Device/Load (10 kΩ pull down resistor connected in parallel for discharge)
  - VND7140AJ, Ch.0:
    10 µF
    22 µF
    32 µF (10+22)
    44 µF (22+22)
    76 µF (22+22+22+10)
    88 µF (22+22+22+22)
  - VND7040AJ, Ch.0:
    100 µF
    220 µF
    320 µF (100+220)
    440 µF (220+220)
    660 µF (220+220+220)
  - VND7020AJ, Ch.0:
    220 µF
    440 µF (220+220)
    1220 µF (1000+220)
    1440 µF (1000+220+220)
    2200 µF
    3200 µF (2200+1000)
  - VN7016AJ
    220 µF
    440 µF (220+220)
    1000 µF
    2200 µF
    2640 µF (2200+220+220)
    3200 µF (2200+1000)
  - VN7004AH-E
    220 µF
    440 µF (220+220)
    2200 µF
    3200 µF (2200+1000)
    4700 µF
    5700 µF (4700+1000)

- Used capacitors: Electrolytic – aluminum
  - 1 µF / 50V, ESR = 1.7 Ω
  - 10 µF / 25V, ESR = 1 Ω
  - 22 µF / 25V, ESR = 0.7 Ω
  - 100 µF / 50V, ESR = 0.17 Ω
  - 220 µF / 35V, ESR = 0.14 Ω
  - 1000 µF / 35V, ESR = 0.03 Ω
  - 2200 µF / 25 V, ESR = 0.035 Ω
  - 4700 µF / 35 V, ESR = 0.020 Ω

Experimental results done on a sample of each mentioned device have highlighted that no protection is triggered for value of capacitance below the ones indicated in *Table 23*.

Figure 69. Measurement example - VND7040AJ on 320µF

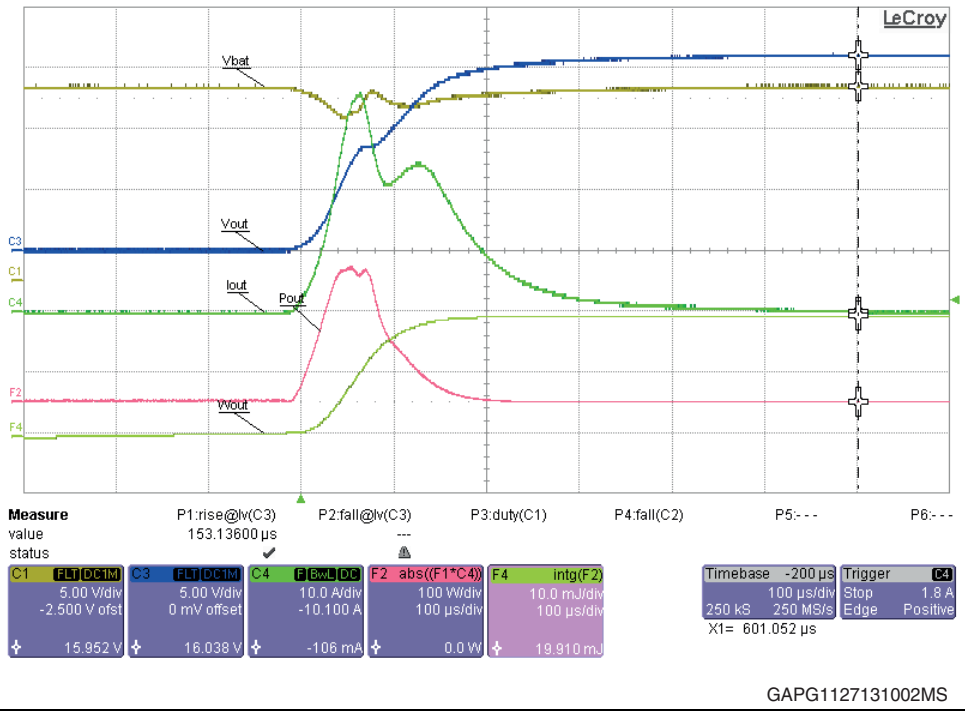


Table 23. Maximum capacitance on the HSD output (no power limitation triggered - T_{jstart} ~ 25 °C)

Part number	Experimentally determined maximum capacitance [µF]	Turn-on loss [mJ]	Slew rate (dV_{OUT}/dt) [V/µs]	Max. capacitance [µF] (safety margin applied)
VND7140AJ	76 (22+22+22+10)	6.05	0.11	47
VND7040AJ	320 (100+220)	19.9	0.084	220
VND7020AJ	1220 (1000+220)	44.7	0.039	820
VN7016AJ	2200	80	0.031	1500
VN7004AH-E	4700	357	0.008	3300

Switching losses - Xenon

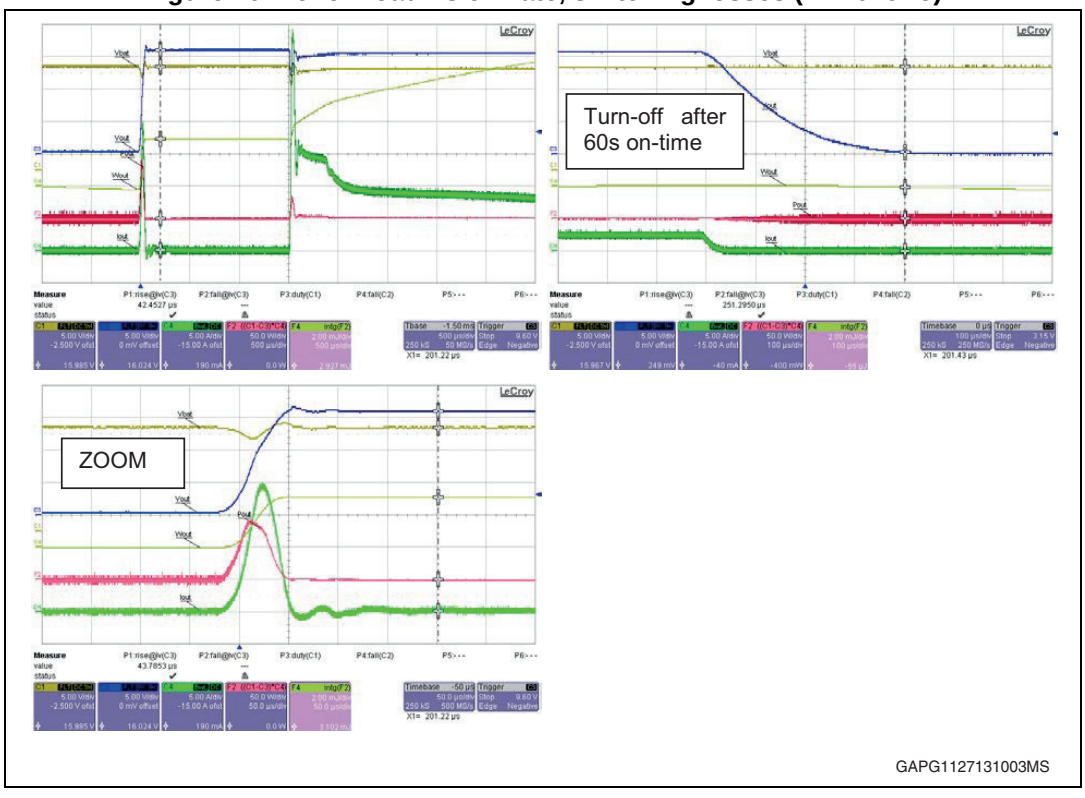
Since there are several different types of the Xenon modules/Lamps, there is probably no general way for the switching losses calculation or estimation. Aim of this chapter is to show one example related to a measurement with specific Xenon module and Xenon lamp.

In most cases, there are two inrush currents phases. The first peak comes during the HSD activation (charging of the input capacitor of the module) and the second peak after the ignition of the Xenon bulb. Therefore, in terms of switching losses, the xenon module behaves like a capacitive load (the first inrush current peak). When the input capacitor is charged (V_{OUT} reaches nominal current) the input current falls down (usually almost zero) until the ignition starts (usually after a few ms delay). This second inrush phase is not contributing to the turn-on switching loss since the HSD is already turned–on. The losses during HSD deactivation are usually negligible due to the capacitive character of the load.

Switching losses – measurement example

- V_{BAT}: 16 V
- Temperature: 23 °C
- Load:
  - Xenon lamp: Phillips D2S 35 W
  - Ballast: Hella 5DV 008 290-00
- Device: VN7016AJ

Figure 70. Xenon load - slew rate, switching losses (VN7016AJ)



Measured values:

W_{ON} ~ 3.1 mJ $(dV_{OUT}/dt)_{ON}$ = 0.8*16 V/44 µs = 0.29 V/µs

W_{OFF} ~ 0 mJ $(dV_{OUT}/dt)_{OFF}$ = 0.8*16 V/251 µs = 0.051 V/µs

During the HSD channel activation the xenon module behaves like capacitive load (waveforms / losses equivalent to ~47 µF capacitor). When the input capacitor is charged (V_{OUT} = nominal) the input current falls to ~0 until the convertor starts (~1.5 ms delay).

The losses during HSD deactivation are below the measurement resolution (capacitive character of the load).

6.3 Inductive loads

Switching inductive loads such as relays, solenoids, motors etc. can generate transient voltages of many times the steady-state value. For example, turning off a 12 volt relay coil can easily create a negative spike of several hundred volts. The M0-7 high-side drivers are well designed to drive such kind of loads, in most cases without any external protection. Nevertheless there are physical limits for each component that have to be respected in order to decide if an external protection is necessary or not.

As a feature of the M0-7 drivers it can be highlighted that a relatively high output voltage clamping leads to a fast demagnetization of the inductive load.

The aim of this chapter is to have a simple guide on how to check the conditions during demagnetization, how to select a proper HSD (and the external clamping if necessary) according to the given load.

6.3.1 Turn-on

When a HSD turns on an inductive load the current is increasing with a time constant given by L/R values, so the nominal load current is not reached immediately. This fact should be considered in diagnostics software (i.e. to avoid false open-load detection).

Figure 71. HSD turn-on phase with inductive load

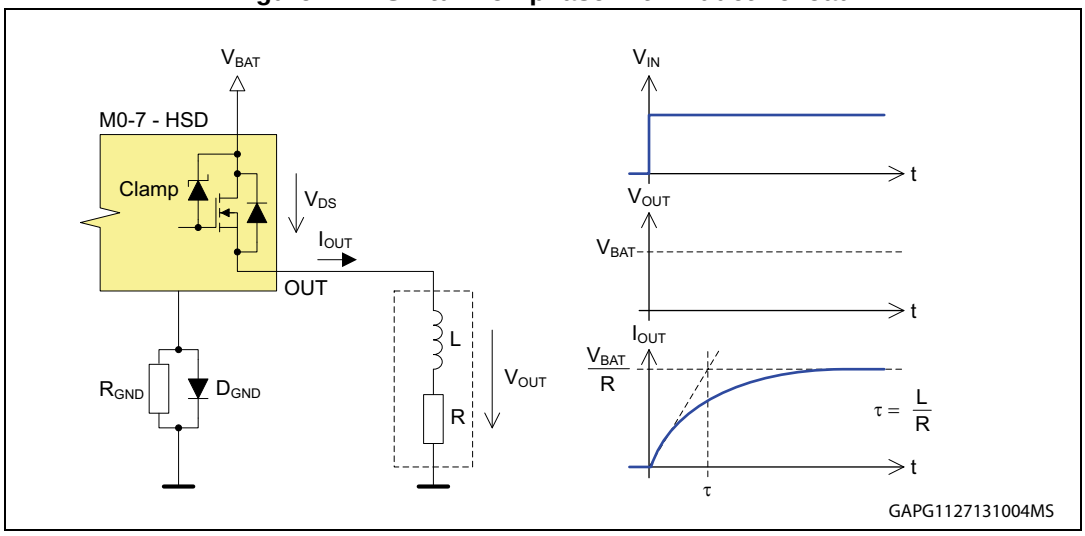
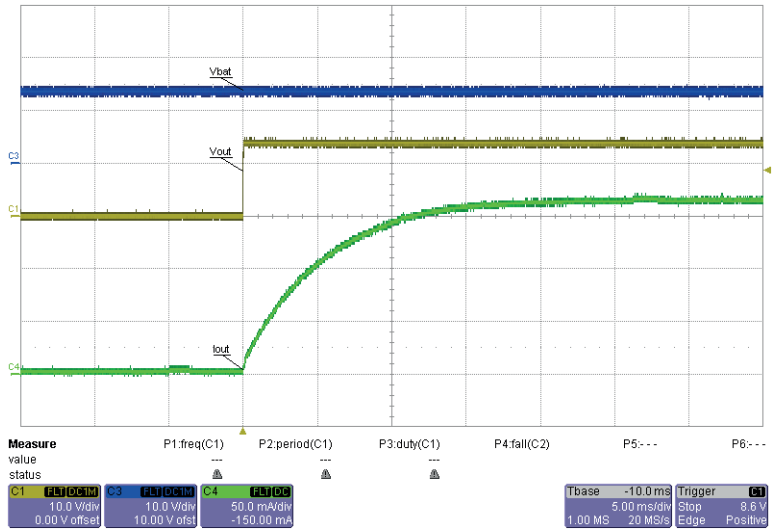


Figure 72. Turn-on example: VND7140AJ with inductive load (L = 260 mH, R = 81 Ω)



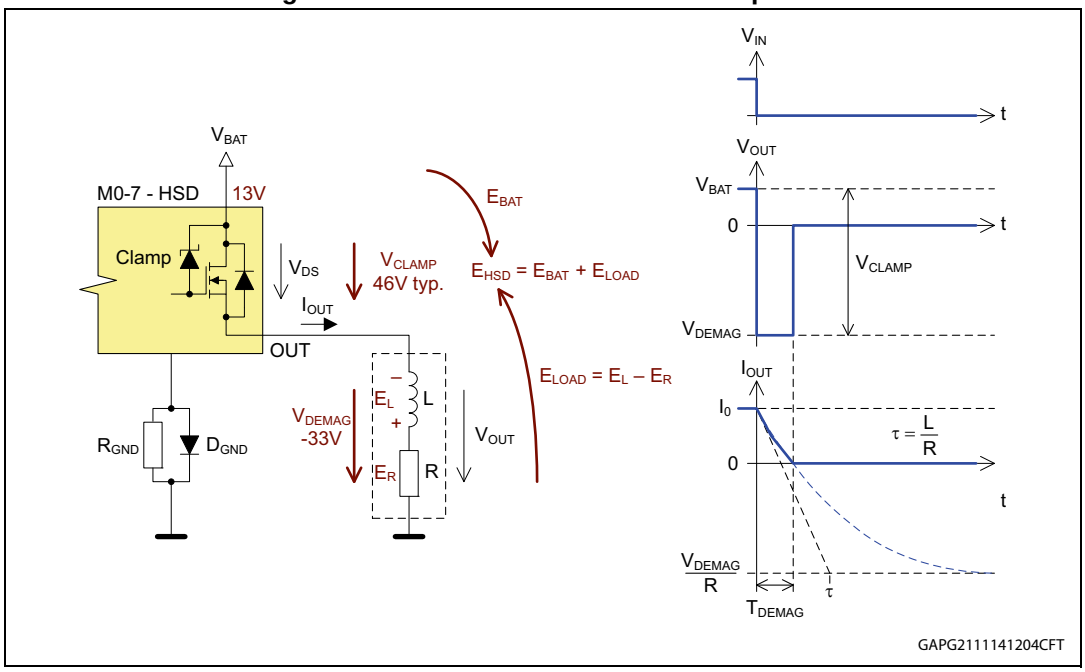
6.3.2 Turn-off

The HSD turn-off phase with inductive load is explained in *Figure 73*. The inductance reverses the output voltage in order to be able to continue driving the current in the same direction. This voltage (so called demagnetization voltage) is limited to the value given by the clamping voltage of the HSD and the battery voltage:

Equation 3

$$V_{DEMAG} = V_{BAT} - V_{CLAMP} = 13V - 46V \text{ (typical)}$$

Figure 73. Inductive load–HSD turn-off phase



The load current decays exponentially (linearly if R → 0) and reaches zero when all energy stored in the inductor is dissipated in the HSD and the load resistance.

Since the HSD output clamp is related to the V_{BAT} pin, the energy absorbed by the HSD grows with increasing battery voltage (the battery is in series with the high-side switch and load so the energy contribution of the battery is increasing with the battery voltage).

6.3.3 Calculation of dissipated energy

The energy dissipated in the high-side driver is given by the integral of the actual power on the MOSFET through the demagnetization time:

$$E_{HSD} = \int_0^{T_{DEMAG}} V_{CLAMP} \cdot i_{OUT}(t)dt$$

To integrate the above formula we need to know the current response $i_{OUT}(t)$ and the demagnetization time T_{DEMAG}. The $I_{OUT}(t)$ can be obtained from the well-known formula of R/L circuit current response using the initial current I_0 and the final current V_{DEMAG}/R considering $i_{OUT} \geq 0$ condition (see *Figure 73*):

$$i_{OUT}(t) = I_0 - \left(I_0 + \frac{|V_{DEMAG}|}{R}\right) \cdot \left(1 - e^{\frac{-t \cdot R}{L}}\right) \qquad (0 < t < T_{DEMAG} \rightarrow i_{OUT} \geq 0)$$

Putting i(t) = 0 we can calculate the demagnetization time:

Equation 4

$$T_{DEMAG} = \frac{L}{R} \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right)$$

Equation 5

$$\lim_{R \to 0} T_{DEMAG} = L \cdot \frac{I_0}{V_{DEMAG}} \qquad \text{(simplified for } R \to 0\text{)}$$

Substituting the T_{DEMAG} and $i_{OUT}(t)$ by the formulas above we can calculate the energy dissipated in the HSD:

$$E_{HSD} = \int_0^{T_{DEMAG}} V_{CLAMP} \cdot i_{OUT}(t)dt = \int_0^{T_{DEMAG}} (V_{BAT} + |V_{DEMAG}|) \cdot i_{OUT}(t)dt$$

then

Equation 6

$$E_{HSD} = \frac{V_{BAT} + |V_{DEMAG}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{DEMAG}| \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right) \right]$$

Equation 7

$$\lim_{R \to 0} E_{HSD} = \frac{1}{2} \cdot L \cdot I^2_0 \cdot \frac{V_{BAT} + |V_{DEMAG}|}{|V_{DEMAG}|} \qquad \text{(simplified for } R \to 0\text{)}$$

Calculation example:

This example shows how to use above equations to calculate the demagnetization time and energy dissipated in the HSD:

- Battery voltage: V_{BAT} = 13.5 V
- HSD: VND7040AJ
- Clamping voltage: V_{CLAMP} = 46 V (typical for M0-7)
- Load resistance: R = 81 Ω
- Load inductance: L = 260 mH
- Load current (at turn-off event): $I_0 = V_{BAT}/R$ = 167 mA

Step 1) Demagnetization voltage calculation using *Equation 1*

$$V_{DEMAG} = V_{BAT} - V_{CLAMP} = 13.5 - 46 = -32.5V$$

Step 2) Demagnetization time calculation using *Equation 2*:

$$T_{DEMAG} = \frac{L}{R} \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right) = \frac{0.260}{81} \cdot \ln\left(\frac{32.5 + 0.167 \cdot 81}{32.5} \right) = 1.12ms$$

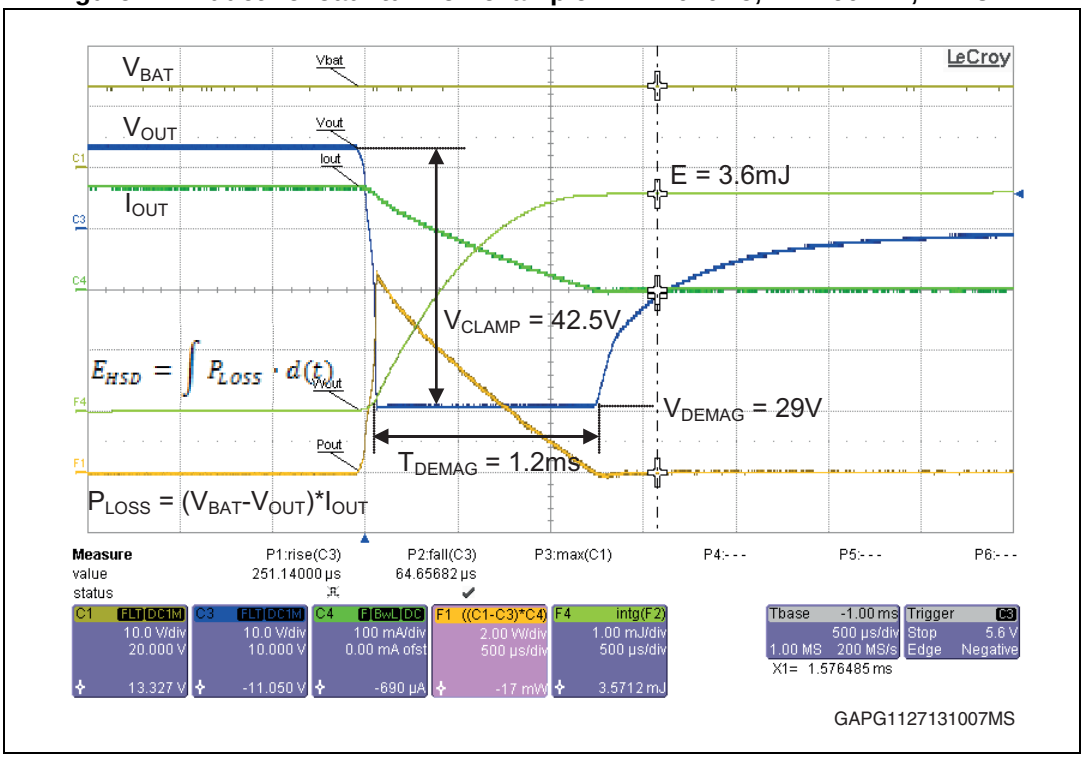
Step 3) Calculation of energy dissipated in the HSD using *Equation 6*:

$$E_{HSD} = \frac{V_{BAT} + |V_{DEMAG}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{DEMAG}| \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right) \right] =$$

$$= \frac{13.5 + 32.5}{81^2} \cdot 0.260 \cdot \left[81 \cdot 0.167 - 32.5 \cdot \ln\left(\frac{32.5 + 0.167 \cdot 81}{32.5} \right) \right] = 4.04\text{mJ}$$

Step 4) Measurement (comparison with theory):

Figure 74. Inductive load: turn-off example: VND7040AJ, L = 260 mH, R = 81 Ω



The demagnetization energy dissipated in the HSD was measured by an oscilloscope with mathematical functions. The first function F1 shows the actual power dissipation on the HSD (V_{BAT} - V_{OUT}) * I_{OUT}, the second function F4 shows the HSD energy (integral of F1).

As seen from the oscillogram, measured values are close to the theoretical calculation: E_{HSD} = 3.6 mJ (4.04 mJ calculated), T_{DEMAG} = 1.2 ms (1.12 ms calculated).

6.3.4 Selection criterion with reference to I-L plot

Even if the device is internally protected against break down during the demagnetization phase, the energy capability has to be taken into account during the design of the application.

It is possible to identify two main mechanisms that can lead to the device failure:

- The temperature during the demagnetization rises quickly (depending on the inductance) and the uneven energy distribution on the power surface can cause the presence of a hot spot causing the device failure with a single shot.
- Like in a normal operation, the life time of the device is affected by the fast thermal variation as described by the Coffin-Manson law. A repetitive demagnetization energy causing a temperature variation above 60 K will cause a shorter life time.

These considerations lead to two simple design rules:

- The energy has to be below the energy the device can withstand at a given inductance.
- In case of a repetitive pulse, the average temperature variation of the device should not exceed 60 K at turn-off.

To fulfill these rules the designer has to calculate the energy dissipated in the HSD at turn-off and then to compare this number with the datasheet values as shown in the following example.

Example:

Check if the VND7020AJ device can safely drive the inductive load 2.2 mH at 4 Ω under following conditions:

- Battery voltage: V_{BAT} = 16 V
- HSD: VND7020AJ
- Load resistance: R = 4 Ω
- Load inductance: L = 2.2 mH
- Load current (at turn-off event): $I_0 = V_{BAT}/R$ = 16 V/4 Ω = 4 A
- Power clamping voltage: V_{CLAMP} = 46 V (typical value considered)

Step 1) Demagnetization voltage calculation using *Equation 1*

$$V_{DEMAG} = V_{BAT} - V_{CLAMP} = 16 - 46 = -30V$$

Step 2) Demagnetization time calculation using *Equation 2*:

$$T_{DEMAG} = \frac{L}{R} \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right) = \frac{0.0022}{4} \cdot \ln\left(\frac{30 + 4 \cdot 4}{30}\right) = 235\mu s$$

Step 3) Calculation of energy dissipated in the HSD using *Equation 6*:

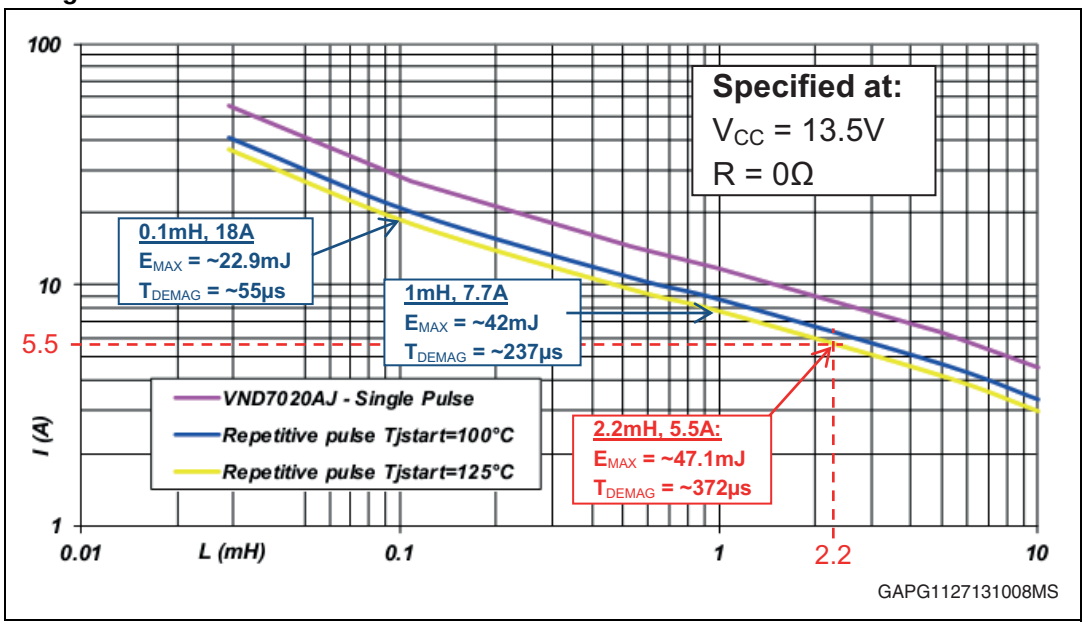
$$E_{HSD} = \frac{V_{BAT} + |V_{DEMAG}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{DEMAG}| \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right)\right] =$$

$$= \frac{16 + 30}{4^2} \cdot 0.0022 \cdot \left[4 \cdot 4 - 30 \cdot \ln\left(\frac{30 + 4 \cdot 4}{30}\right)\right] = 20.1mJ$$

Step 4) HSD datasheet analysis:

The maximum demagnetization energy is derived from the I-L diagram in the datasheet (see *Figure 75*).

Figure 75. Maximum turn-off current versus inductance – VND7020AJ datasheet



The maximum turn-off current for 2.2 mH inductance is 5.5 A (for the repetitive pulse, T_{jstart} = 125 ºC) which is above the load current in this example (I_0 = 4 A). However, this current limit is specified for R = 0 Ω and V_{BAT} = 13.5 V. Since these conditions are different from conditions considered in this example (R = 4 Ω, V_{BAT} = 16 V), it is recommended to find the energy limit in the I-L diagram with same demagnetization time as calculated in the example (235 µs). Then it is possible to directly compare this limit with calculated energy in the application (regardless the different condition). As a first step, the 2.2 mH, 5.5 A limit is selected from the I-L diagram and related energy limit and demagnetization time is calculated:

Demagnetization energy related to selected point (2.2 mH, 5.5 A) using *Equation 7*:

$$E_{MAX} = \frac{1}{2} \cdot L \cdot I^2_{MAX} \cdot \frac{V_{BAT} + |V_{DEMAG}|}{|V_{DEMAG}|} = \frac{1}{2} \cdot 0.0022 \cdot 5.5^2 \cdot \frac{13.5 + 32.5}{35.5} = 47.1mJ$$

Demagnetization time related to selected point (2.2 mH, 5.5 A) using *Equation 5*:

$$T_{DEMAG} = L \cdot \frac{I_0}{V_{DEMAG}} = 0.0022 \cdot \frac{5.5}{32.5} = 372\mu s$$

Note: Same calculation as E_{MAX} and T_{DEMAG} is performed at 1 mH and 0.1 mH, just to see the dependency on inductance (see Figure 75).

As seen from the calculation, the maximum energy related to selected point is 47.1 mJ at 372 µs. In order to find the energy limit at 235 µs, either an iterative process can be performed in graphical way (repeat the same calculation with different I-L point choices until the T_{DEMAG} is matching), or the following empiric formula can be used, where E_1 is the sustainable energy for time t_1 and E2 is sustainable energy corresponding to different application condition (time t_2):

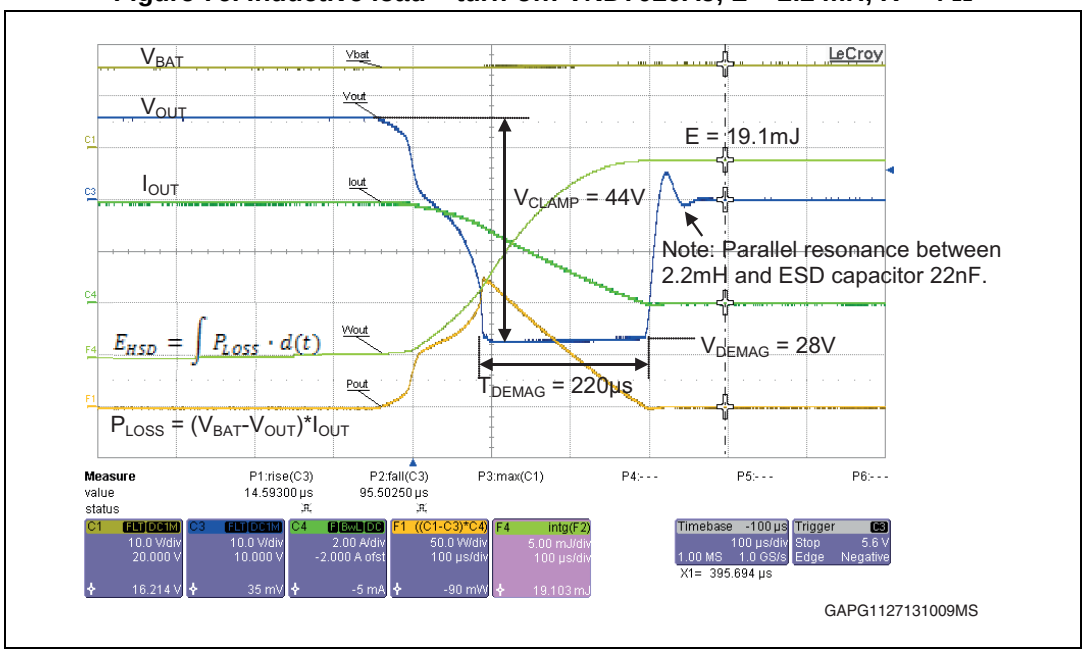
$$E_2 \approx E_1 \cdot \sqrt{\frac{t_2}{t_1}} = 47.1\text{mJ} \cdot \sqrt{\frac{235\mu s}{372\mu s}} = 37.4\text{mJ}$$

Conclusion: The device is able to safely drive the selected load since the calculated demagnetization energy (20.1 mJ at 235 µs) is clearly below the maximum allowed demagnetization energy derived from the I-L diagram for the repetitive operation T_{jstart} = 125 ºC: 37.4 mJ at 235 µs.

Step 5) Measurement (comparison with theory):

The demagnetization energy dissipated in the HSD was measured by an oscilloscope with mathematical functions. The first function F1 shows the actual power dissipation on the HSD (V_{BAT} - V_{OUT}) * I_{OUT}, the second function F4 shows the HSD energy (integral of F1).

Figure 76. Inductive load – turn-off: VND7020AJ, L = 2.2 mH, R = 4 Ω



As seen from the oscillogram, measured values are close to the theoretical calculation: E_{HSD} = 19.1 mJ (20.1 mJ calculated), T_{DEMAG} = 220 µs (235 µs calculated).

Conclusion:

The device can safely drive the load without additional protection. The worst case demagnetization energy is clearly below the device limit.

6.3.5 External clamping protection

The main function of an external clamping circuitry is to clamp the demagnetization voltage and dissipate the demagnetization energy in order to protect the HSD. It can be used as a cost effective alternative in case the demagnetization energy is exceeding the energy capability of a given HSD. A typical example is driving DC motors (high currents in combination with high inductance). During the selection of a suitable HSD for such kind of application we usually end up in the situation that a given HSD is fitting in terms of current profile, but the worst case demagnetization energy is too high (turn-off from stall condition at

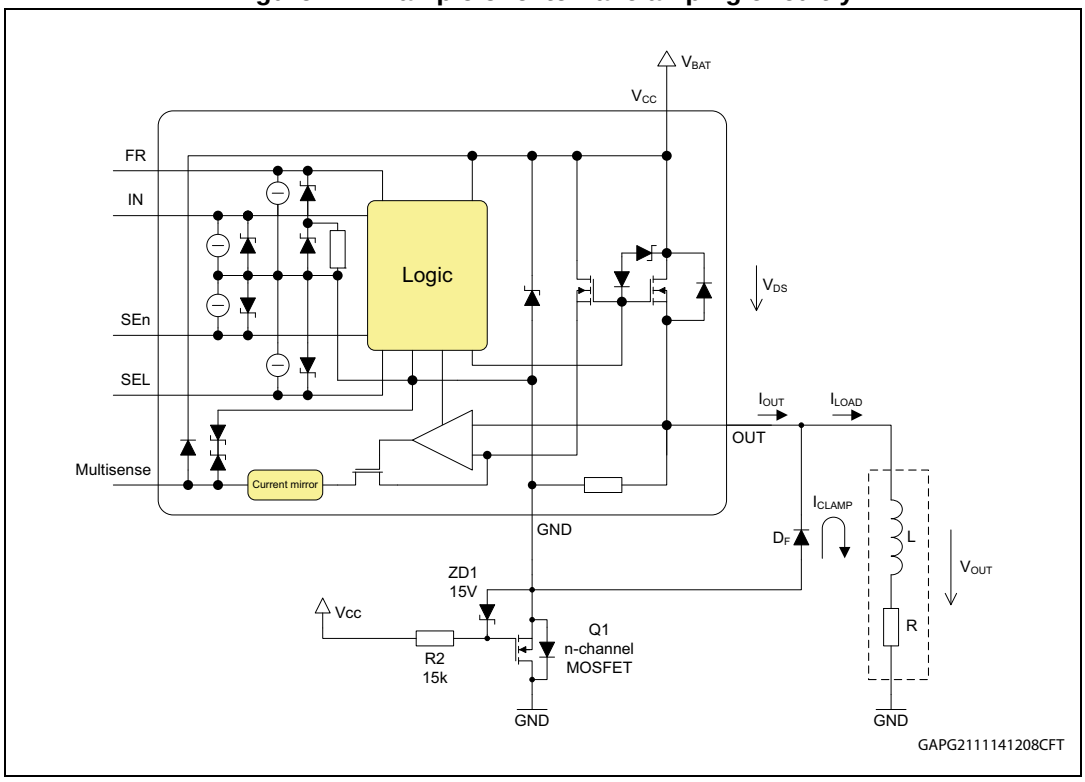
16 V, -40 ºC). Rather than selecting a bigger HSD the use of an external clamp can be the most convenient choice.

External clamping circuitry – requirements summary:

- Negative clamping voltage below the HSD clamping voltage
- No conduction at:
  - Normal operation (0-16 V)
  - Jump start (27 V for 60 s)
  - Load Dump (36 V for 400 ms)
  - Reverse battery condition (-16 V for 60 s)
- Proper energy capability
  - Single demagnetization pulse
  - Repetitive demagnetization pulse

An example of external clamping circuitry (compatible with all above listed requirements) is shown on *Figure 77*.

Figure 77. Example of external clamping circuitry



It is a combination of standard freewheeling diode and active reverse battery protection with N-channel MOSFET (introduced in previous reverse battery protection chapter). Since the anode of the diode is connected to the source of the MOSFET, it is protected (disconnected) during reverse battery condition or negative ISO pulse. In normal operation conditions it behaves like a standard freewheeling diode (connected in parallel with load). By using a standard silicon diode, the demagnetization voltage is reduced from –32 V (a typical V_{DEMAG} of M0-7 device at V_{BAT} = 14 V) to approximately –1 V (depending on forward voltage of the diode and the voltage drop on the MOSFET). This has an influence to the

demagnetization time (lowering $|V_{DEMAG}| \rightarrow$ increasing T_{DEMAG}), as can be derived from the T_{DEMAG} equation.

Component selection:

- MOSFET Q1:
  - According to ISO pulse requirements – see reverse battery protection chapter
  - Drain current (pulsed) I_{DM}: I_{DM}[(a)] > Load current
- Diode D_F:
  - Peak repetitive reverse voltage V_{RRM}: V_{RRM} > 52 V
    (must not conduct during positive transient on the output → limited by the V_{CC_GND} clamp V_{CLAMP_max} = 52 V)
  - Non-repetitive peak forward surge current I_{FSM}: I_{FSM} > Load current
    This parameter must be aligned with T_{DEMAG}
  - Average rectified forward current $I_{F(AV)}$: I_{FAV} > (Average clamp current in repetitive operation)

Limited by max. junction temperature

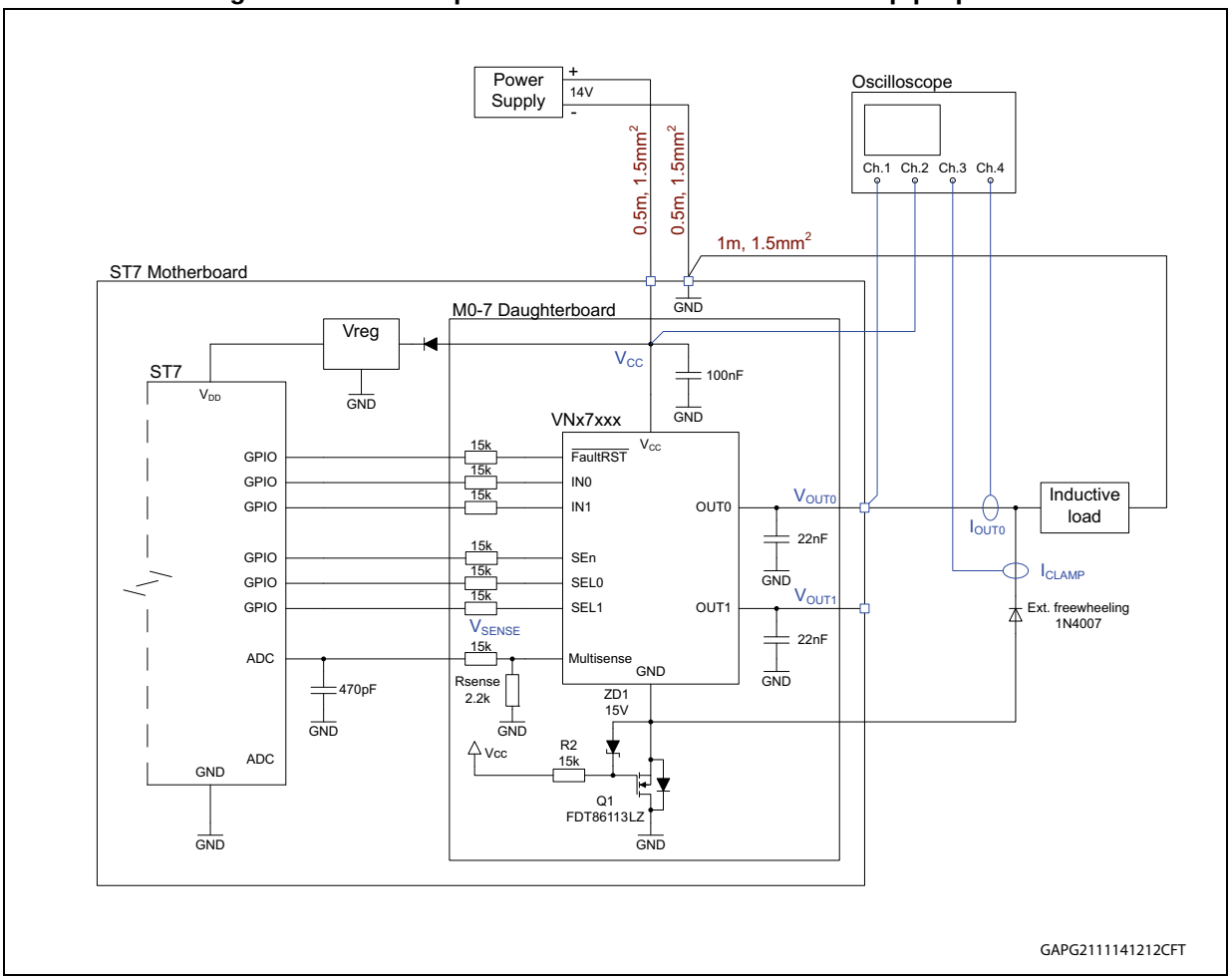
Experimental verification of described clamping circuitry

Check the freewheeling operation at different conditions (different duty cycle in repetitive operation, negative ISO pulse, loss of V_{CC}).

- V_{BAT}: 14 V
- Temperature: 25 °C
- Device: VND7040AJ
- Load: 2 mH, 5.5 Ω

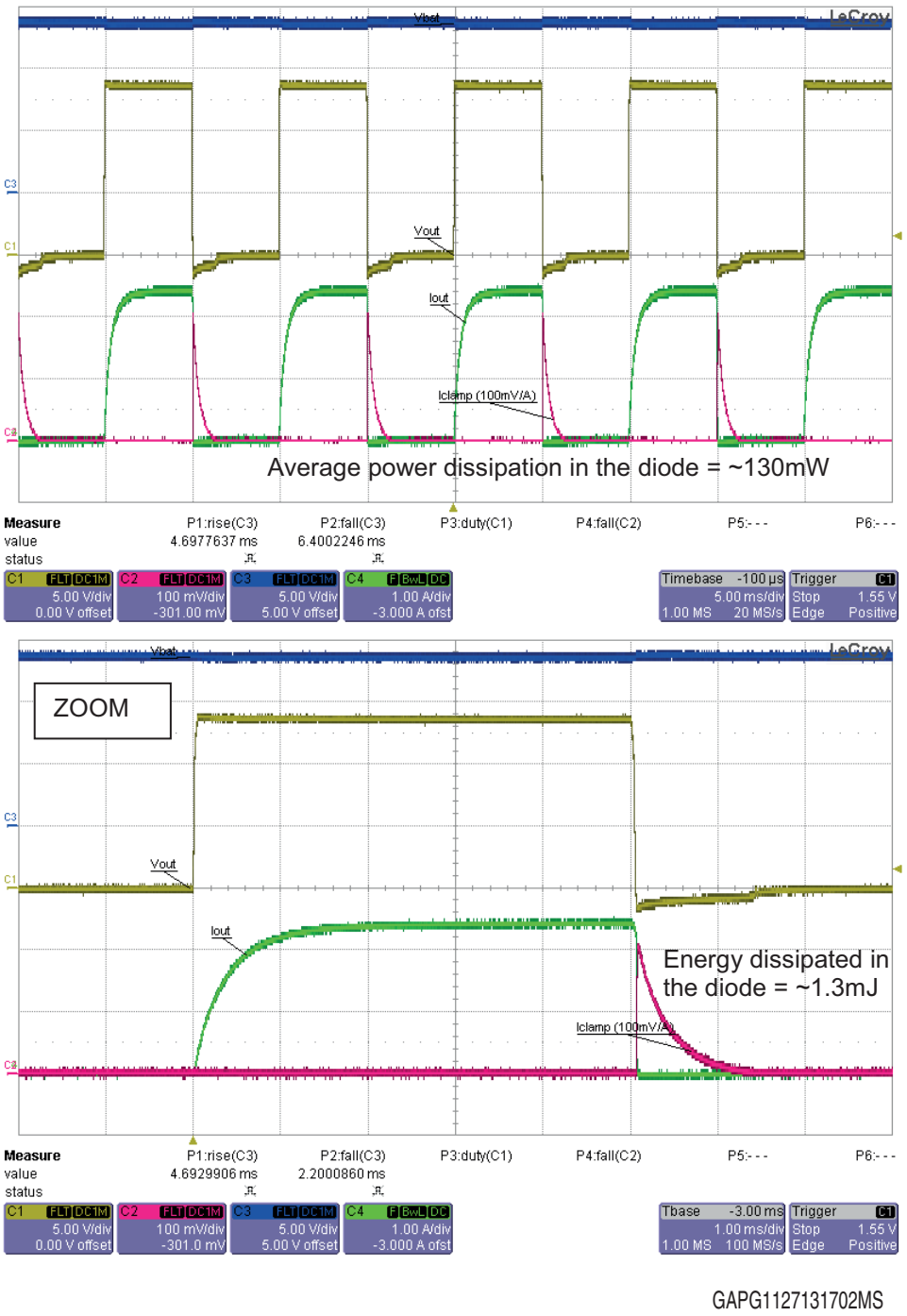
a. Limited by safe operating area according to T_{DEMAG} (single pulse).
Limited by max. junction temperature (repetitive pulses).

Figure 78. Test setup-verification of new external clamp proposal



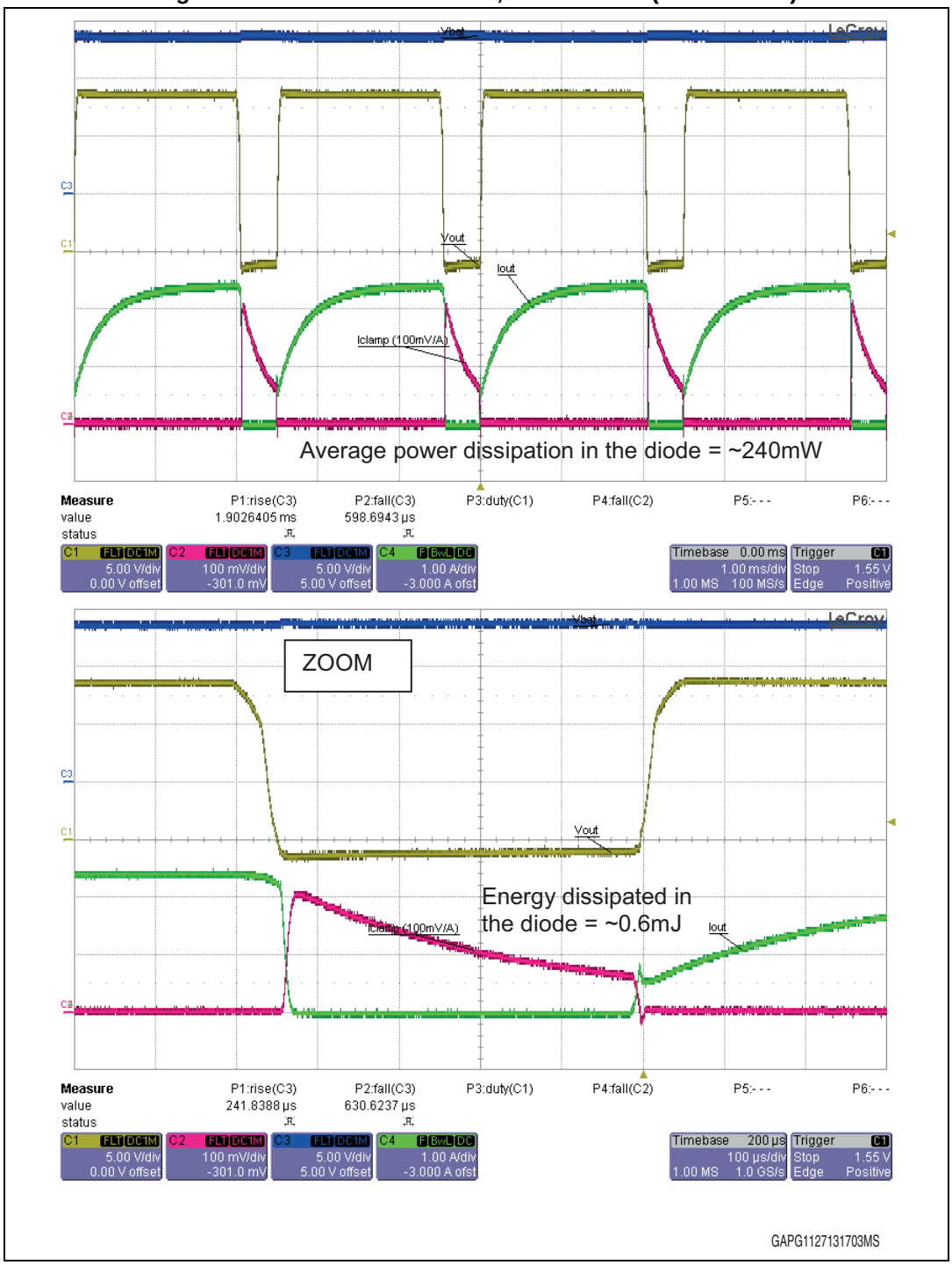
Repetitive operation – PWM 50 % at 100 Hz (the demagnetization time is shorter than the PWM off-state time, see *Figure 79*):

Figure 79. PWM 50% at 100 Hz, 2 mH / 5.5 Ω (VND7040AJ)



Repetitive operation – PWM 80 % at 400 Hz (the demagnetization time is longer than the PWM off-state time, see *Figure 80*):

Figure 80. PWM 80 % at 400 Hz, 2 mH / 5.5 Ω (VND7040AJ)



Negative ISO pulse exposure on V_{CC} line:

Figure 81. ISO pulse 1 (-100 V, 10 Ω), 2 mH at 5.5 Ω (VND7040AJ)

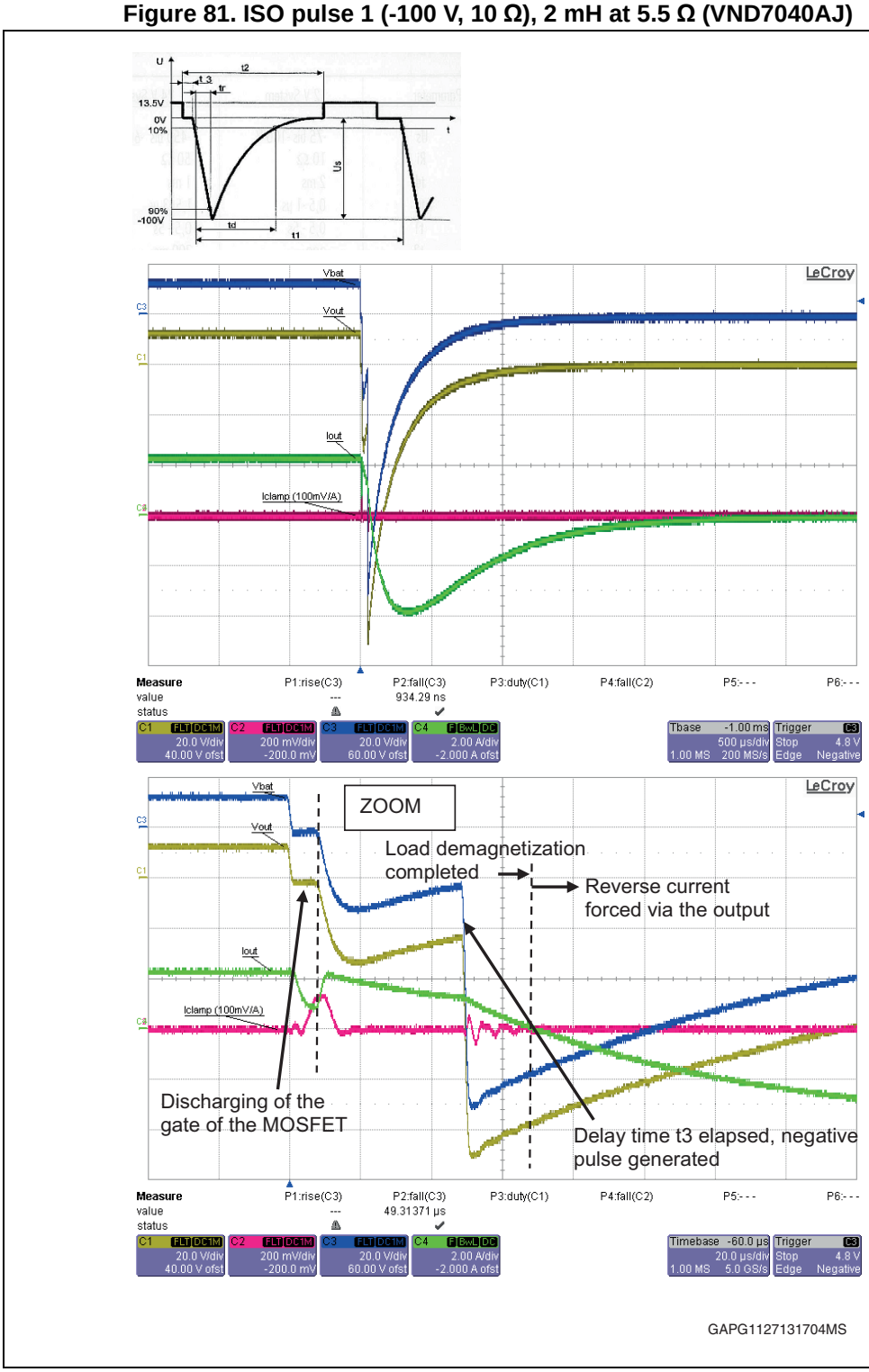
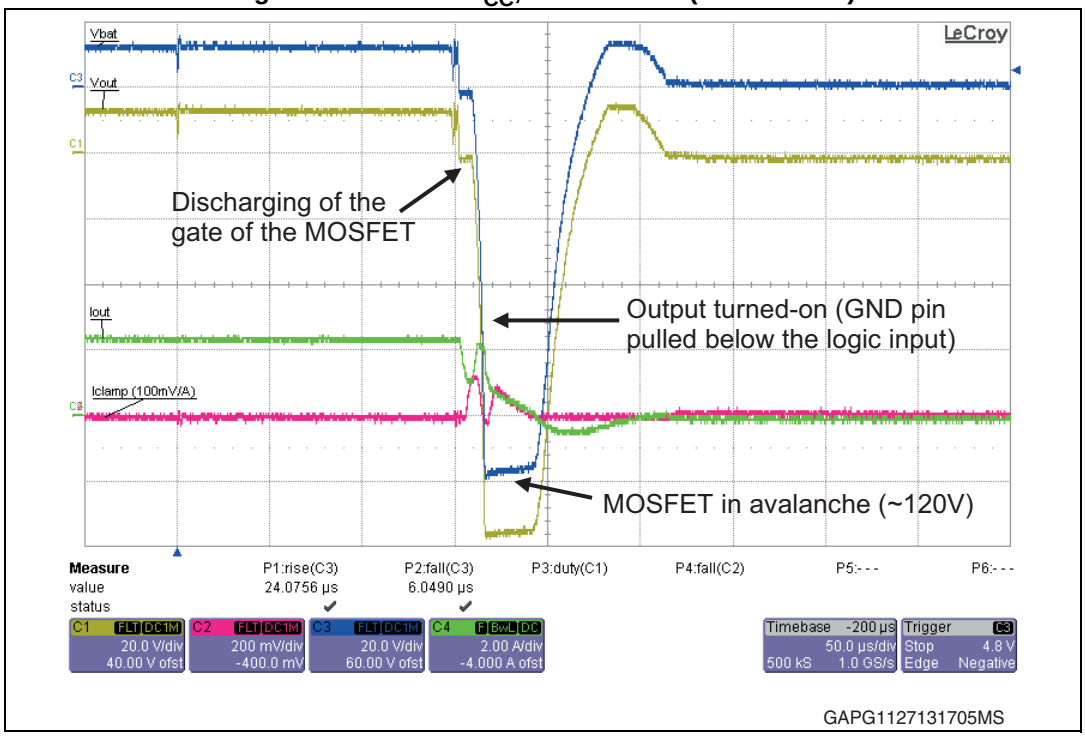


Figure 82. Loss of V_{CC}, 2 mH / 5.5 Ω (VND7040AJ)



Conclusion:

The circuitry behavior is the expected one. After loss of V_{CC} or negative ISO transient, most of the demagnetization energy is submitted to the reverse battery protection MOSFET and supply line (capacitor). The energy dissipated in the device is relatively low since the channels are most of the time turned-on (the device GND pin pulled negative via freewheeling diode, below the logic pins).

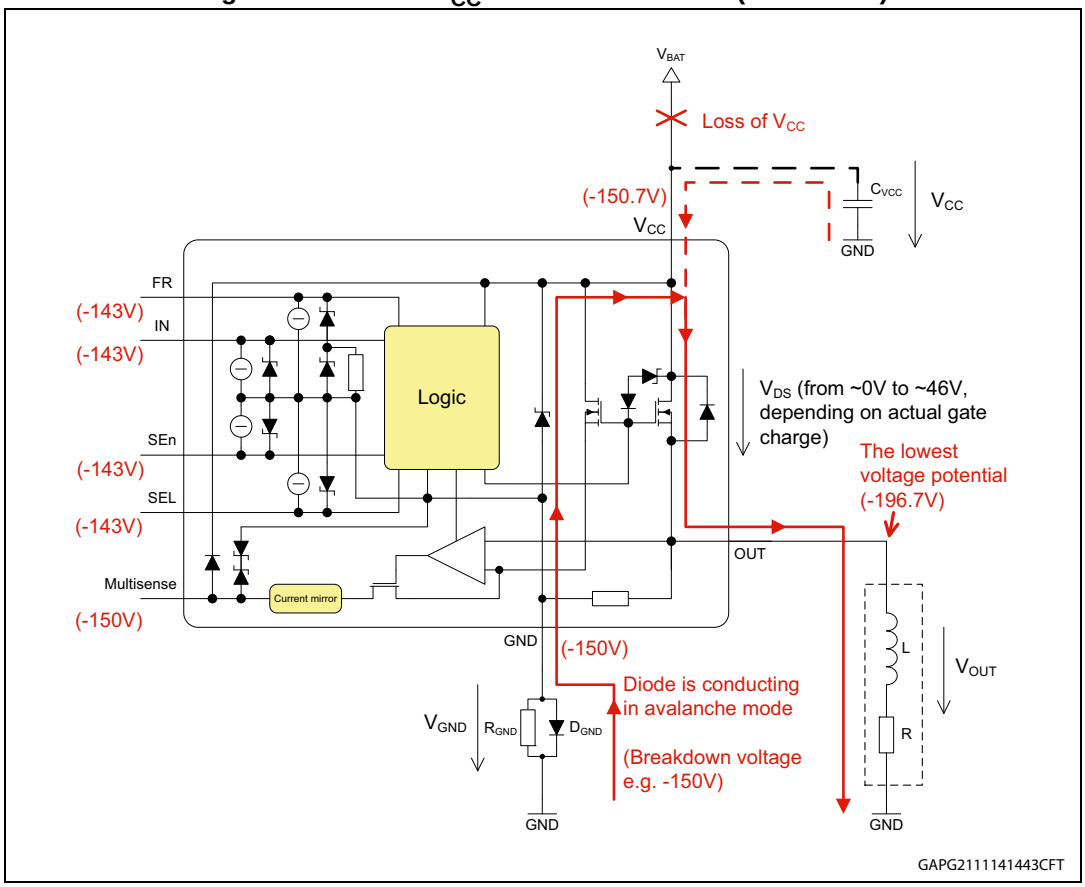
6.3.6 Loss of V_{CC}

The loss of supply voltage (e.g. due to blown fuse, intermittent contact on ECU connector etc.), in combination with inductive load on HSD output, can lead to huge negative voltage peak on all device pins (assuming the load without external freewheeling). The aim of this paragraph is to complement the theoretical explanations of different cases of loss of V_{CC} with experimental verifications. The device used is the VND7020AJ.

Monolithic device (with GND network)

When the V_{CC} disconnection occurs during the on-state, the load inductance tends to continue to drive the current via any available path by reversing its voltage (acts as a source) until the stored energy $E_L = \frac{1}{2} \cdot L \cdot I_0^2$ is dissipated. Therefore the lowest voltage potential is seen on the OUT pin which is forced in negative by the inductance – see *Figure 83*.

Figure 83. Loss of V_{CC} with inductive load (monolithic)



The V_{CC} pin is pulled down by the output via the device power MOSFET. If the gate of this MOSFET is still charged (immediately after the V_{CC} disconnection), the V_{CC} pin voltage follows the OUT pin voltage while the voltage levels on both pins are the same (neglecting the voltage drop on R_{DSON}). As the gate is being discharged, the voltage drop can rise up to the V_{CLAMP} (~46 V) as indicated on the figure. Since the V_{CC} pin is floating (neglecting the V_{CC} capacitor), the negative voltage is theoretically unlimited (no external freewheeling considered, no discharge path for the demagnetization available). Practically, the V_{CC} pin voltage is limited by the breakdown voltage of the GND network diode through which the demagnetization paths is closed (the GND pin is also pulled down via an internal V_{CC} - GND clamp structure with one diode voltage drop versus V_{CC} pin). The MultiSense and all logic pins are pulled down as well – see clamp structure on *Figure 83*.

The fact that all device pins are pulled so deeply in negative can have the following drawbacks:

- The GND network diode must have a proper avalanche capability (limiting factor during the choice, higher cost)
- A relatively high current injected to the microcontroller (~ -10 mA per pin in case of above example, assuming 15 k serial resistors)
- Negative peak on V_{CC} pin can influence other devices sharing same supply line or same ground protection network
- The level of the negative pulse on V_{CC} is not exactly known (depends on break down voltage of D_{GND} which is usually not exactly specified)

The above mentioned issues can be eliminated by a proper *Capacitor selection* or *Bidirectional suppressor selection* connected between the V_{CC} pin and module ground. This external device provides the demagnetization path and absorbs the demagnetization energy.

Capacitor selection

A minimum capacitor value can be roughly estimated from the energy content stored in the inductor and required suppression level (voltage change on the capacitor after the demagnetization phase):

Energy stored in the inductor: $E_L = \frac{1}{2} \cdot L \cdot I_0^2$

Energy absorbed by the V_{CC} capacitor: $E_L = \frac{1}{2} \cdot C_{VCC} \cdot (V_{CC} - V_{CC\_FINAL})^2$

Where:

I_0: Load current at V_{CC} disconnection

V_{CC}: Supply voltage

V_{CC_FINAL}: Final voltage on V_{CC} capacitor after the demagnetization phase

If we assume that the whole inductive energy is transferred to the capacitor ($E_L = E_C$) this yields:

$$C_{VCC} \cong L \cdot \frac{I_0^2}{(V_{CC} - V_{CC\_FINAL})^2}$$

Calculation example:

Battery voltage: V_{CC} = 14 V

- Final voltage on V_{CC} capacitor:
  - Option 1) V_{CC_FINAL} = 0 V (negative voltage fully suppressed)
  - Option 2) V_{CC_FINAL} = -90 V (still safe value in order to avoid the breakdown of D_{GND}, with maximum reverse voltage 100 V)
- Load inductance: L = 1 mH
- Load current: I_0 = 4 A

Option 1):

$$C_{VCC} \cong L \cdot \frac{I_0^2}{(V_{CC} - V_{CC\_FINAL})^2} = 0.001 \cdot \frac{4^2}{(14-0)^2} = 81.63\ \mu F$$

Option 2):

$$C_{VCC} \cong L \cdot \frac{I_0^2}{(V_{CC} - V_{CC\_FINAL})^2} = 0.001 \cdot \frac{4^2}{(14-90)^2} = 1.48\ \mu F$$

The minimum capacitor value needed to completely suppress the negative voltage peak on V_{CC} pin after the loss of V_{CC} is ~81.6 µF. If the V_{CC} drop down to -90 V is accepted (still safe level in case of 100 V D_{GND} used), the capacitor value can be reduced to ~1.48 µF.

Bidirectional suppressor selection

A bidirectional suppressor can be used as an alternative to the capacitor. Following requirements must be fulfilled:

- Negative clamping voltage (absolute value considered)
  - Below the maximum reverse voltage of the GND network diode
  - Above the reverse battery requirement (-16 V)
- Positive clamping voltage
  - Above normal V_{BAT} range (0-16 V)
  - Above the Jump Start requirement (27 V for 60 s)
  - Above the Load Dump requirement (36 V for 400 ms)
- Energy capability
  - Must be compatible with standard ISO pulses 1, 2a, 3a, 3b
  - Must be able to withstand the demagnetization energy:
    Peak power dissipation (see calculation below)
    Discharge time (see calculation below)

Peak power dissipation on suppressor: $P_P = V_{CL} \cdot I_0$

Discharge (demagnetization) time: $T_{DEMAG} = \frac{L}{R} \cdot \ln\left(\frac{|V_{CL}| + R \cdot I_0}{|V_{CL}|}\right)$

where:

I_0: Load current at V_{CC} disconnection

V_{CL}: Clamping voltage of the suppressor device

R: Load resistance

Example of suppressor selection for given application conditions:

- Load inductance: L = 1 mH
- Load current: I_0 = 4 A
- Load resistance: R = 3.5 Ω
- Negative clamping voltage requirement: $|V_{CL}| < |-60\ V|$

Peak power dissipation:

$$P_P = V_{CL} \cdot I_0 = 60 \cdot 4 = 240W$$

Discharge (demagnetization) time:

$$T_{DEMAG} = \frac{L}{R} \cdot \ln\left(\frac{|V_{CL}| + R \cdot I_0}{|V_{CL}|}\right) = \frac{0.001}{3.5} \cdot \ln\left(\frac{60 + 3.5 \cdot 4}{60}\right) = 60\mu s$$

Bidirectional automotive TRANSIL SM4T39CAY-E (SMA package) selected:

- Peak pulse power rating: 400 W (10/1000 µs) OK (240 W at 60 µs required)
- Max. clamping voltage: +/-53.3 V at 7.5 A OK ($|V_{CL}| < |-60\ V|$ required)
- Min. breakdown voltage: +/-36.7 V at 1 mA OK (compatible with load dump)
- Compatibility with ISO pulses: OK (ISO pulse 1, 2a, 3a, 3b specified in datasheet)

Measurement example (VND7020AJ)

- V_{BAT}: 14 V
- Temperature: 25 °C
- Load
  - Ch 0: 1 mH, 3.5 Ω
  - Ch 1: No load connected
- Capacitor on device V_{CC} pin:
  - Option 1) 100 nF
  - Option 2) 100 nF + 2.2 µF (ceramic)
  - Option 3) 100 nF + 100 µF (electrolytic)
- GND network: Diode STPS2H100 + Resistor 4.7 k
- To be checked:
  - Make a Loss of V_{CC} during normal operation (mechanical disconnection of power supply while the channel is active – see test setup schematic)
  - Monitor following signals:
    V_{OUT} (Ch. 1 – Yellow)
    V_{CC} (Ch. 2 – Red)
    V_{GND} (Ch. 3 – Blue)
    I_{OUT} (Ch. 4 – Green)
    $V_{CC} – V_{GND}$: (F1 – Yellow) – Calculated by math. function

Figure 84. Test setup – loss of V_{CC} (monolithic)

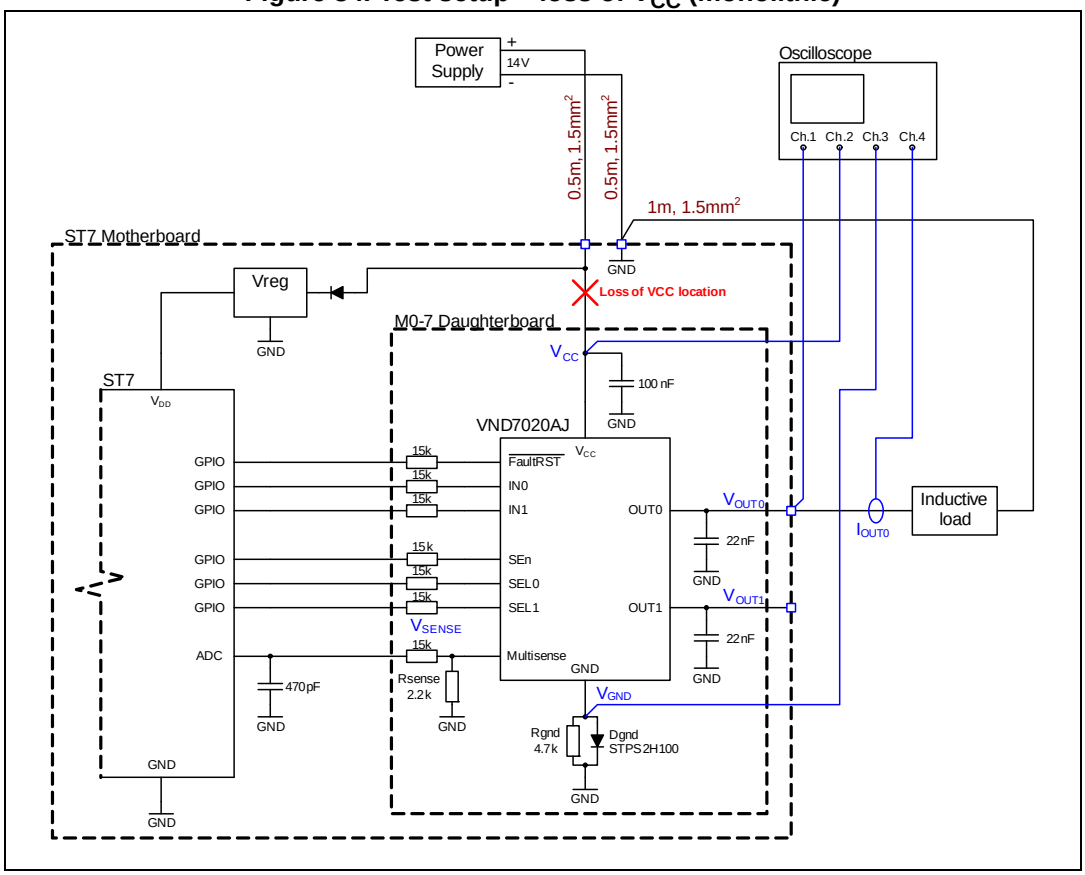
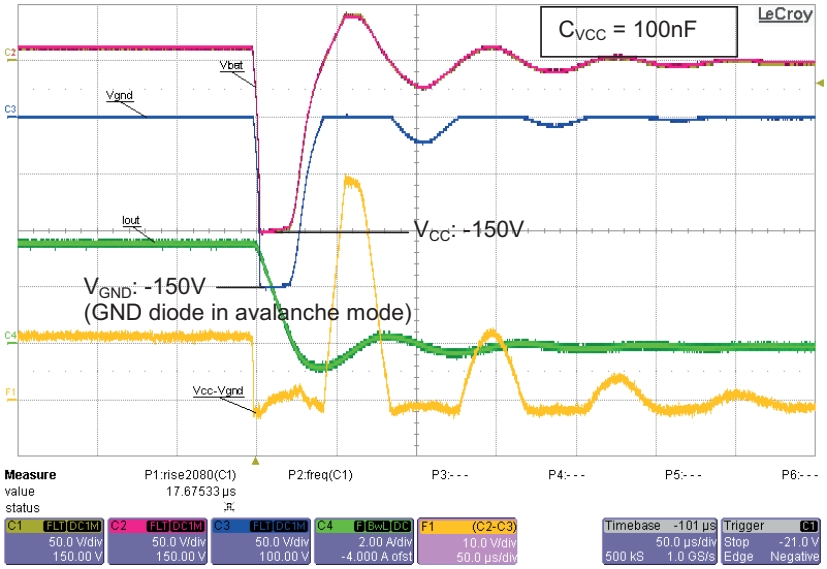
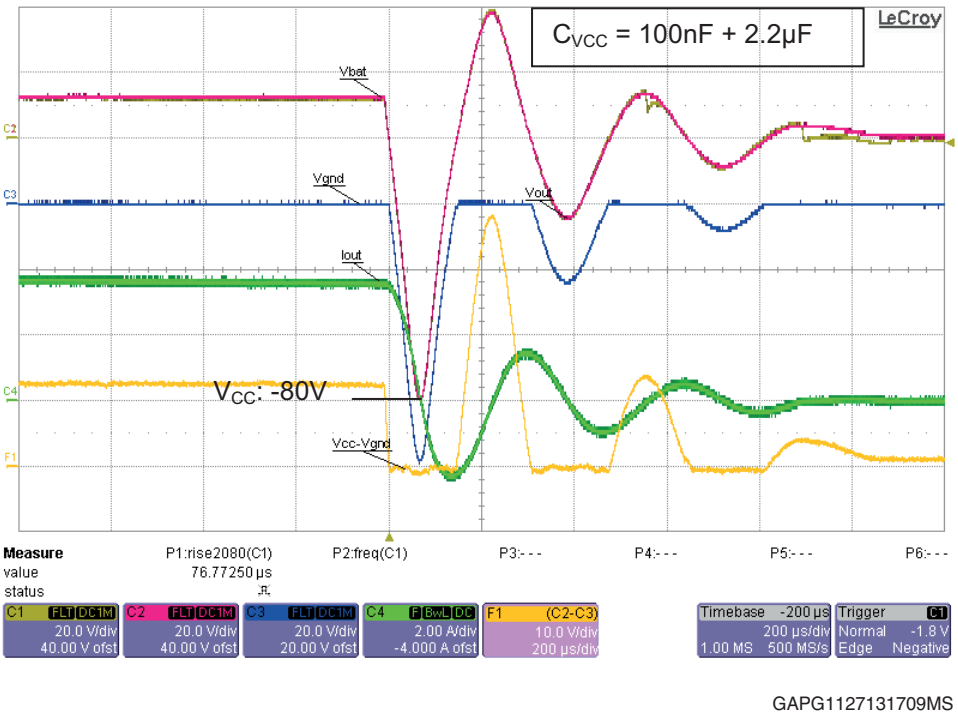


Figure 85. Loss of V_{CC} (VND7020AJ, 1 mH/ 3.5 Ω, 100 nF)



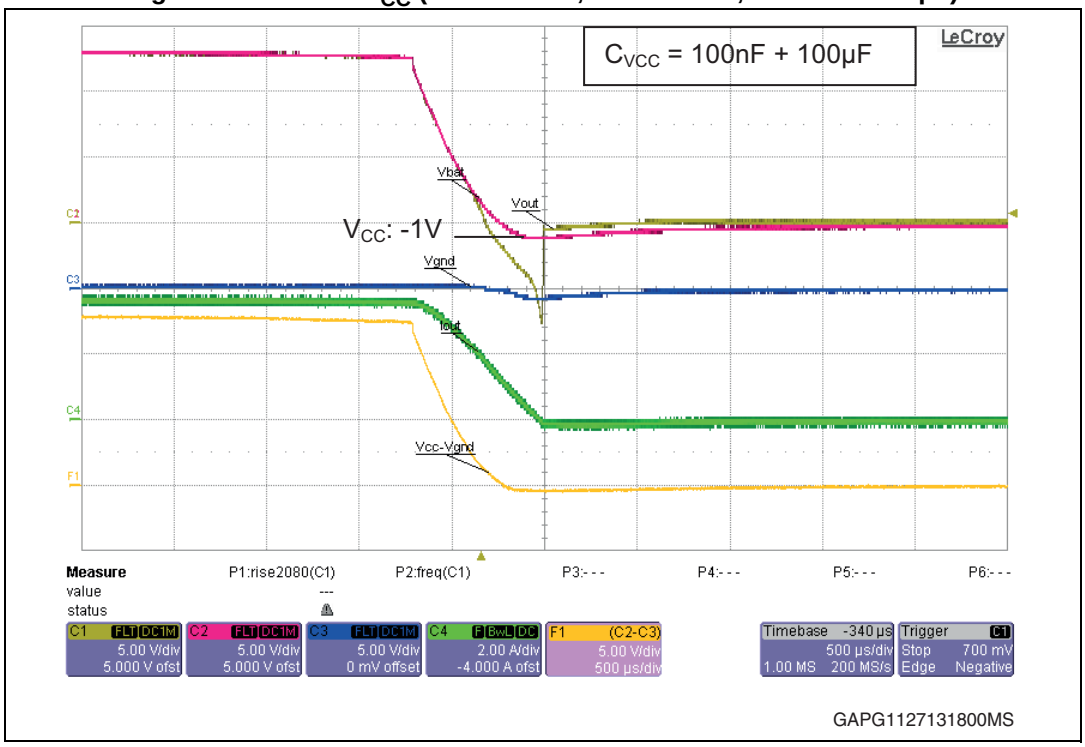
Most of the demagnetization energy (*Figure 85*) is absorbed by the GND network diode (in avalanche mode). The voltage peak on the V_{CC} and GND pin is ~-150 V (equal to break down voltage of the diode). The device channel stays on for whole demagnetization phase ~30 µs. A positive overshoot on V_{CC} is seen at the end of demagnetization phase, due to the resonance between the V_{CC} capacitor and load inductance.

Figure 86. Loss of V_{CC} (VND7020AJ, 1 mH/ 3.5 Ω, 100 nF + 2.2 µF)



Most of the demagnetization energy (*Figure 85*) is absorbed by the V_{CC} capacitor. The voltage peak on the V_{CC} pin is -80 V. The device channel stays on for the whole demagnetization phase ~80 µs. A positive overshoot on V_{CC} is seen at the end of demagnetization phase, due to the resonance between the V_{CC} capacitor and load inductance.

Figure 87. Loss of V_{CC} (VND7020AJ, 1 mH/ 3.5 Ω, 100 nF + 100 µF)



The demagnetization energy (*Figure 87*) is distributed between the device and V_{CC} capacitor. The turn-off phase is seen when the V_{CC} capacitor is discharged below undervoltage. Final voltage on V_{CC} is ~ -1 V.

7 MultiSense - analogue current sense

7.1 Introduction

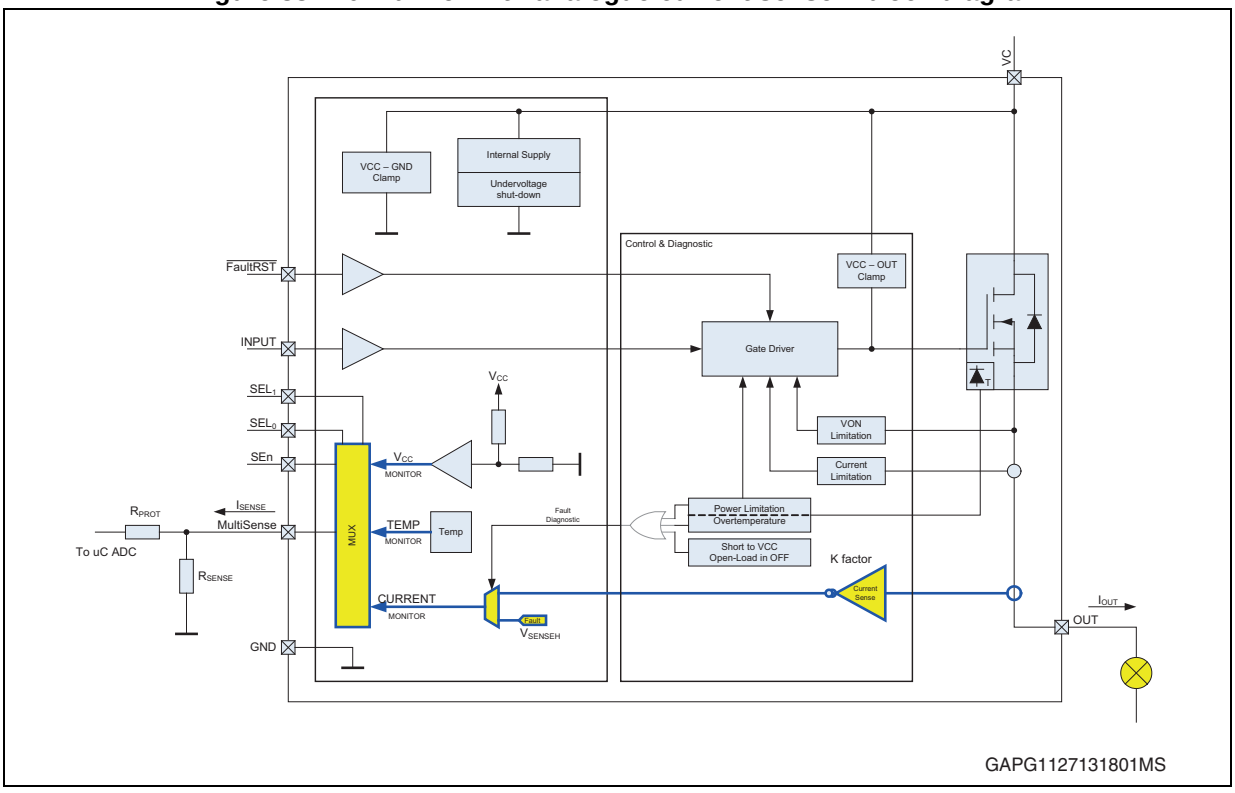
For diagnostic of M0-7 devices an analog monitoring output called MultiSense is used. It is multiplexing several analogue signals, controlled by SELx and SE_n pins.

Depending on the device family, these types of signals are provided:

- Current monitor-current mirror of channel output current
- V_{CC} voltage-scaled monitor of V_{CC}
- Case temperature-scaled chip temperature

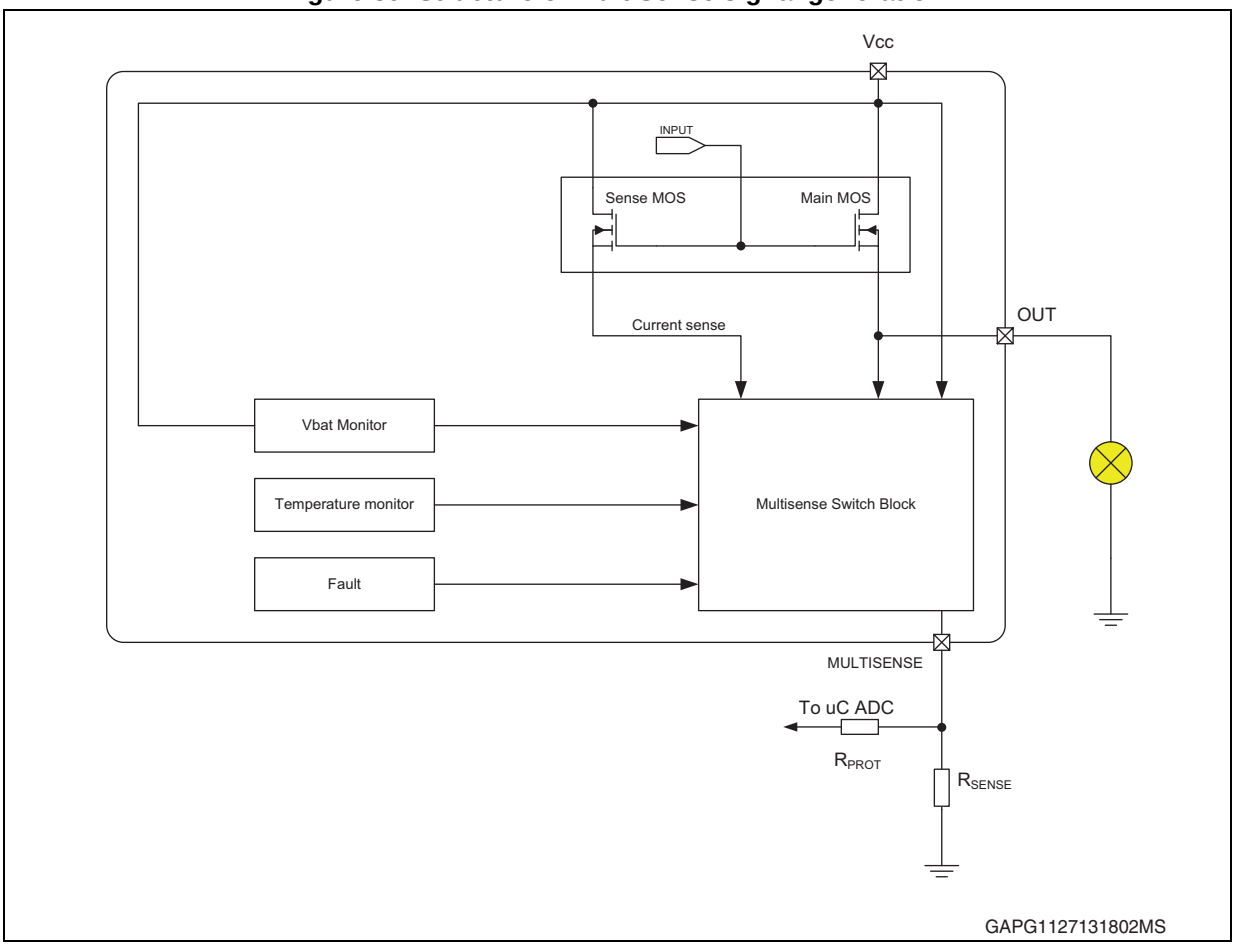
On top of these signals, it is possible to apply high Z state on MultiSense pin output when SE_n is set to low

Figure 88. M0-7 driver with analogue current sense – block diagram



7.2 Principle of MultiSense signal generation

Figure 89. Structure of MultiSense signal generation



In General, the MultiSense output signal operates for V_{CC} < 24 V

Current monitor

During no fault conditions (V_{OUT} > V_{OUT_MSD} - see datasheet value), the current flowing through Main MOS is mirrored through Sense-MOS. Sense-MOS is scaled down as a copy of the Main MOS according to a defined geometric ratio. Current is passed through MultiSense Switch Block fully decoupling MultiSense signal from output current.

In fault conditions, internal logic switches to MultiSense mode and delivers constant voltage on the output (named V_{SENSEH}).

Temperature, V_{BAT} monitor

Internal logic is switched to voltage output mode, applying output voltage corresponding to temperature or V_{CC} sensor (according to the selected signal).

7.2.1 Current monitor

When current mode is selected in the MultiSense, this output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to known ratio named K
- Diagnostics flag in fault conditions delivering fixed voltage with a certain current capability in case of
  - Power Limitation, Overtemperature in on-state
  - Short to V_{BAT} / Open-load in off-state (with external pull-up resistor) condition.

The current delivered by the current sense circuit can be easily converted to a voltage by using an external sense resistor, allowing continuous load monitoring and abnormal condition detection.

7.2.2 Normal operation (channel ON, no fault, SE_n active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using the following simple equations:

Current provided by MultiSense output: $I_{SENSE} = I_{OUT}/K$

while the Voltage on Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is the voltage measurable on R_{SENSE} resistor
- I_{SENSE} is the current provided from MultiSense pin in current output mode
- I_{OUT} is the current flowing through output
- K factor represents the ratio between Power MOS cells and Sense MOS cells; Its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE}.

7.2.3 Current monitoring range of linear operation

During the current monitoring the voltage on MultiSense pin will have a certain voltage depending on load conditions and R_{SENSE} value (as default value it can be assumed, for example, that MultiSense voltage at nominal load current is 2 V). Particular care must be taken for the correct dimensioning of the R_{SENSE} in order to ensure linearity in the whole load current range to be monitored (for different the full dimensioning rules on R_{SENSE} please see*Section 7.2.5: Failure flag indication*). In fact the current monitoring via MultiSense is guaranteed until a maximum MultiSense voltage of 5 V (defined as minimum value of V_{SENSE_SAT} in M0-7 datasheets)

Example 1: MultiSense voltage saturation

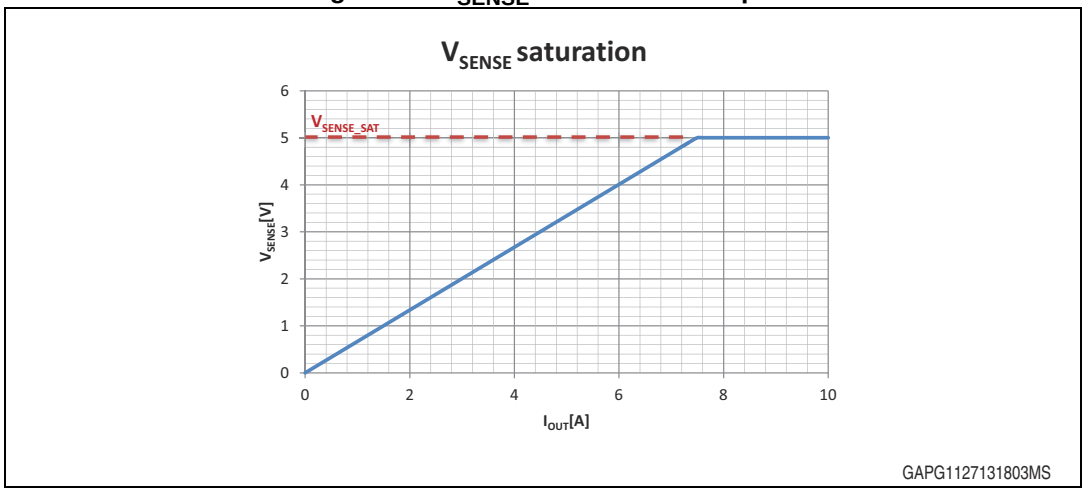
VND7020AJ R_{SENSE} selected in order to have V_{SENSE} = 2 V at I_{OUT} = 3 A

Considering (for sake of simplicity) K_2 at 3 A = 2755 (typical value) → I_{SENSE} = 1.089 mA → R_{SENSE} = 1.84 kΩ

Given a V_{SENSE_SAT} minimum (given in the datasheets) of 5 V, the maximum I_{SENSE} = 5 V/ 1.84 kΩ = 2.72 mA so to have still linearity, and assuming that K_2 remains constant, the maximum I_{OUT} ~ 7.5 A.

In other words, with the selected R_{SENSE} any load current greater than 7.5 A will produce the same V_{SENSE} (see *Figure 90*)

Figure 90. V_{SENSE} saturation example



Moreover care must be taken to prevent the current mirror output from saturation, then causing again the I_{SENSE} no longer to be proportional to I_{OUT}. This normally happens when the maximum current from the current mirror is reached and corresponds to the minimum value of the parameter I_{SENSE_SAT} (I_{SENSE_SAT} minimum, reported in the datasheets).

Example 2 MultiSense current saturation

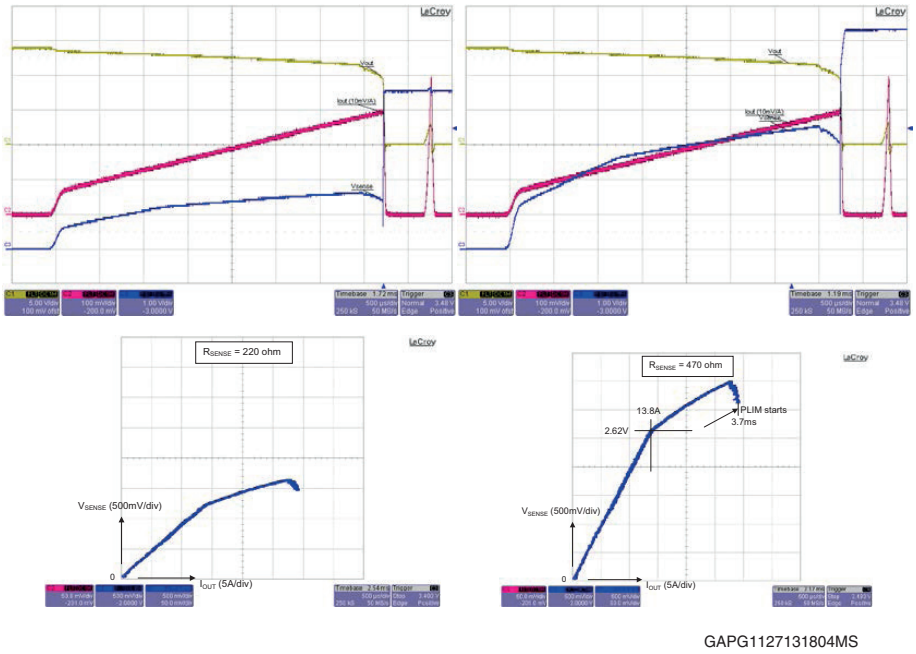
VND7020AJ R_{SENSE} selected in order to have V_{SENSE} = 2 V at I_{OUT} = 3 A

Considering an overload current of 6 A at 4 V of MultiSense pin Analog Voltage and I_{SENSE_SAT} = 4 mA minimum, R_{SENSE} has to fulfill the following formula:

$$R_{SENSE} > \frac{V_{SENSE}}{I_{SENSE\_SAT\_MIN}} = \frac{4V}{4mA} = 1k\Omega$$

In *Figure 91* a measurement of MultiSense of VND7040AJ is given. Two different low R_{SENSE} values are connected to the MultiSense pin and relevant linearity range of V_{SENSE} versus I_{OUT} is highlighted. In the measured sample the $I_{SENSE\_SAT} = V_{SENSE} / R_{SENSE}$ is about 5.4 mA corresponding to a maximum monitorable current of about 13 A.

Figure 91. Plotted V_{SENSE} with increasing I_{OUT} versus time with R_{SENSE} = 220 Ω (left) and R_{SENSE} = 470 Ω (right) for VND7040AJ and corresponding XY plot (V_{CC} = 14 V)



Note: V_{SENSE_SAT} and I_{SENSE_SAT} minimum values are guaranteed for the minimum V_{CC} voltage in which all K factor limits are guaranteed (in datasheets this is 7 V) and maximum operating junction temperature (in datasheets this is 150 °C) which represent worst case conditions in the assessment of the maximum load current to be monitored. Experimental Measurements on samples have.

In *Figure 92* and *Figure 93* plots extracted from experimental data at 25 °C are shown for V_{SENSE_SAT} and I_{SENSE_SAT} respectively. The Voltages in the plots refer to module GND so they include the voltage drop on GND network of about 300 mV.

Figure 92. Behavior of V_{SENSE_SAT} vs V_{CC}

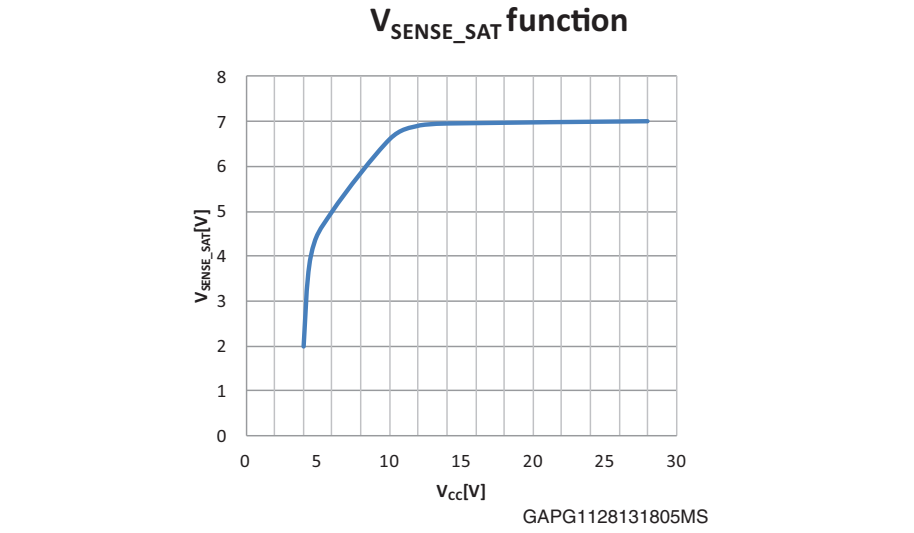
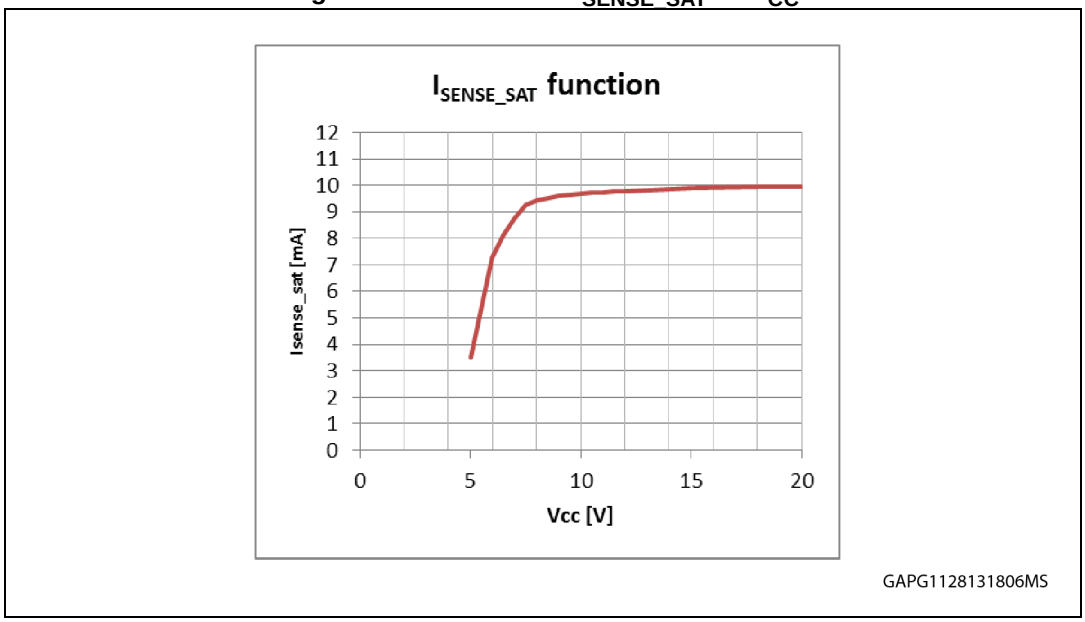


Figure 93. Behavior of I_{SENSE_SAT} vs V_{CC}



The I_{SENSE_SAT} decreases significantly for V_{CC} below about 10 V. Above this battery level we can consider as minimum value of I_{SENSE_SAT} = 5.2 V (instead of the minimum of I_{SENSE_SAT} = 4 mA given in the datasheets at V_{CC} = 7 V). This increases the upper load current range that can be monitored by the current sensing avoiding any saturation

Note: The MultiSense current monitoring linear behavior is featured down to a V_{CC} = 4.5 V and for $V_{SENSE} < V_{CC} - 1.5$ V (even though relevant specification limits reported in datasheets are not guaranteed anymore).

7.2.4 Impact of the output voltage to the MultiSense output

The current sense operation for load current approaching the current limitation is not guaranteed and predictable. Indeed, because of the intervention of the current limiter, the output voltage can drop significantly, up to approximately 0 V in the extreme case of a hard short circuit.

Being the whole circuit referred to V_{OUT}, ambiguous and unreliable current values could be sourced by the MultiSense under such conditions.

In order to bring the MultiSense into a defined state, a dedicated circuit section shuts down the current sense circuitry when V_{OUT} drops below the threshold V_{OUT_MSD} (typically 5 V).

In conclusion, in normal operation the current sense works properly within the described border conditions. For a given device, the I_{SENSE} is a single value monotonic function of the I_{OUT} as long as the maximum V_{SENSE} (1st example) or the current sense saturation (2nd example) are reached, i.e. there's no chance to have the same I_{SENSE} for different I_{OUT} within the given range.

7.2.5 Failure flag indication

In case of Power Limitation or overtemperature or open load/short to V_{CC} in OFF state, the fault is indicated by the MultiSense pin which is switched to a "current limited" voltage source.

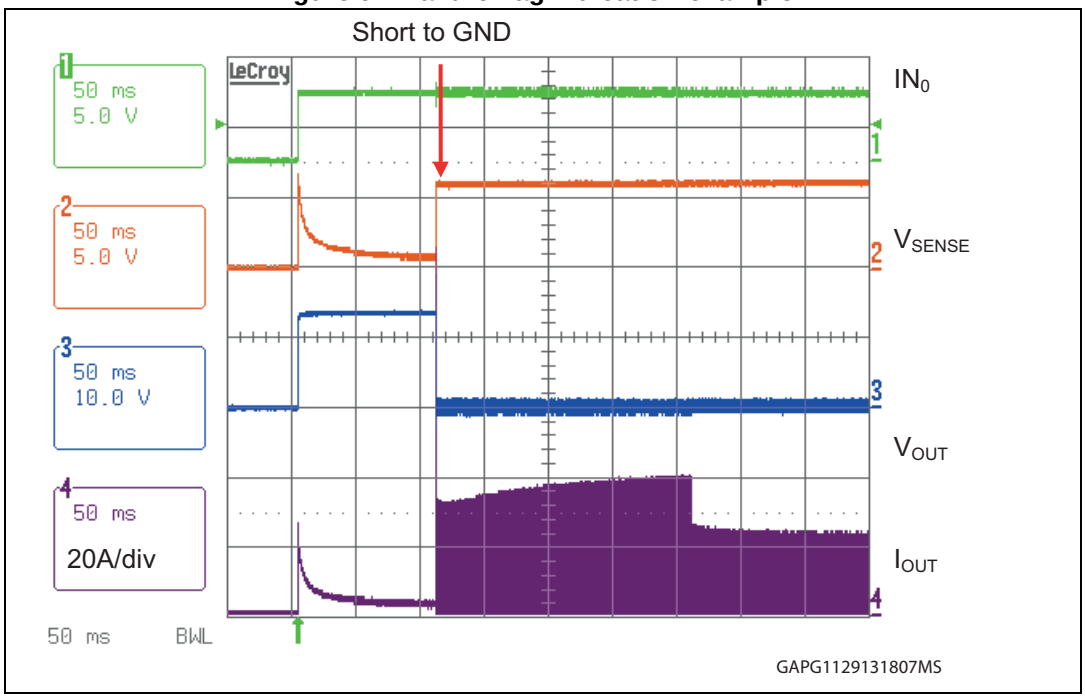
Indeed, with reference to *Figure 89* whenever a Power Limitation/overtemperature condition is reached, The MultiSense output is internally pulled up to V_{SENSEH}.

The MultiSense output, in those events is controlled in such a way to develop at least a voltage of V_{SENSEH} (given in the datasheet) across the external sense resistor.

In any case, the current sourced by the MultiSense in this condition is limited to the I_{SENSEH} (given in the datasheet). In order to allow the current sense pin to develop at least V_{SENSEH} = 5 V, a minimum sense resistor value must be set (for details see *Section 7.2.6: Considerations on MultiSense resistor choice for current monitor*).

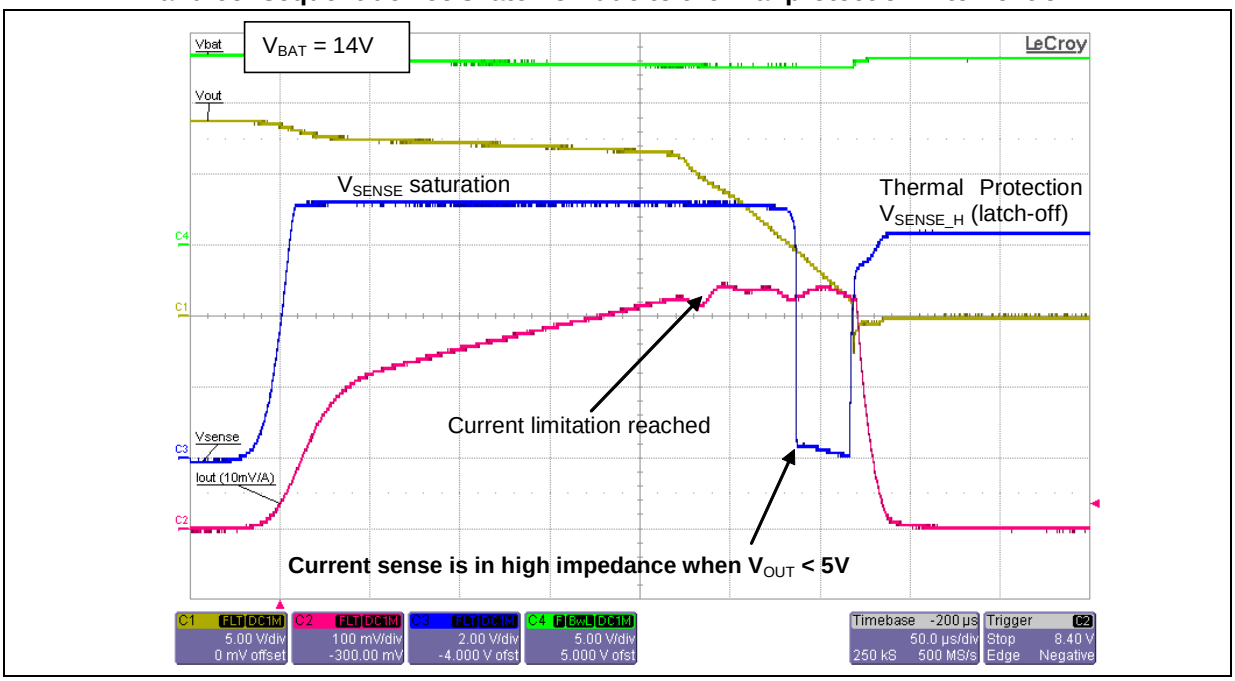
The typical behavior of a M0-7 high-side driver in case of overload or hard short circuit is shown in the following figures (FaultRST set low so to indicate autorestart mode):

Figure 94. Failure flag indication-example 4



An example of a condition with a progressive increase of the output current (single shot ramp) by an electronic load supplied by VND7040AJ is shown in *Figure 95*. Sense resistor is 2.2 kΩ. Device is set in latch-off mode. The saturation voltage V_{SENSE_SAT} is reached and then the current limitation I_{LIM_H}: afterwards the Thermal protection acts. As soon as the output voltage falls down below about 5 V (parameter V_{OUT_MSD} in the datasheet) the MultiSense pin goes in high impedance, as previously explained, until the first power limitation peak is reached. At this point the MultiSense pin is reactivated again and the V_{SENSE_H} voltage is issued and latched. Since, in this case, the FaultRST pin is set high (latch off) the PowerMOS remains off.

Figure 95. MultiSense operation of VND7040AJ in current monitoring with increasing overload and consequent device's latch off due to thermal protection intervention



7.2.6 Considerations on MultiSense resistor choice for current monitor

In normal operating conditions, the following equation describes relation between I_{OUT} and V_{SENSE}

Equation 8

$$V_{SENSE} = R_{SENSE} I_{SENSE} = R_{SENSE} \frac{I_{OUT}}{K} [V]$$

Design value of Sense Resistor can be calculated from the above equation given the intended voltage at the ADC with the nominal load current and the typical K factor of the device.

The calculated sense resistor implies the following considerations that the Hardware Designer has to take into account:

1. In normal operating conditions, in order not to reach MultiSense voltage saturation V_{SENSE_SAT}, with the maximum load current that can be read I_{OUT_MAX}, the R_{SENSE} has to fulfill the following equation:

Equation 9

$$R_{SENSE} < K_{MIN} \frac{V_{SENSE\_SAT\_MIN}}{I_{OUT\_MAN}} [V]$$

Within this maximum current linearity of MultiSense is guaranteed. If a lower maximum load current needs to be read, like for example LED string, the R_{SENSE} value must be increased.

2. In normal operating conditions, the maximum sense voltage that can be read with the given R_{SENSE} must be higher than a certain ADC threshold. This can be expressed by the following equation:

$$R_{SENSE} > \frac{V_{SENSEMAX}}{I_{SENSE\_SAT\_MIN}}$$

Where $V_{SENSEMAX}$ is the maximum voltage that the ADC has to read at the maximum monitored load current. This value can be below or equal to 5 V which normally is the maximum operating range of the ADC.

3. In fault conditions (overload, short-circuit to GND that cause Power Limitation or Thermal Shutdown and in Open Load/Short to Battery in OFF state), in order to be able to differentiate a normal operating condition from a Fault condition, the MultiSense pin must be capable of developing a voltage above the V_{SENSEH} (Value given in the datasheet, V_{SENSEH} = 6 V typically). Therefore the following condition must be fulfilled:

Equation 10

$$R_{SENSE} > \frac{V_{SENSE\_H\_min}}{I_{SENSE\_H\_min}}$$

4. Finally the current sense resistor is necessary to protect the MulitSense pin in case of reverse battery. During this event, for monolithic devices an intrinsic diode between MultiSense and V_{CC} pins is forward biased and the resulting current must be limited (in the datasheet the maximum MultiSense current that can flow in reverse battery condition is indicated in the absolute maximum ratings table). This value is given in the Absolute Maximum Ratings section of M0-7 datasheets (I_{SENSE} value, in case of VND7020AJ this is 20 mA), therefore the minimum R_{SENSE} to protect the MultiSense pin in case of reverse battery (supposing a static condition of V_{CC} = -16 V) is:

$$R_{SENSE} > \frac{-V_{CC} - V_F}{I_{SENSE\_rev\_max}} = \frac{16V - 0.7V}{20mA} = 765\Omega$$

5. The above given R_{SENSE} = 765 Ω is suitable as well to protect the current sense circuit against pulse 1, up to level IV (ISO 7637-2 (E): 2004 and 2011)

In conclusion the R_{SENSE} value must fulfill two opposite conditions for having linearity in normal operating condition: one is avoiding MultiSense pin current saturation (increase R_{SENSE}) and the other is avoiding MultiSense pin voltage saturation (decrease of R_{SENSE}). Moreover the R_{SENSE} value has to be dimensioned in order to distinguish a normal operating condition (linear mode V_{SENSE} proportional to load current) from a Fault condition (Constant Voltage Generator developing V_{SENSE_H} across the R_{SENSE}).

In Chip Temperature and V_{CC} monitor mode the MultiSense is a voltage source with limited current but in this case the current saturation is higher than the I_{SENSE_SAT} so linearity in T_{CHIP} and V_{CC} reading is respected with the minimum R_{SENSE} which fulfills the recommendation of point b). In *Figure 96* and *Figure 97* experimental plots on a VND7140AJ are shown in typical conditions for the T_{CHIP} and V_{CC} monitor versus R_{SENSE} respectively.

Figure 96. MultiSense in T_{CHIP} mode behavior versus R_{SENSE} for VND7140AJ at V_{CC} = 14 V and T_C = 25 °C

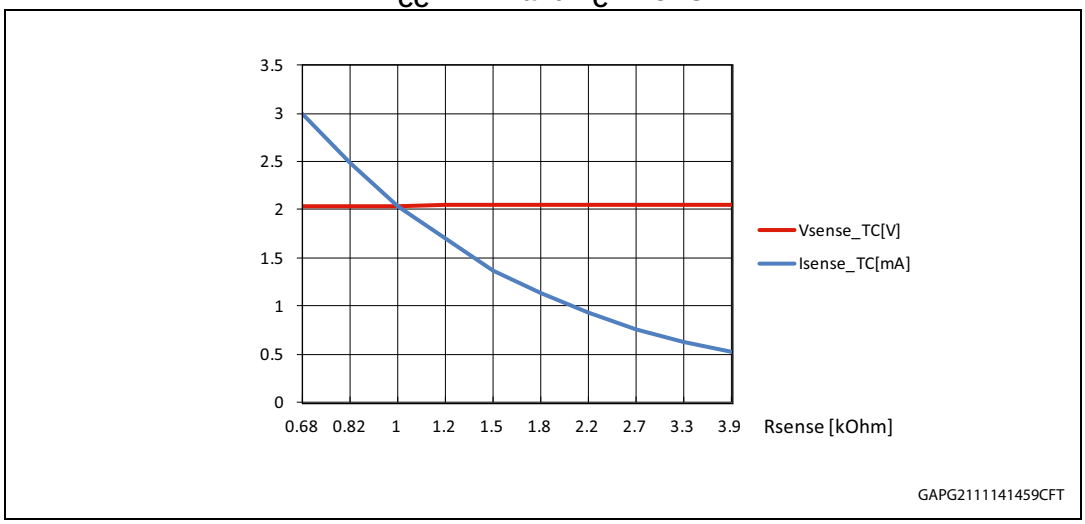
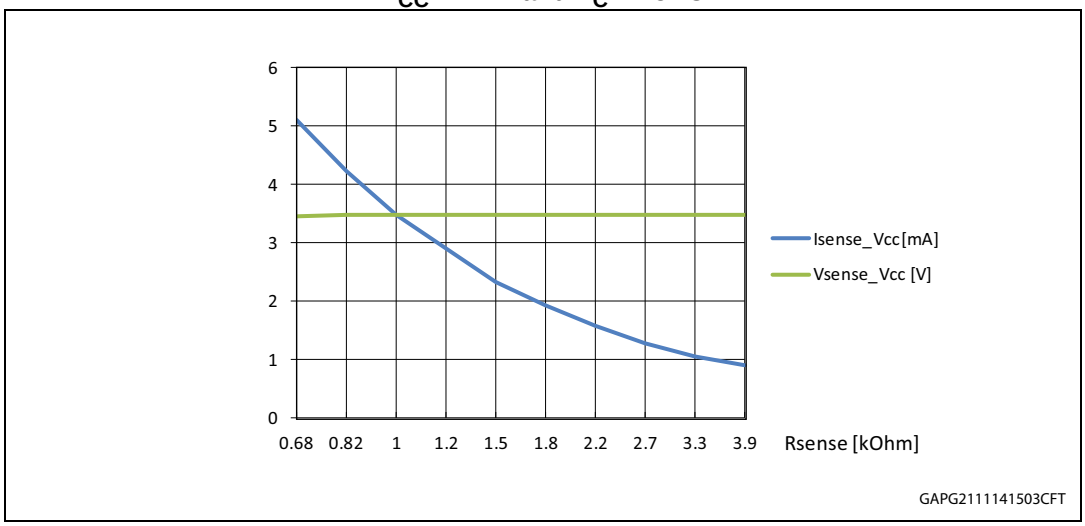


Figure 97. MultiSense in V_{CC} mode behavior versus R_{SENSE} for VND7140AJ at V_{CC} = 14 V and T_C = 25 °C



An example about R_{SENSE} value definition is shown:

Example 3:

Let's consider the VN7016AJ (16 mΩ HSD) with a nominal load current I_N = 5 A which corresponds to an intended V_{SENSE} = 2 V and typical K_2 = 3750 (from datasheet). Let us apply above *Equation 8*:

$$R_{SENSE} = K \cdot \frac{V_{SENSE}}{I_{OUT}} = 3750 \cdot \frac{2}{5} = 1.5k\Omega$$

Let us suppose that the maximum load current the ADC has to monitor in linearity is 2 times the nominal current so to say 10 A at $V_{SENSEMAX}$ = 4 V. So this means that neither V_{SENSE_SAT} nor I_{SENSE_SAT} must be reached and in fault conditions a voltage above 5 V must be issued. Let us verify that R_{SENSE} value chosen is the correct one by applying above

Equation 9, and *Equation 10*:

$$R_{SENSE} < K_{3MIN} \cdot \frac{V_{SENSE\_SAT\_MIN}}{I_{OUT\_MAN}} \approx (3750 - 3750 \cdot 0.18) \cdot \frac{5}{10} = 1.54k\Omega$$

$$R_{SENSE} > \frac{V_{SENSEMAN}}{I_{SENSE\_SAT\_MIN}} = \frac{4V}{4mA} = 1k\Omega$$

$$R_{SENSE} > \frac{V_{SENSE\_H\_min}}{I_{SENSE\_H\_min}} = \frac{5V}{7mA} = 714\Omega$$

So the chosen sense resistor of 1.5 kΩ is correct.

7.2.7 Usage when multiplexing several devices

If several devices are supposed to share one R_{SENSE} resistor, for proper diagnostic only one MultiSense of each device at a time should be activated.

All other devices sharing the R_{SENSE} should apply the High-Z state on MultiSense output (SE_n = L). In this case, R_{SENSE} is supplied from one device at a time.

If, by mistake more than one MultiSense is activated, the MultiSense output in current mode will draw a current in the shunt resistor R_{SENSE} defined as:

$$I_{SENSE} = \sum I_{SENSE[N]}$$

where [N] is number of devices with enabled current output

There must be considered the possibility of V_{SENSE} saturation (range of linear operation), since current delivered from multiple devices increase voltage drops on R_{SENSE}.

In case one device is switched to voltage output (due to fault condition), diagnostic for other devices cannot be applied (since V_{SENSEH} is applied to R_{SENSE})

7.2.8 LED diagnostic

VNQ7040AY device (Quad channels) contains a feature consisting in a switch able output mode selected through dedicated control pin LEDx according to the connected load (Bulb/LED).

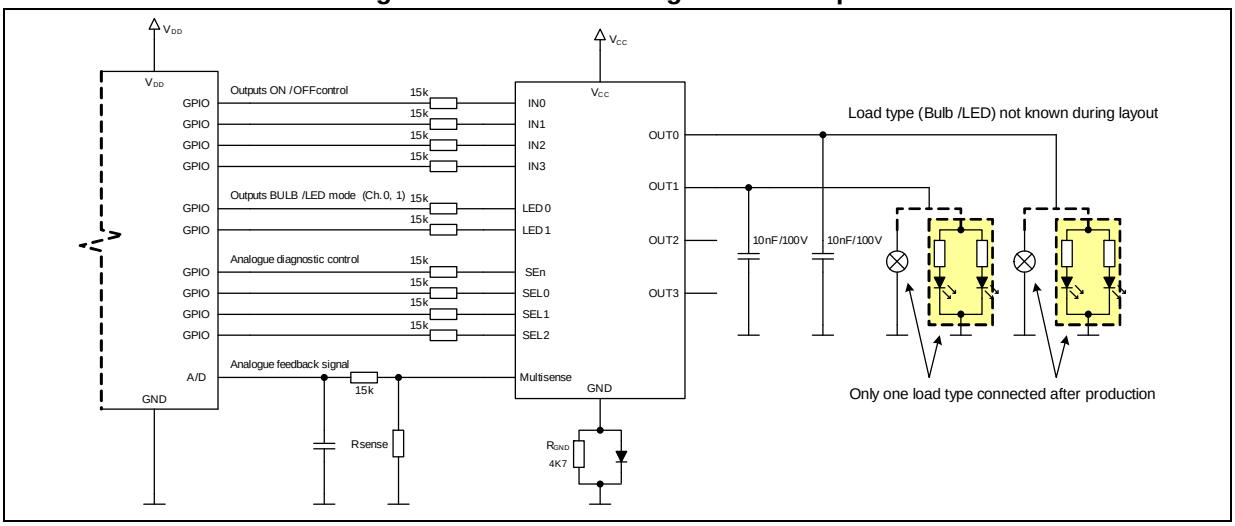
Several output parameters are influenced according to the selected mode (Bulb/LED):

- K factor for current sense monitoring
- I_{LIMH}, I_{LIML} as well as
- dV/dt slopes for rising and falling edges

For applications, where output type is not known in advance, it is possible drive LED_x pin by microcontroller pin (applying appropriate protection - see relevant chapter).

Then output mode (parameters) can be adjusted even after PCB production by SW modification inside microcontroller.

Figure 98. Bulb / LED diagnostic example



Diagnostic in OFF state

Considering diagnostic of LED loads, it can appear specific situation during diagnostic in OFF state. While pull-up resistor is applied during OFF state diagnostic (allowing distinguish between output “short to V_{CC}” and “open-load”), current flowing through pull-up resistor can create unintended LED light emission.

To prevent such a situation, external circuitry inside the LED load, or a pull-down structure on device level is needed to create sufficient load for detection, without side effect of LED lightning.

Without external circuitry on LED loads, diagnostic in off state is not recommended.

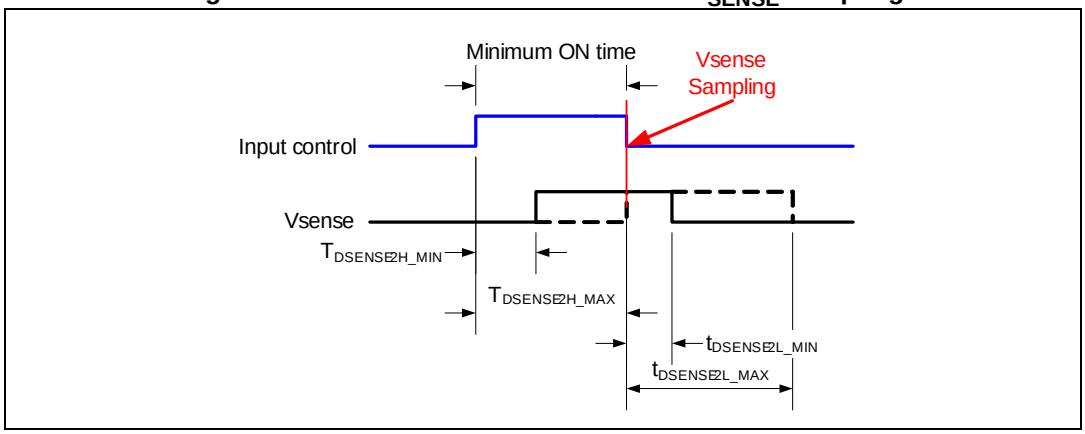
Diagnostic in ON state

Since LED loads are usually driven by PWM signal at low duty cycle, limitations for diagnostic in ON state can arise.

Considering the spread of time delay between Input switched and current sense output signal (specified in datasheet by $T_{DESENSE2H}$), there is a minimum required ON time, for which diagnostic is possible:

Minimum duty cycle calculation

Figure 99. Minimum ON time for correct V_{SENSE} sampling



$t_{DSENSE2H}$ ~250 µs (maximum datasheet value)

$t_{ON\_MINIMUM} = t_{DSENSE2H} = 250$ µs

Considering PWM frequency 200 Hz →T_{PERIOD} = 1/200 Hz = 5 ms

Duty cycle corresponding to $t_{ON\_MINIMUM}$ = 100% * (250 / 5000) = 5%

Result: At PWM frequency 200 Hz, minimum duty cycle is 5 % for valid V_{SENSE} diagnostic.

Minimum operating current

Distinguishing between open load and minimum load is possible without calibration.

Taking reference values of VND7020AJ datasheet: minimum K_{OL} = 1020 at specified current of 10 mA, considered as maximum failure current gives maximum:

$$I_{OL\_SENSE\_MAX} = \frac{0.01A}{1020} = 9.8\mu A$$

For output current of 0.1 A, considered as detectable load I_{SENSE}, the minimum and maximum sense current can be calculated as follows:

$$I_{SENSE\_MIN} = \frac{I_{OUT}}{K_{LED\_MAX}} = \frac{0.1A}{5100} = 19\mu A$$

$$I_{SENSE\_MAX} = \frac{I_{OUT}}{K_{LED\_MIN}} = \frac{0.1A}{1800} = 55\mu A$$

Results show that differentiation between open load of 10 mA and minimum load current of 100 mA is possible without calibration.

Diagnostics with different load options

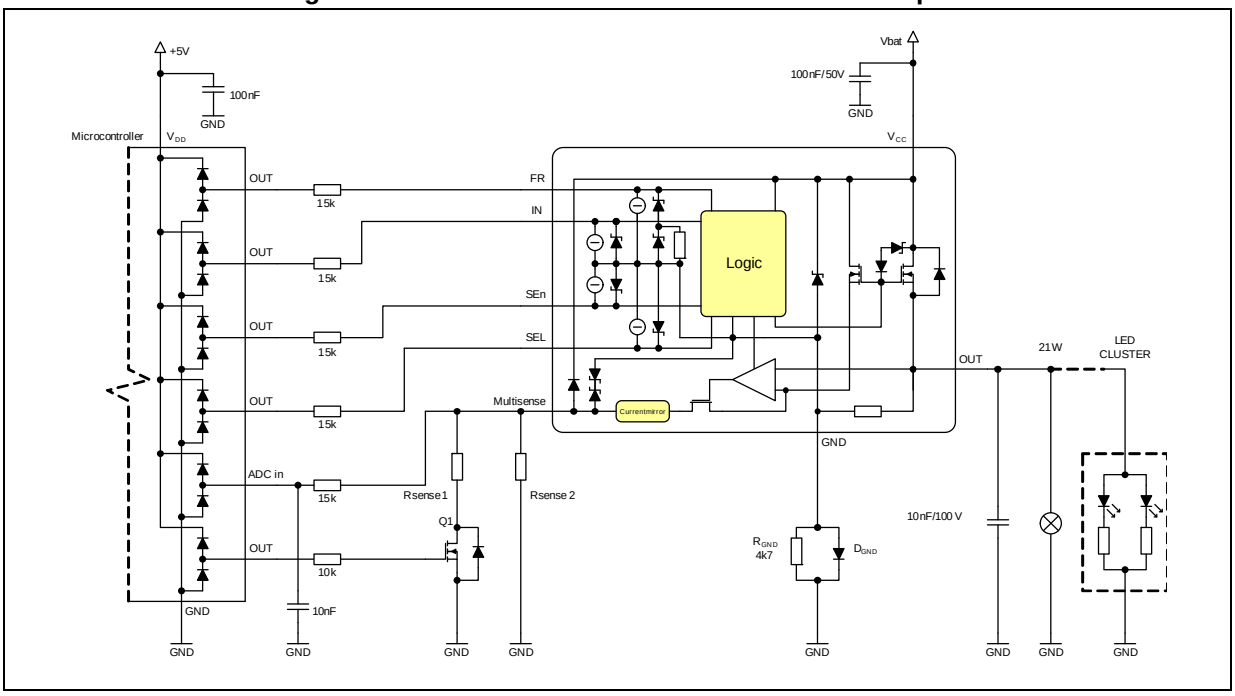
In some cases the requirement profile asks for alternative loads driven with one and the same high-side driver. This could be a bulb lamp with the alternative of an LED (- cluster). In this case the driver:

- Has to handle the high inrush current of the bulb load
- Has to provide a power dissipation low enough during continuous operation
- Must not indicate an open load in case of an LED (-cluster) is applied instead of a bulb.

In case of different load options (Bulb/LED) there is the possibility to use two different (switch able) sense resistors in order to have the current sense band in the appropriate range matching the different load currents.

An example of a current sense resistor switching circuit can be seen in the *Figure 100*. The measured scale can be extended by R_{SENSE1} switched in parallel to R_{SENSE2} by MOSFET Q1.

Figure 100. Switched current sense resistor–example



7.2.9 Diagnostic with paralleled loads / partial load detection

Table 24. Paralleling bulbs – overview on the example of VND7020AJ

Configuration	Failure type detection
2x21W	Failure of one 21 W detectable without calibration
2x27W	Failure of one 27 W detectable without calibration
21W + 5W	Failure of 21 W detectable without calibration, failure of 5 W cannot be detected
2x21W + 5W	Failure of one 21 W bulb can be detected without calibration only above 10 V battery voltage, assuming that a missing 5 W bulb must not trigger the failure diagnostic

Table 24. Paralleling bulbs – overview on the example of VND7020AJ (continued)

Configuration	Failure type detection
2x27 W + 5 W	Failure of one 27 W detectable without calibration, failure of 5 W cannot be detected
2x21 W + 5 W	Failure of one 21 W bulb can be detected with calibration, assuming that a missing 5 W bulb must not trigger the failure diagnostic

The *Table 24* shows a set of cases where bulbs in parallel, driven by the suitable M0-7 HSD (see as reference *Table 20* in *Section 6.1: Bulbs*) channel are used. The M0-7 HSD family allows the detection of individual bulb failures when in a parallel arrangement. However, if we consider the bulb wattage spread, the HSD K-factor tolerance, the variation of bulb currents vs. V_{BAT} and the resolution of the ADC it is clear that accurate failure determination can be difficult in some cases. For example if there are bigger and smaller bulbs paralleled the detection limit for the lowest power bulb is lost in the tolerances.

In order to achieve better current sense accuracy, the current sense calibration (K factor measurement) of each HSD can be adopted.

7.2.10 K factor calibration method

In order to reduce the V_{SENSE} spread, it is possible to reduce the K spread and eliminate the R_{SENSE} variation by adding a simple test (calibration test) at the end of the module production line.

Single point calibration on low current

K factor can be calibrated in “single point” by measurement of I_{SENSE} for specified I_{OUT}.

K is then calculated as

$$K_{CALIBRATED} = \frac{I_{OUT}}{I_{SENSE}}$$

For low currents diagnostic using single point calibration method, it is possible distinguish between open-load (<10 mA) and low current (limit depending on device R_{DSON}; for example VND7020AJ datasheet specifies low current level > 50 mA).

For calibration of K factor at I_{OUT} = 30 mA, T_j = 25 °C and V_{CC} = 13 V, in the datasheet of VND7020AJ there is specified a maximum drift of K factor ±30 % in range I_{OUT} = 10 to 50 mA, temperature range of T_j = -40 ºC to 150 ºC and battery range V_{CC} = 7 V to 18 V.

All these parameters allow clear distinguishing between minimum and maximum I_{OUT} within specified range.

Following example shows detection thresholds with no overlapping zone between maximum V_{SENSE} corresponding to open load threshold (at 10 mA) and minimum V_{SENSE} corresponding to minimum load (at 50 mA)

Example 4

I_{OUT} = 30 mA

R_{SENSE} = 2.2 kΩ

V_{SENSE} = 17.6 mV – measured value

$$K_{CALIBRATED} = \frac{I_{OUT}}{I_{SENSE}} = \frac{I_{OUT}}{\frac{V_{SENSE}}{R_{SENSE}}} = \frac{30mA}{\frac{17.6mV}{2.2k\Omega}} = 3750$$

$$K_{MIN} = K_{CALIBRATED}(-30\%) = 3750 \cdot 0.7 = 2625$$

$$K_{MAN} = K_{CALIBRATED}(30\%) = 3750 \cdot 0.7 = 2625$$

Maximum V_{SENSE} level for open-load detection is then

$$K_{SENSE\_OL} = R_{SENSE} \cdot \frac{I_{OUT}}{K_{MIN}} = 2200 \cdot \frac{10mA}{2625} = 8.4mV$$

And following minimum V_{SENSE} for low current load (at 50 mA)

$$K_{SENSE\_LOAD} = R_{SENSE} \cdot \frac{I_{OUT}}{K_{MAX}} = 2200 \cdot \frac{50mA}{4819} = 22.6mV$$

Considering 12-bit A/D converter for V_{SENSE} monitoring with error of 2LSB bits and measurement range 0 - 5 V, gives precision

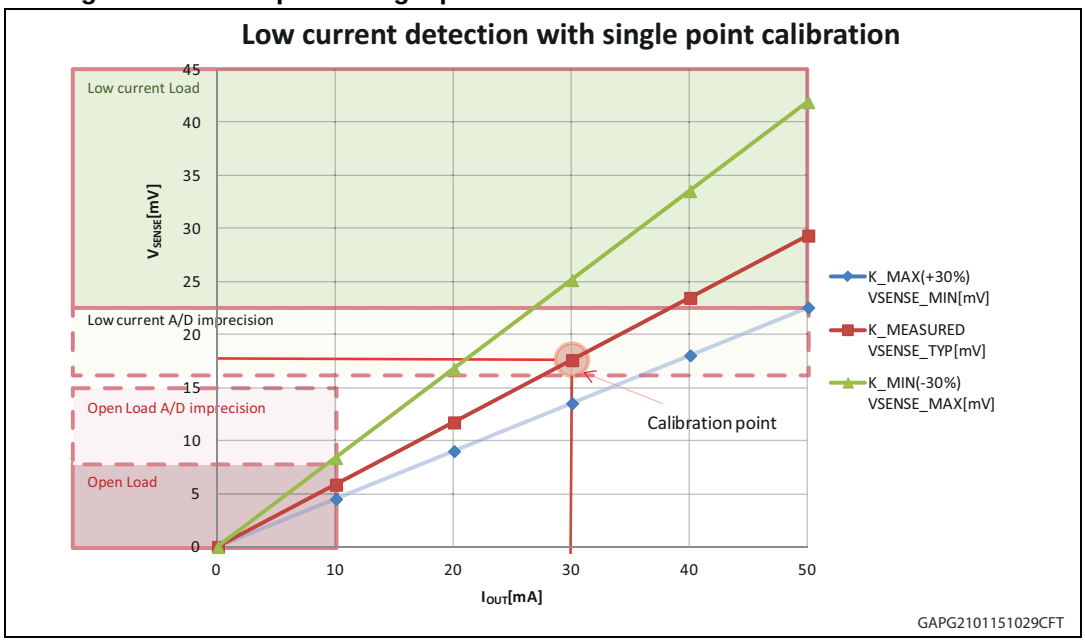
$$\pm 2(LSB) \cdot \frac{5V}{4096} = \pm 2mV$$

Considering a maximum leakage of +/-0.3 µA of the ADC, this causes on the 15 kΩ ADC series resistor, an error on ADC voltage of +/- 4.5 mV. Even applying these errors, result is a non-overlapping thresholds for detection of:

- Open-load (I_{OUT} < 10 mA),
  where V_{SENSE} < 8.4 mV +/- 2 mV +/- 4.5 mV → Max 14.9 mV
- Minimum load (I_{OUT} > 50 mA),
  where V_{SENSE} > 22.6 mV +/- 2 mV +/- 4.5 mV → Min 16.1 mV

Figure 101 gives a graphical explanation of the *Example 4*.

Figure 101. Example of single point calibration at low current for VND7020AJ



Two points calibration - How the calibration works

To calibrate means to measure on a specific device soldered in a module the K ratio at a given output current by a V_{SENSE} reading. Since the relation of $I_{OUT} = I_{SENSE} \cdot K$ is known it is then easy to calculate the K ratio. However, even if the K ratio measured in a single point eliminates the parametric spread, it doesn't eliminate the V_{SENSE} variation due to the K dependency on output current.

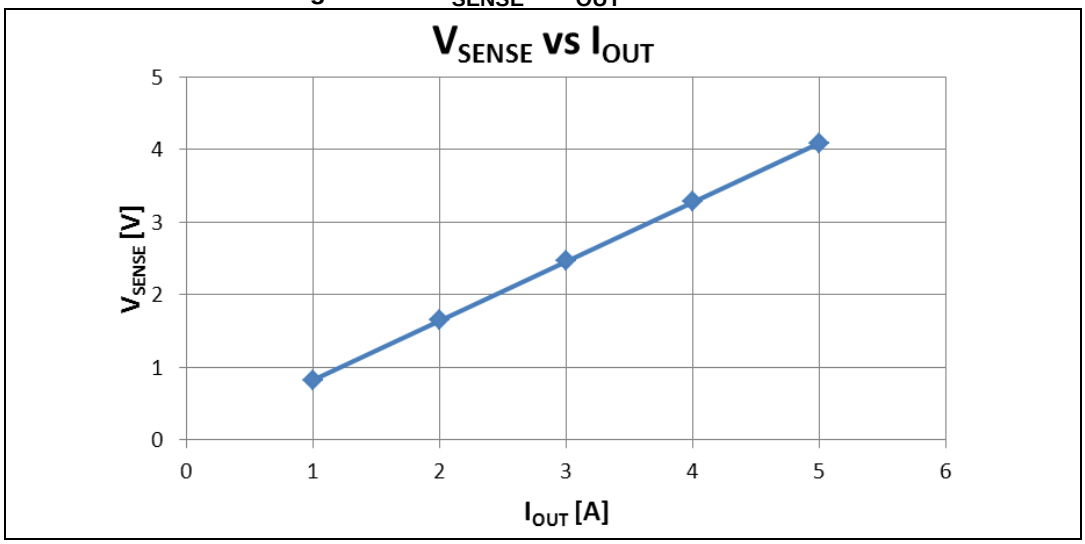
This variation can be eliminated doing the following considerations:

Table 26 and *Figure 102* show a V_{SENSE} measurement on a sample of VND7020AJ with R_{SENSE} = 2.2 kΩ.

Table 25. V_{SENSE} measurement

I_{OUT} [A]	V_{SENSE} [V]
1	0.823
2	1.647
3	2.465
4	3.283
5	4.090

Figure 102. V_{SENSE} vs I_{OUT} measurement



The trend is almost linear in the application range and then we can approximate the V_{SENSE} trend with the following equation:

Equation 11

$$V_{SENSE} = m \cdot I_{OUT} + a$$

Where “m” [Ω] is the rectangular coefficient and “a” [V] is a constant.

By inverting this equation it is easy to get a relation where the output current can be calculated as:

Equation 12

$$I_{OUT} = M \cdot V_{SENSE} + b$$

Instead of $I_{OUT} = I_{SENSE} \cdot K$ once M [S] and b are known, it is possible to evaluate the I_{OUT} with a high accuracy leaving only the spread due to the temperature variation.

The current sense ratio maximum fluctuation is expressed in the datasheet with the parameter dK/K (maximum relative error in the full MultiSense V_{CC} and T_j specification range versus K at V_{CC} = 13 V and T_j = 25 °C).

How to calculate M and b

To calculate M and b two simple measurements, done at the end of the production line, are needed. Chosen two reference output currents, I_{REF1} and I_{REF2}, the relevant V_{SENSE1} and V_{SENSE2} have to be measured. Then these 4 values can be stored in an EEPROM in order to let the microcontroller use this information to calculate M and b using the simple formulas reported below.

Since we defined $I_{OUT} = M \cdot V_{SENSE} + b$ it is also true that:

Equation 13

$$I_{REP1} = M \cdot V_{SENSE1} + b$$
$$\text{and}$$
$$I_{REP2} = M \cdot V_{SENSE2} + b$$

Solving these two equations we get the following relations:

Equation 14

$$I_{OUT} = M \cdot V_{SENSE} + b$$
$$M = \frac{I_{REF1} - I_{REF2}}{V_{SENSE1} - V_{SENSE2}}$$
$$b = \frac{I_{REF2} \cdot V_{SENSE1} - I_{REF1} \cdot V_{SENSE2}}{V_{SENSE1} - V_{SENSE2}}$$

Example 5: M, b calculation for the chosen device

Fixing I_{REF1} = 2 A and I_{REF2} = 4 A according to *Table 25*, we get V_{SENSE1} = 1.647 V and V_{SENSE2} = 3.283 V, then:

M = 1.222 [S]

b = -0.013 [A]

I_{OUT} is then:

Equation 15

$$I_{OUT} = 1.222 \cdot V_{SENSE} - 0.013$$

An easy algorithm can give the M and b values. During the EOL the pairs (V_{SENSE1}, I_{REF1}) and (V_{SENSE2}, I_{REF2}) or alternatively only M and b can be stored in the microcontroller relevant EEPROM. After the calibration the current sense variation is still influenced by the device temperature. *Equation 15* is still affected by an error proportional to the sense current thermal drift.

This drift is reported in the datasheet as dK/K. The drift decreases when increasing the output current, e.g. in the VND7020AJ datasheet the drift is +/-25 % at 0.1 A and it decreases down to +/-5 % when the output current is 9 A.

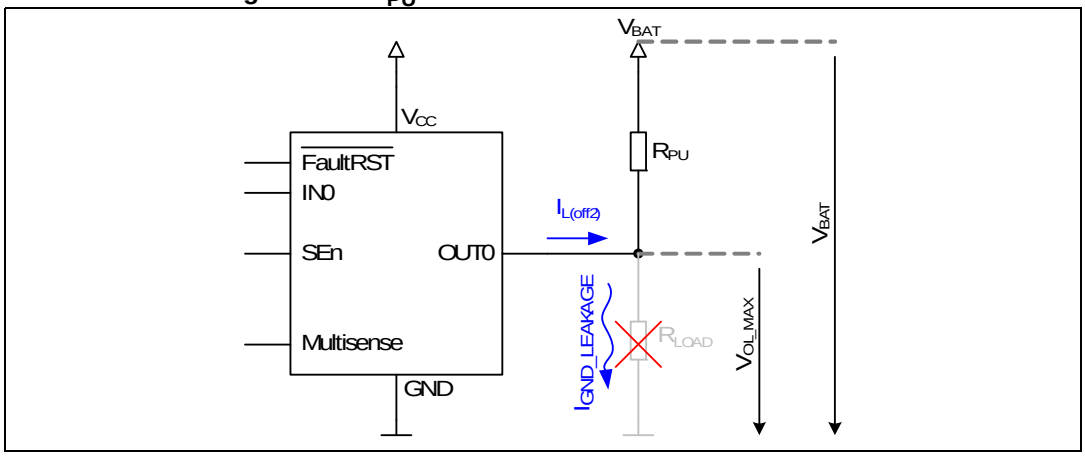
7.2.11 Open load detection in off-state

- Available if SE_n pin is set high
- Indicated by V_{SENSEH} on MultiSense pin
- External pull-up on the output needed
- Possibility to distinguish between open load in off-state and short to V_{BAT} using switchable pull-up resistor.

Maximum R_{PU} calculation during open-load condition:

Switchable resistor R_{PU} must be selected in order to ensure $V_{OUT} > V_{OL\_MAX}$ (value given in the datasheet) considering maximum leakage current for V_{OL_MAX}, as well as additional leakage current flowing to GND (i.e. due to humidity),

Figure 103. R_{PU} calculation with no load connected



Resistor R_{PU} connected to V_{BAT} supply results to:

$$R_{PU} < \frac{V_{BAT} - V_{OL\_MAX}}{I_{GND\_LEAKAGE} - I_{L(off2)\_MIN}}$$

Where $I_{L(off2)}$ is a value present in the datasheet.

Considering V_{BAT} = 7 V, ground leakage current $I_{GND\_LEAKAGE}$ = 0 and $I_{L(off2)}$ = -100 µA

$$R_{PU} < \frac{7V - 4V}{100\mu A} = 30k\Omega$$

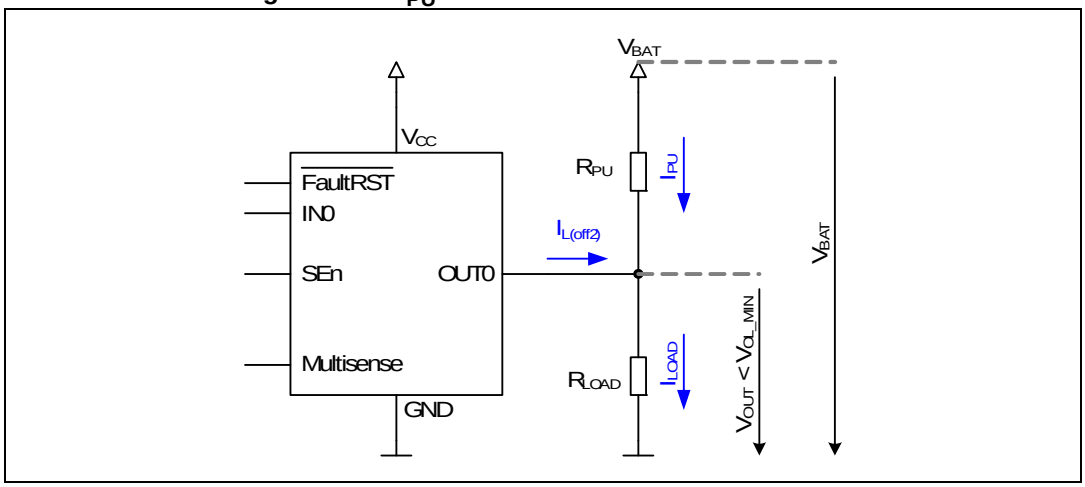
For V_{BAT} = 7 V, R_{PU} should be applied less than 30 kΩ to identify open load in off-state.

Minimum R_{PU} calculation while load is connected

In order to ensure that no OL in off state failure flag set, if the load is connected, minimum R_{PU} must be evaluated.

Minimum R_{PU} can be calculated as follows:

Figure 104. R_{PU} calculation with load connected



Considering:

$$I_{LOAD} = \frac{V_{OUT}}{R_{LOAD}} = I_{L(off2)} + I_{PU}$$

$$R_{PU} = \frac{V_{BAT} - V_{OUT}}{I_{PU}} \Rightarrow I_{PU} = \frac{V_{BAT} - V_{OUT}}{R_{PU}}$$

then:

$$\frac{V_{OUT}}{R_{LOAD}} = I_{L(off2)} + \frac{V_{BAT} - V_{OUT}}{R_{PU}}$$

with $V_{OUT} < V_{OL\_MIN}$

results to:

$$R_{PU} > \frac{R_{LOAD} \cdot (V_{BAT} - V_{OL\_MIN})}{V_{OL\_MIN} - R_{LOAD} \cdot I_{L(off2)\_MAX}} \qquad (I_{L(off2)\_MAX} \text{ is negative})$$

Example 6

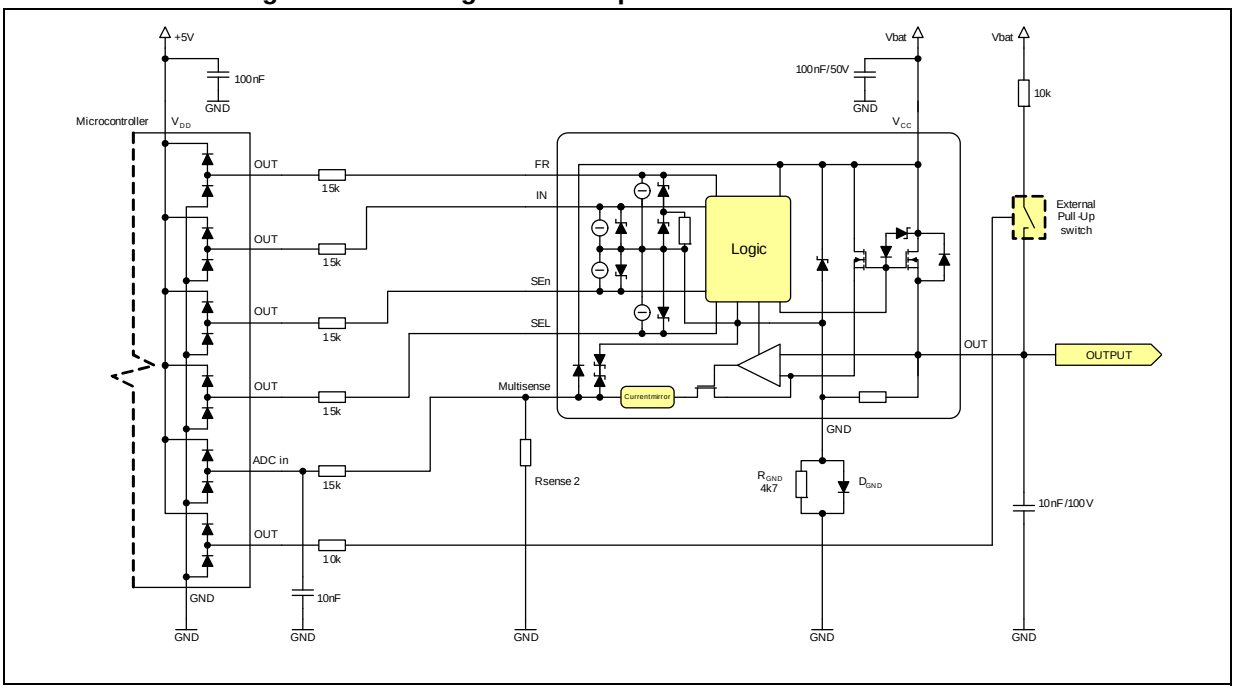
Let us consider a VND7020AJ driving a load with R_{LOAD} = 4 Ω and following parameters: V_{OL_min} = 2 V and V_{BAT} = 18 V (as worst case battery)

$I_{L(off2)\_MAX}$ = -15 µA

Applying below formula the pull-up resistance in order not to generate a false OL diagnostic is:

$$R_{PU} > \frac{4\Omega \cdot (18V - 2V)}{2V - 4\Omega \cdot (-15\mu A)} = 32\Omega$$

Figure 105. Analogue HSD – open load detection in off-state



In the following plots delay times for the OL detection in off state vs settings of INx and SE_n are shown. The relevant delay times t_{DSTKON} and t_{D_VOL} are given in the datasheets.

Figure 106. Open load / short to V_{CC} detection in OFF state - delay after IN is set from low to high

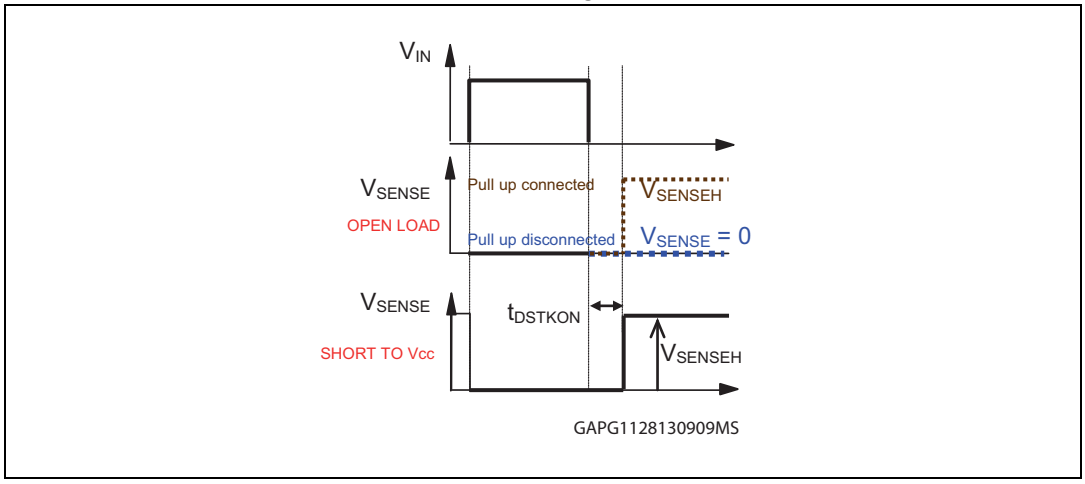


Figure 107. Open load/short to V_{CC} detection in OFF state - delay after SE_n is set from low to high

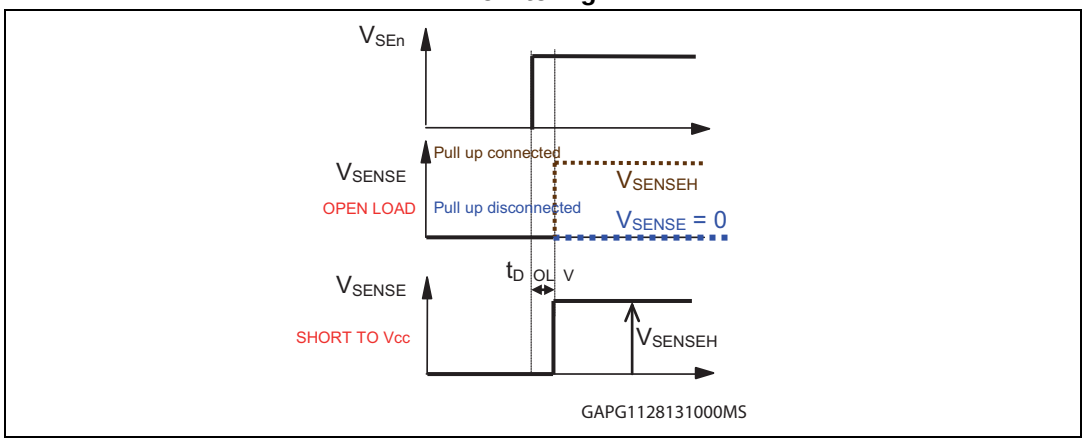


Table 26. MultiSense pin levels in off-state

Condition	Pull up	MultiSense	SE_n
Open load	Yes	0	L
		V_{SENSEH}	H
	No	0	L
		0	H
Short to V_{CC}	Yes	0	L
		V_{SENSEH}	H
	No	0	L
		V_{SENSEH}	H
Nominal	Yes	0	L
		0	H
	No	0	L
		0	H

Diagnostic summary

The table below summarizes all failure conditions, the V_{SENSE} signal behavior and recommendations for diagnostics sampling.

Table 27. Diagnostics - overview

Fault condition	Signal	Value	
Open load (without pull-up)	V_{IN}	L	H
	V_{SENSE}	0 V	0 V
	Notes		Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$).
	Waveforms sampling	See *Figure 108*	
Open load (with pull-up)	V_{IN}	L	H
	V_{SENSE}	V_{SENSEH}	0V
	Notes	Delay time from falling edge of IN pin must be considered (t_{DSTKON}).	Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$).
	Waveforms sampling	See *Figure 109*	
Short circuit to V_{BAT}	V_{IN}	L	H
	V_{SENSE}	V_{SENSEH}	< Nominal
	Notes	Delay time from falling edge of IN pin must be considered (t_{DSTKON}).	Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$).
	Waveforms sampling	See *Figure 110*	
Power limitation or over temperature (Autorestart mode)	V_{IN}	L	H
	FR	L	L
	V_{SENSE}	0 V	V_{SENSEH}
	Notes		Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$, trip time to PowerLimitation/Overtemperature shutdown whatever is longer).
	Waveforms sampling	See *Figure 111*	

Table 27. Diagnostics - overview (continued)

Fault condition	Signal	Value	
Power limitation or over temperature (Latch mode)	V_{IN}	L	H
	FR	H	H
	V_{SENSE}	0 V	V_{SENSEH}
	Notes		Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$, trip time to PowerLimitation/Overtemperature shutdown whatever is longer). Output latched-off after the first intervention of power limitation or thermal shutdown. Can be unlatched by a low level pulse on the FR pin ($_{TPULSE} > T_{LATCH\_RST}$).
	Waveforms sampling	See *Figure 112*	

Figure 108. Open-load without pull-up timings

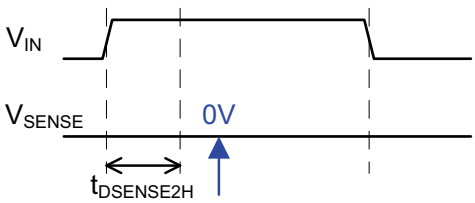


Figure 109. Open-load with pull-up timings

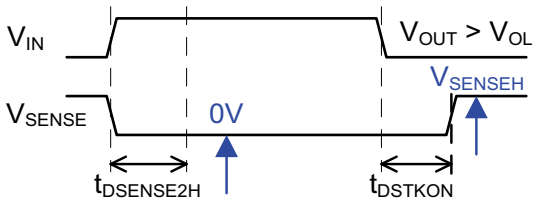


Figure 110. Short circuit to V_{BATT} timings

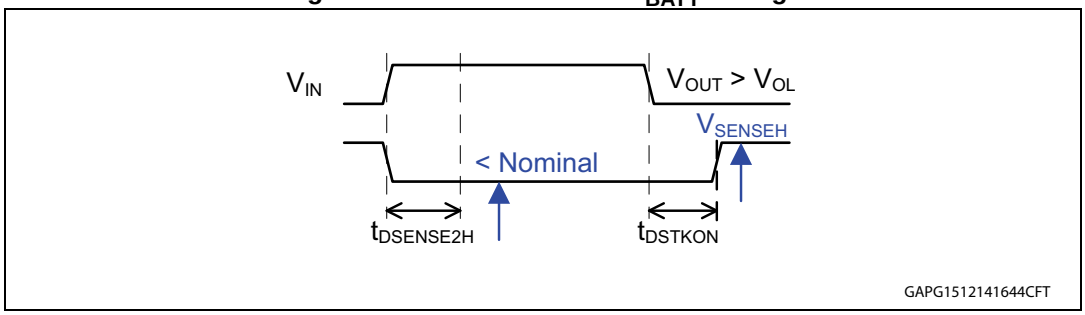


Figure 111. Power limitation or overtemperature waveforms (in autorestart mode)

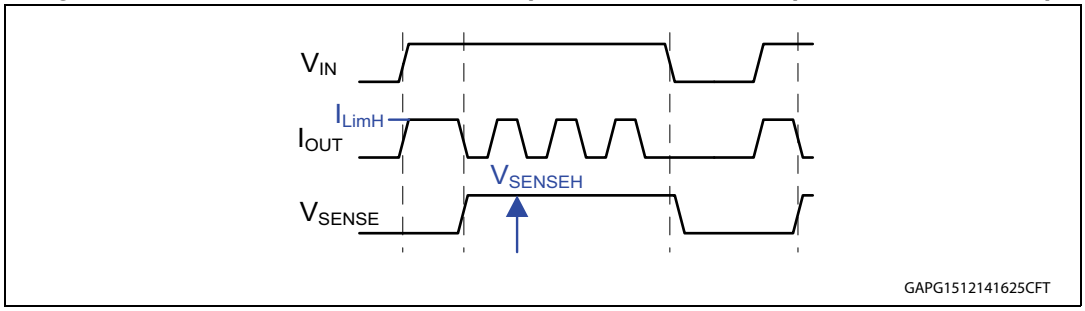
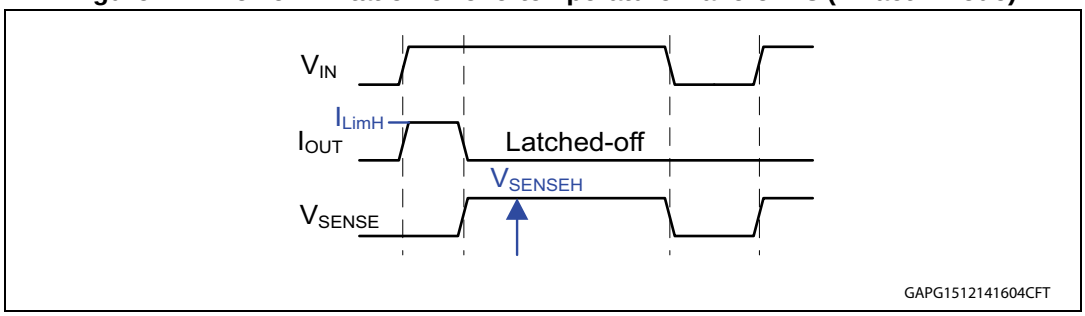


Figure 112. Power limitation or overtemperature waveforms (in lacth mode)



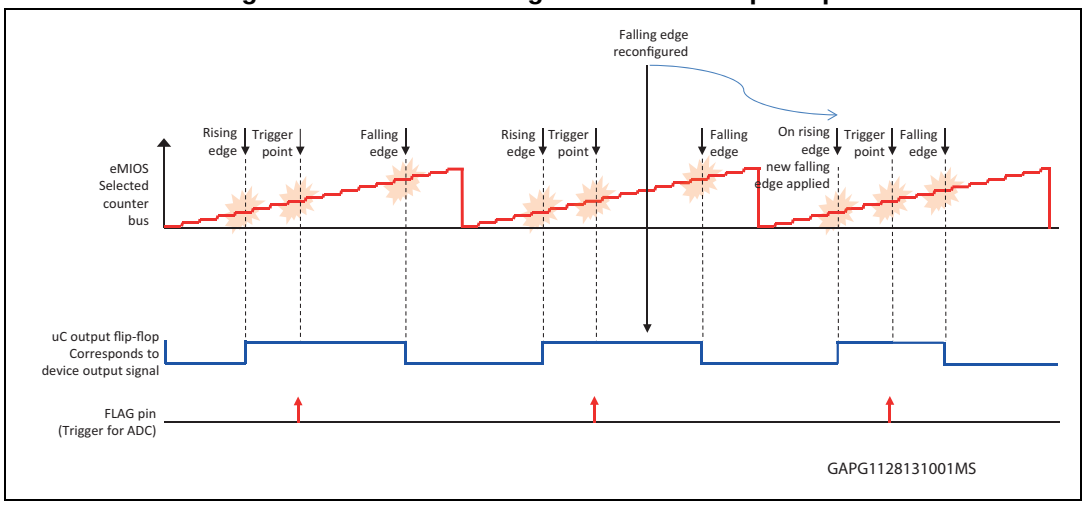
7.2.12 MultiSense diagnostic evaluation with SPC560Bxx

Considering analogue monitoring for several outputs, appropriate microcontroller must be used. Choosing SPC560Bxx, dedicated HW blocks can be used with advantage to monitor multiple C_{SENSE} signals (together with automated MultiSense channel switching).

SPC560Bxx is capable to generate independent PWM signals for multiple outputs by dedicated hardware block called eMIOS. It includes capability to specify trigger position within PWM period for signal A/D conversion without any SW intervention (0 % CPU load in software task used for MUX switching and A/D conversion triggering).

Figure 113 shows specific eMIOS mode, applicable for PWM generation and A/D conversion triggering (OPWMT mode)

Figure 113. eMIOS PWM generation mode principle



eMIOS block is able to control many channels applying independent configuration of rising, falling edge position (duty cycle), together with trigger, specifying sampling point for MultiSense signal. For example SPC560B64 - up to 2x31channels are available for this purpose (other models can contain different number of eMIOS channels). These channels can be mapped directly to control INx signals of multiple HSDs.

Additional block aligned with M0-7 devices MultiSense control, is ADC external Multiplexer. This peripheral use MA[2:0] control pins capable to control external analogue Multiplexer (in this case M07 devices are in role of external multiplexer). $SEL_{0...2}$, SE_n pins are controlled by MA[2...0] outputs.

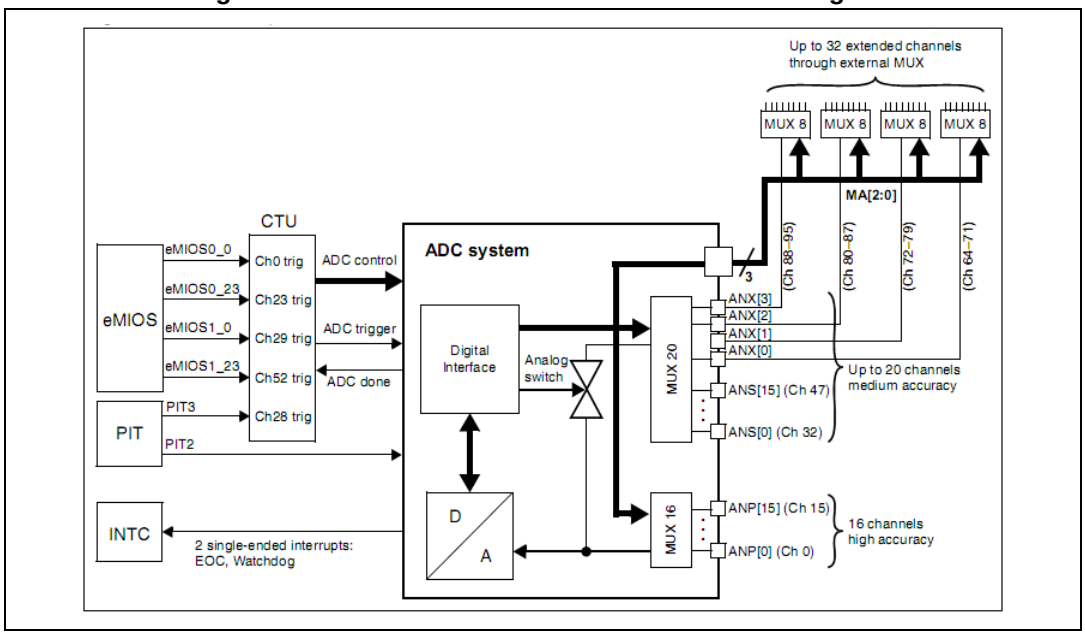
Four analogue input channels ANX[3:0] linked with MA[2...0] selector outputs create possibility to monitor 4(A/D inputs) x 8 (possible combination of MA[2...0]) = 32 analogue signals, driven by MA[2...0] outputs.

Depending on the system complexity, multiple devices can be diagnosed using extended ADC channels without need of SW control on the microcontroller side. eMIOS block create trigger measurement points, pass them to the ADC external multiplexer. It drives MA[2...0] outputs applied to M0-7 HSDs SELx pins (selecting relevant monitored channel). Selected MultiSense feedback passed to one of the A/D inputs is automatically measured by microcontroller A/D converter at preconfigured time. This operation applies to all channels using MA[2...0] (external multiplexer).

For simple/medium complex systems (up to 32 analogue monitored channels), analogue monitoring of all channels can be applied without impact on CPU load (using extended ADC attached to eMIOS channels in OPWMT mode).

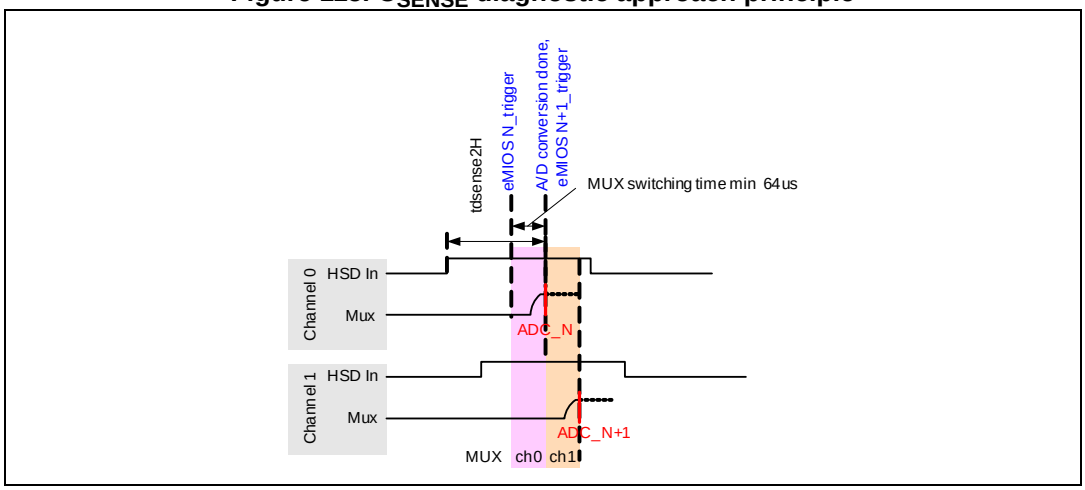
On more complex system (analogue monitoring more than 32 channels) additional logic must be involved.

Figure 114. SPC extended ADC channels block diagram



While ADC external MUX control is used on SPC, it is important to preconfigure maximum delay (64 µs) between MUX switching and A/D conversion. This delay covers time necessary to switch M0-7 internal Multiplexer to newly selected channel/signal together with time needed for signal stabilization caused by low-pass filter used on A/D input. Additionally must be ensured valid current sense signal during A/D conversion. It means there must be delay between HSD channel switch ON and ADC sampling, at least $t_{DSENSE2H}$ time. After ADC is sampled, MUX can be changed to following channel/signal. (Via MA [2...0])

Figure 115. C_{SENSE} diagnostic approach principle



Example configuration applying 0 % CPU load (MUX switching done by microcontroller HW peripherals)

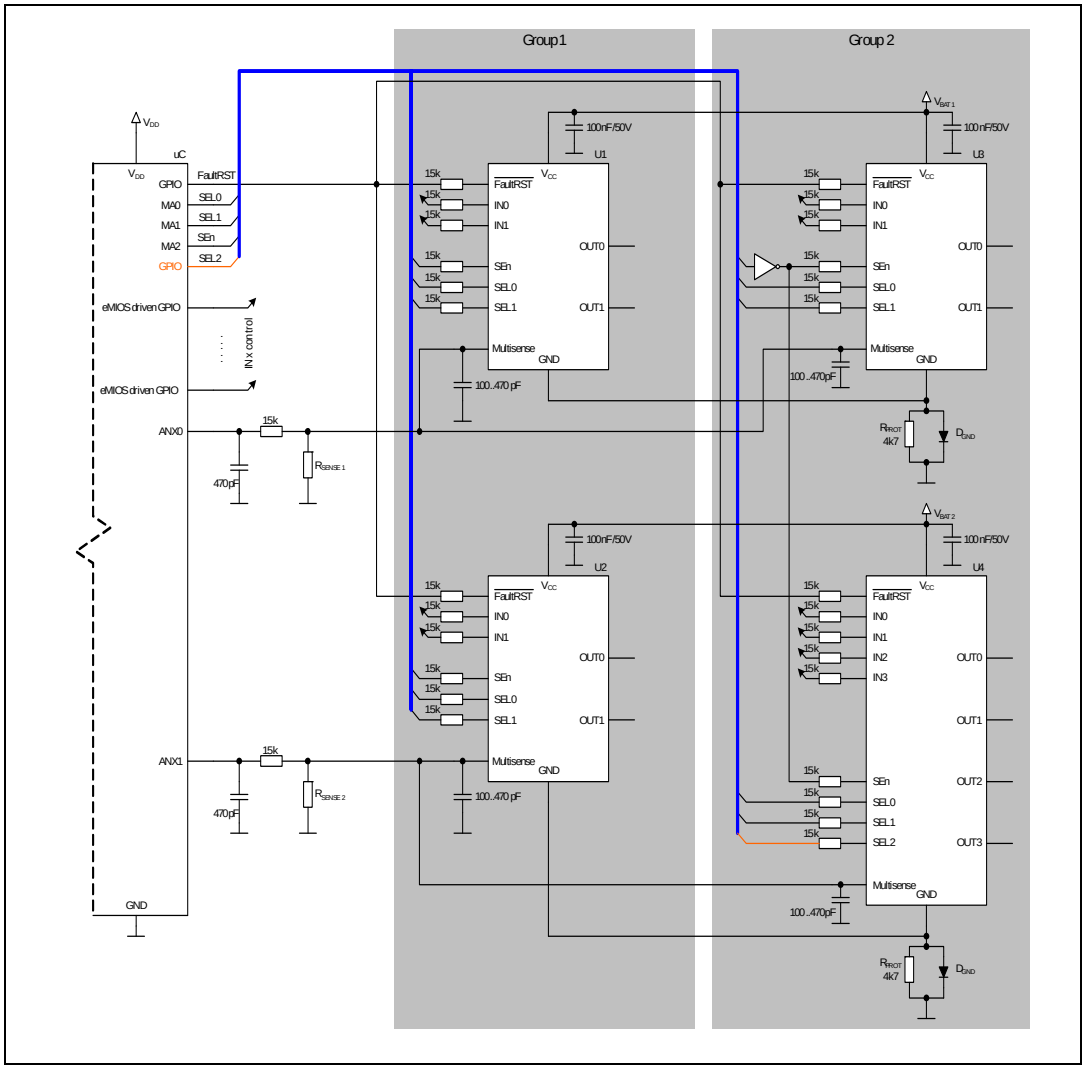
In the following example two groups of drivers are given. Each group consists of two devices (maximum can be 4 – given by microcontroller A/D peripheral - number of analogue input channels linked to external multiplexer ANX0...3, see *Figure 114*), where SEL pins are connected in parallel (selecting the same MUX channel on all devices). During diagnostic,

groups 1 and 2 are alternated by SE_n signal (every time, only one group is active for diagnostic, group 2 use inverter on SE_n signal).

SPC560Bxx diagnostic Interface is using externally multiplexed A/D channels ANX0 and ANX1 linked with control SE_n and SEL0...1 pins automatically without any microcontroller load.

Since quad channel device (U4) in Group 2 is used, SEL2 pin must be controlled by SW (no additional MA pin is available). In this example, SW controls alternation between current sense signals and V_{CC} + T_C signals on quad channel HSD (U4).

Figure 116. Example of connection of multiple HSDs to SPC using external ADC MUX control



In *Table 28*, the mapping between $SEL_{0...2}$, SE_n control signals and ANX0, ANX1 signals is shown:

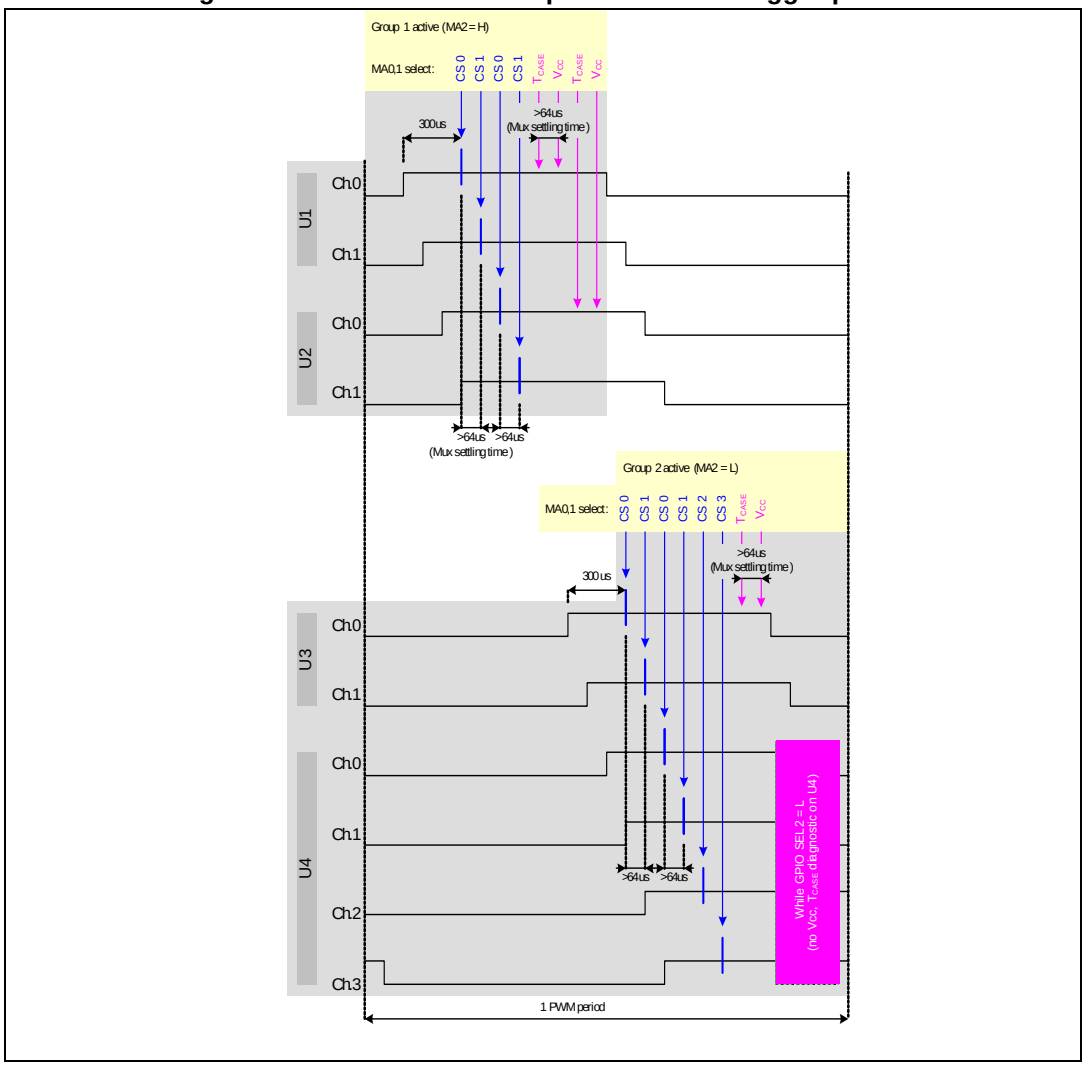
Table 28. SPC560Bxx example signals mapping

GPIO	MA1	MA0	MA2	Negative MA2	ANX0		ANX1		
(SEL_2)	(SEL_1)	(SEL_0)	SEn U1 + U2	SEn U3 + U4	(MultiSense)		(MultiSense)		
X	L	L	H	L	CurrentSense Ch0	MultiSense U1 VND7020AJ	CurrentSense Ch0	MultiSense U1 VND7020AJ	Group1
X	L	H	H	L	CurrentSense Ch1		CurrentSense Ch1		
X	H	L	H	L	T_{CHIP} Sense		T_{CHIP} Sense		
X	H	H	H	L	V_{CC} Sense		V_{CC} Sense		
L	L	L	L	H	CurrentSense Ch0	MultiSense U3 VND7020AJ	CurrentSense Ch0	MultiSense U4 VNQ7140AJ	Group2
L	L	H	L	H	CurrentSense Ch1		CurrentSense Ch1		
L	H	L	L	H	T_{CHIP} Sense		CurrentSense Ch2		
L	H	H	L	H	V_{CC} Sense		CurrentSense Ch3		
H	L	L	L	H	CurrentSense Ch0(1)	MultiSense U3 VND7020AJ	T_{CHIP} Sense		
H	L	H	L	H	CurrentSense Ch1		V_{CC} Sense		
H	H	L	L	H	T_{CHIP} Sense		T_{CHIP} Sense		
H	H	H	L	H	V_{CC} Sense		V_{CC} Sense		

1. SEL_2 not applicable - output according SEL_1, SEL_0 and SEn.

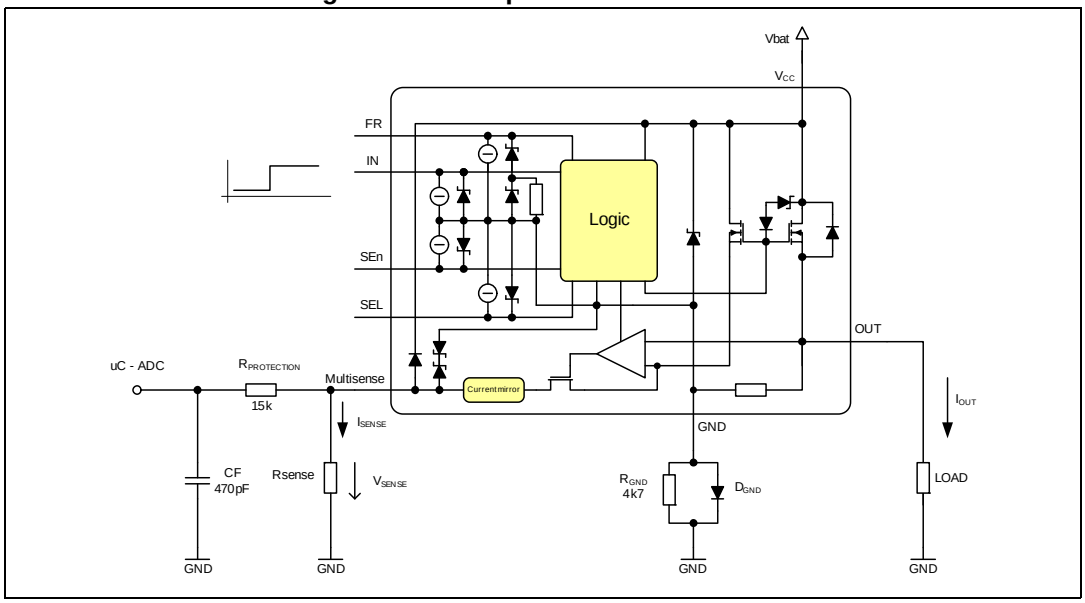
Time diagram shows A/D trigger points of MultiSense diagnostic:

Figure 117. SPC560Bxx example MultiSense trigger points



7.2.13 MultiSense low pass filtering

Figure 118. Low pass filter connection



The current sense voltage is usually connected through a 15 kΩ protection resistor to the ADC input of the microcontroller. In case of V_{SENSEH} level the voltage is limited by the microcontroller internal ESD protection (~5.6 V) while the ADC shows maximum value (0xFF in case of 8-bit resolution). The capacitor CF is used to improve the accuracy of the V_{SENSE} measurement (refer to *Figure 118*).

This capacitor acts as a low impedance voltage source for the ADC input during the sampling phase. Together with 15 kΩ serial resistor, it creates a low pass filter (with cutoff frequency of ~22 kHz) against potential HF noise on the MultiSense line (especially if a long wire is routed to the microcontroller). This capacitor should be connected close to the microcontroller.

Chosen value of filtering capacitor (470 pF) together with $R_{PROTECTION}$ = 15 kΩ results in a time constant lower than settling times between multiplexer selection (control of $SEL_{0...2}$ pins) so with a minimized delay between $SEL_{0...2}$ settings and sampling at the ADC.

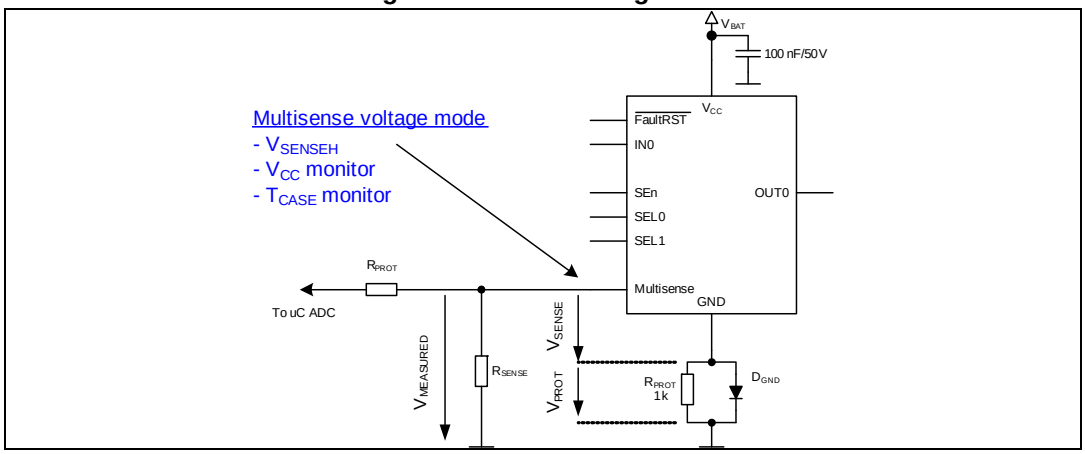
7.3 T_{CASE}, V_{CC} (device dependent)

Devices containing full logic implementation have the possibility to monitor device case temperature and battery voltage (please for knowing the list of devices containing or not the full logic, consult *Table 14*)

In this case, MultiSense output operates in voltage mode and output level is referred to device GND. For monolithic devices, where reverse battery protection circuitry is used on device GND pin, voltage offset is created relative to real GND potential. This offset must be considered during measurement on microcontroller side.

Following picture shows the link between $V_{MEASURED}$ and real V_{SENSE} signal.

Figure 119. GND voltage shift



7.3.1 V_{CC} monitor

Battery monitoring channel provides $V_{SENSE} = V_{CC} / 4$

Without calibration of voltage analogue feedback accuracy, limited precision of V_{CC} monitoring can be applied.

Considering limit values of VND7020AJ datasheet, and in case all channels are deactivated ($IN_x = 0$)

$$V_{SENSE\_VCC\_MIN} = 3.16 = \frac{13}{TRANSFER\_COEFFICIENT\_MAX}$$

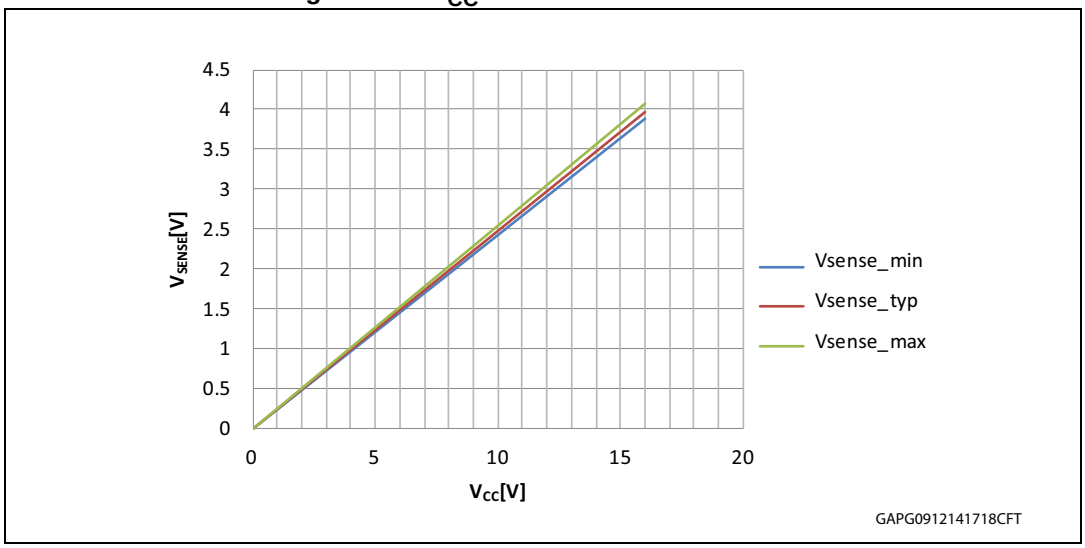
$$TRANSFER\_COEFFICIENT\_MAX = \frac{13}{3.09} = 4.114(+2.1\%)$$

and similar

$$V_{SENSE\_VCC\_MIN} = 3.30 = \frac{13}{TRANSFER\_COEFFICIENT\_MIX}$$

$$TRANSFER\_COEFFICIENT\_MIX = \frac{13}{3.30} = 3.939(-2.1\%)$$

Figure 120. V_{CC} monitor transfer function



Applying limit cases of transfer coefficients show possible inaccuracy of V_{CC} monitoring.

The precision of MultiSense V_{CC} monitor can be improved with a calibration, this means measuring an operating point of one device V_{SENSE_VCC}(for example calibration at 13 V and 25 °C) and by knowing the dependency of the V_{SENSE_VCC} with the device temperature to be able to read the V_{CC} value with maximum precision.

Experimental results show an average dV_{SENSE_VCC} / DT_{CHIP} ~ -70 µV/K and an average relative error (dV_{SENSE_VCC} / V_{SENSE_VCC}) / DT_{CHIP} ~ 4.5 (µV/V)/K in the range -40 °C to 85 °C.

Moreover the MultiSense signal in V_{CC} mode depends on the state of the channels; experimental results show an increase for each channel turned on of about 8 mV.

7.3.2 Case temperature monitor

Case temperature monitor is capable of providing information about actual device temperature. Since diodes are used for temperature sensing, the following equation describes the link between temperature and output V_{SENSE} level:

$$V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T_0) + \frac{dV_{SENSE\_TC}}{dT} \cdot (T - T_0)$$

where dV_{SENSE_TC} / dT is the temperature coefficient. Typical V_{SENSE_TC} at 25 °C and 13 V and with all channels off with R_{SENSE} = 1 kΩ is 2.06 V. The temperature coefficient is dV_{SENSE_TC} / dT ~ -5.5 mV/°C. The total spread of V_{SENSE_TC} at a given temperature (between -40 °C and 150 °C) is constant and equal to ±85 mV. This corresponds to a precision in temperature reading of about +/- 16 °C without calibration.

The precision of MultiSense T_{CHIP} monitor can be improved with a calibration, this means measuring an operating point of one device V_{SENSE_TC} (for example calibration at 1 V and 25 °C) and by knowing the dependency of the V_{SENSE_VCC} with the battery voltage to read the T_{CHIP} value during the real operation.

Experimental results show an average dV_{SENSE_TC} / dV_{CC} ~ -0.4 mV/V, this means dT_C / dV_{CC} ~ + 0.1 °C/V in the range from 7 V to 18 V.

Moreover the MultiSense signal in V_{CC} mode depends on the state of the channels; experimental results show an increase for each channel turned on of ~ 10 mV, this means a positive offset of about 1.8 °C.

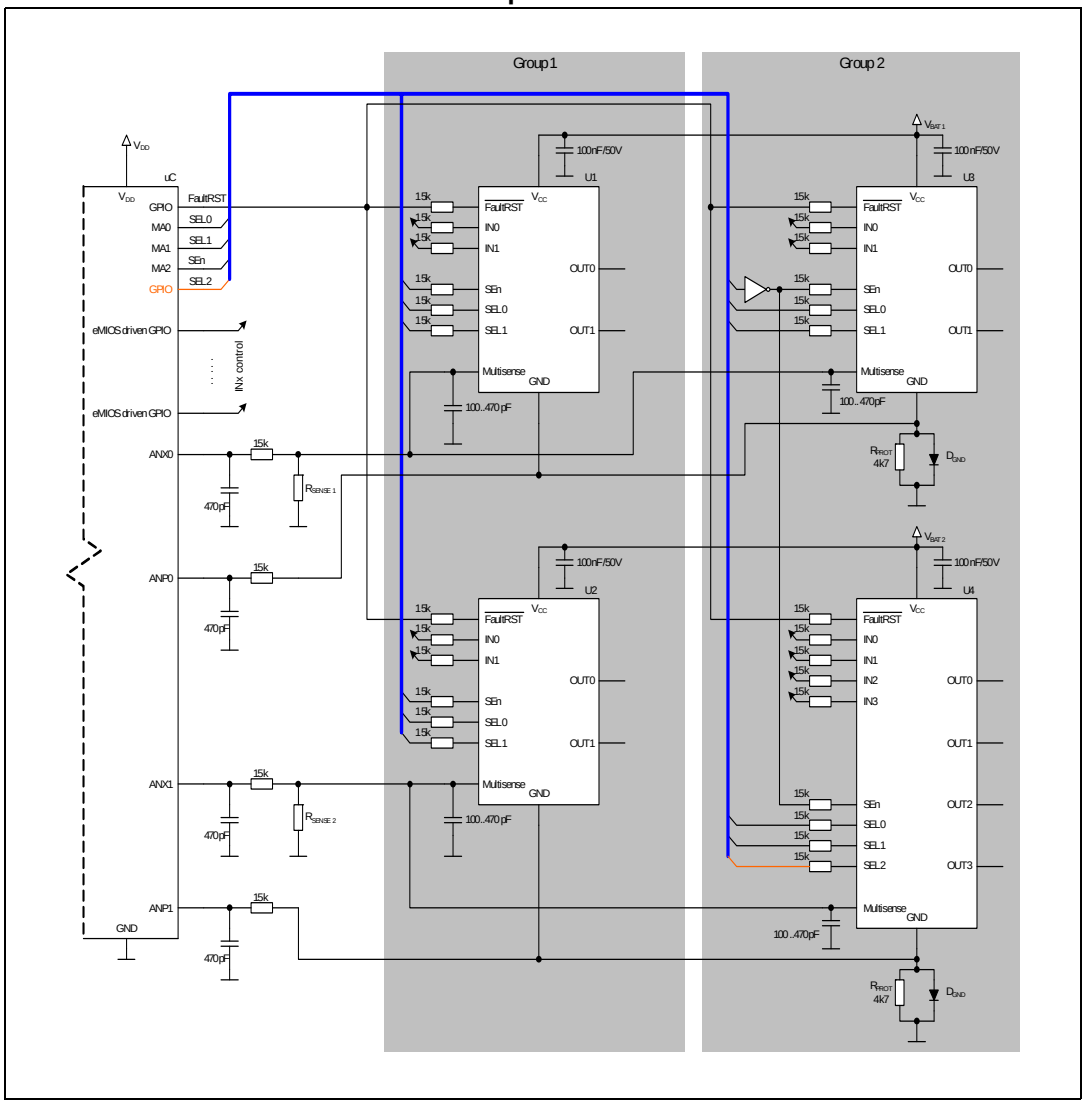
7.3.3 Example on evaluation of V_{CC}, T_{CASE} and diagnostic with SPC560Bxx

Similar concept shown in the example for Current Sense monitoring can be applied. The major difference is consideration of GND offset on monolithic devices. Since voltage drop on GND protection depends on varying operating conditions, device ground voltage should be monitored for accurate MultiSense result.

The measurement setup is similar to previous evaluation extended with 2 additional AD channels for GND shift monitoring (two reverse battery protection groups). These AD channels are HW triggered with dedicated eMIOS channels.

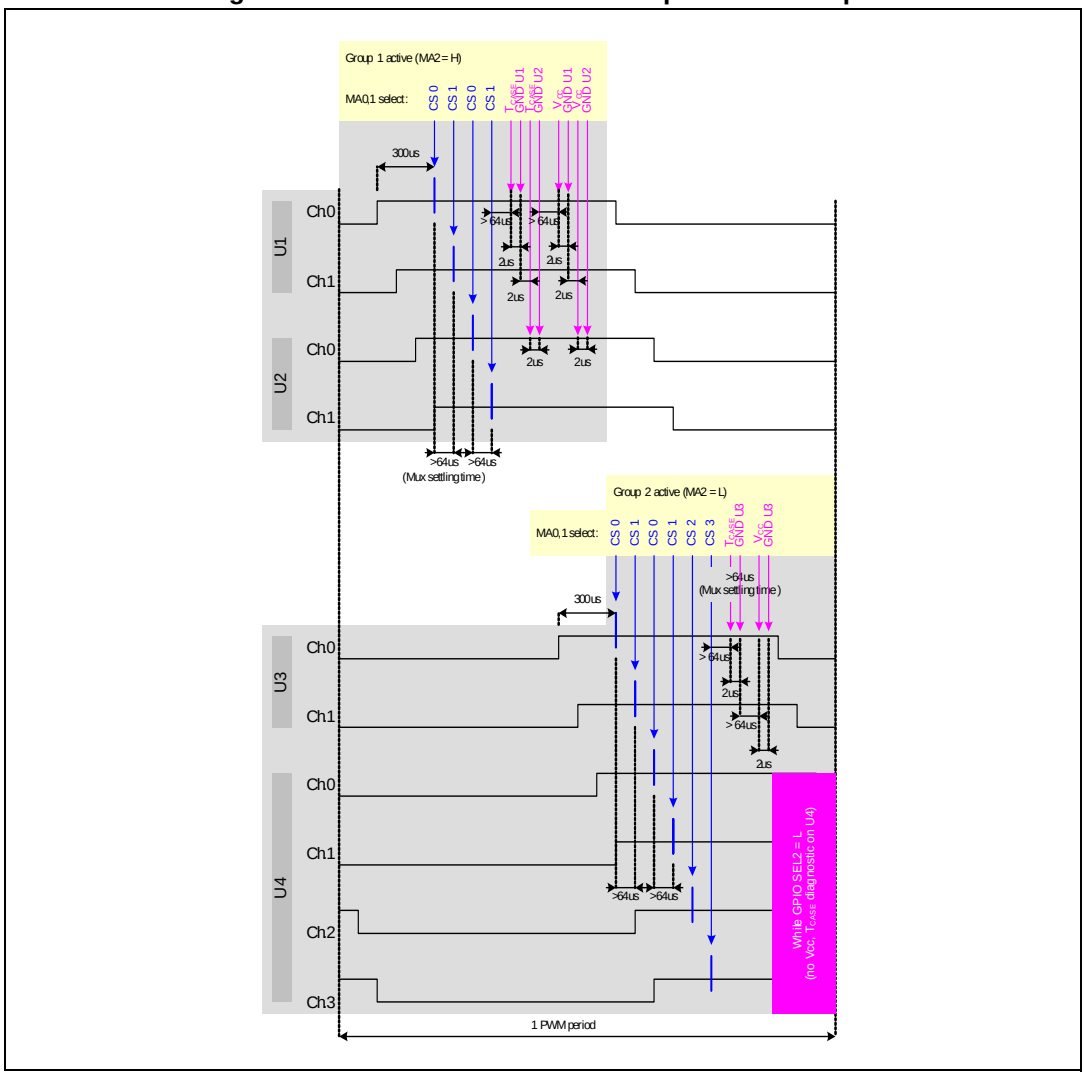
Analogue signals mapping is the same as shown in *Table 28*.

Figure 121. Example MultiSense reading on multiple HSDs with GND shift compensation



To eliminate the effect of the GND shift variation, it is important to measure the GND voltage and V_{CC} / Temp signal in the same time (ideally) or with a few µs delay. Possible solutions are shown in the *Figure 122*.

Figure 122. GND shift measurement position example



The best trigger position for the V_{CC}/Temp and the GND voltage measurement is usually after the rising edge of channel with highest phase shift, when all PWM channels are already activated. At that point the GND signal is stable (note that this statement is not valid during power limitation or thermal shutdown).

8 Paralleling of devices

8.1 Paralleling of logic input pins

The following chapters describe the paralleling of Logic input pins (SE_n, INx, SELx, LEDx and FaultRST) of different HSDs, taking into account device technology (monolithic HSDs or hybrid HSDs) and supply line configuration (either the same or separate supply lines for each HSD).

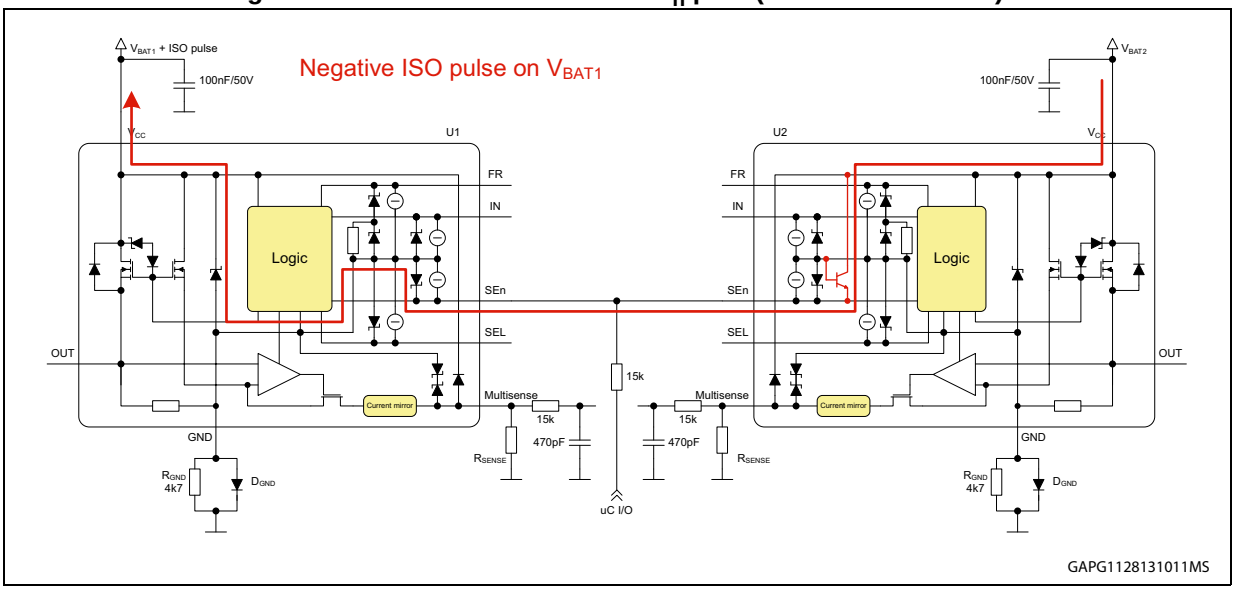
Direct paralleling of logic pins is generally an allowed operation in case of devices designed in the same technology (monolithic or hybrid) supplied from one supply line. In all other cases (like combination of monolithic with hybrid technology, different supply lines) we should use additional components to ensure a safe operation under conditions in automotive environment (ISO pulses, reverse battery …).

The clamp structure of all logic input is similar (except for a slight difference on FaultRST pin), therefore all the explanations related to the paralleling of SE_n pins are applicable also to paralleling of other logic input pins (including the FaultRST pin).

8.1.1 Monolithic HSDs supplied from different supply lines

Paralleling of SE_n pins of monolithic HSDs is possible, however some precautions in schematic should be applied if the HSDs are supplied from different supply lines. In this case the direct connection of SE_n pins (as shown in *Figure 123*) is not safe.

Figure 123. Direct connection of SE_n pins (not recommended)



Direct connection of SE_n pins is not safe in following cases:

- Negative voltage surge either on V_{BAT1} or V_{BAT2}
- Positive voltage surge either on V_{BAT1} or V_{BAT2} while:
  - Device GND pin disconnected;
  - D_{GND} not used (resistor protection only);
  - Positive pulse energy higher than HSD (or D_{GND}) capability - all paralleled devices could be damaged

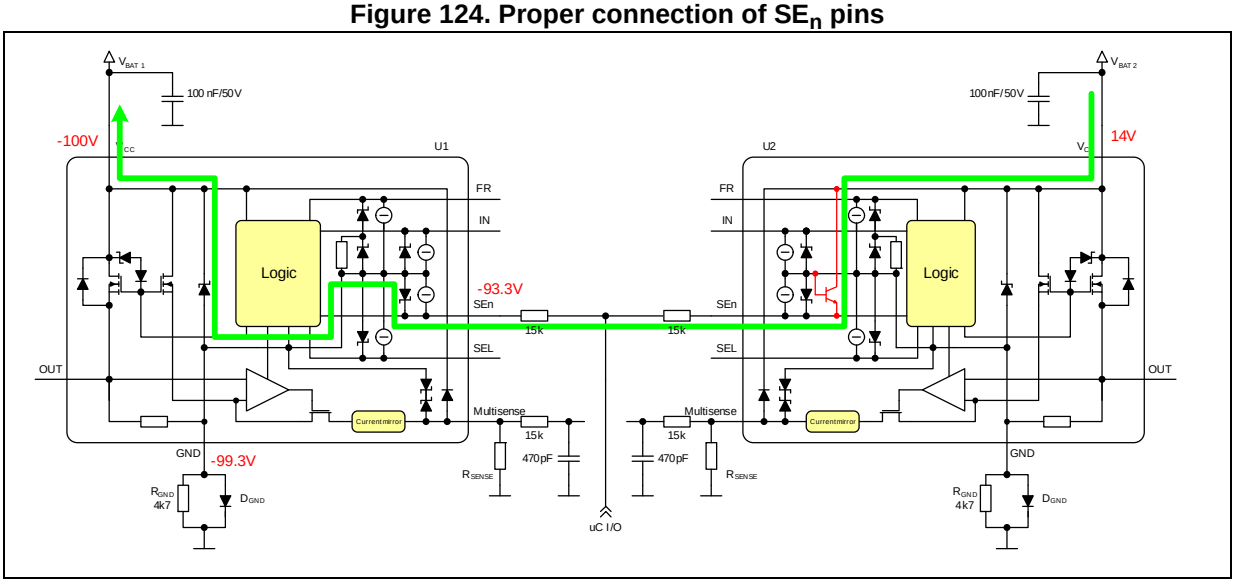
A negative voltage surge (ISO7637-2 pulse 1, 3a) either on V_{BAT1} or V_{BAT2} could cause unlimited current flow between both supply lines via the SE_n pins of connected devices. This current could lead to malfunction or even failure of one or both of the HSDs. The mechanism (current path) is shown graphically on example on *Figure 123*. The negative transient (i.e. -100 V) on V_{BAT1} (device U1) is transferred to the GND pin via the V_{CC} - GND clamp (~0.7 V voltage drop → -99.3 V) and consequently to the SE_n pin via the SE_n - GND clamp (~6.3 V voltage drop → -93 V). Since the SE_n pin of second device U2 is pulled negative, a parasitic NPN bipolar structure on SE_n pin is activated (emitter pulled negative versus base) and pulls the SE_n pin high towards the V_{CC} pin (V_{BAT2}). Since this parasitic NPN structure doesn't allow the SE_n pin to be pulled negative to -93 V, an unlimited current can flow between the devices.

A positive voltage surge (ISO7637-2 pulse 2a, 3b) either on V_{BAT1} or V_{BAT2} could lead to the increase of the GND pin voltage (in case of missing D_{GND}, D_{GND} failure or GND pin disconnected). As soon as this occurs, the voltage on SE_n pin is rising also since a parasitic NPN bipolar structure is activated (base positive versus emitter). Since the second device (with properly connected GND pin) doesn't allow the voltage on SE_n pin to rise above the clamp voltage (~6.3 V) an unlimited current can flow between the devices. This could lead to malfunction or even failure of one or both of the HSDs.

In order to avoid such failures it is recommended to add a 15 K resistor in series to each SE_n pin (see *Figure 124*).

In principle the same applies to all other logic input pins as well (since the clamp structure is similar).

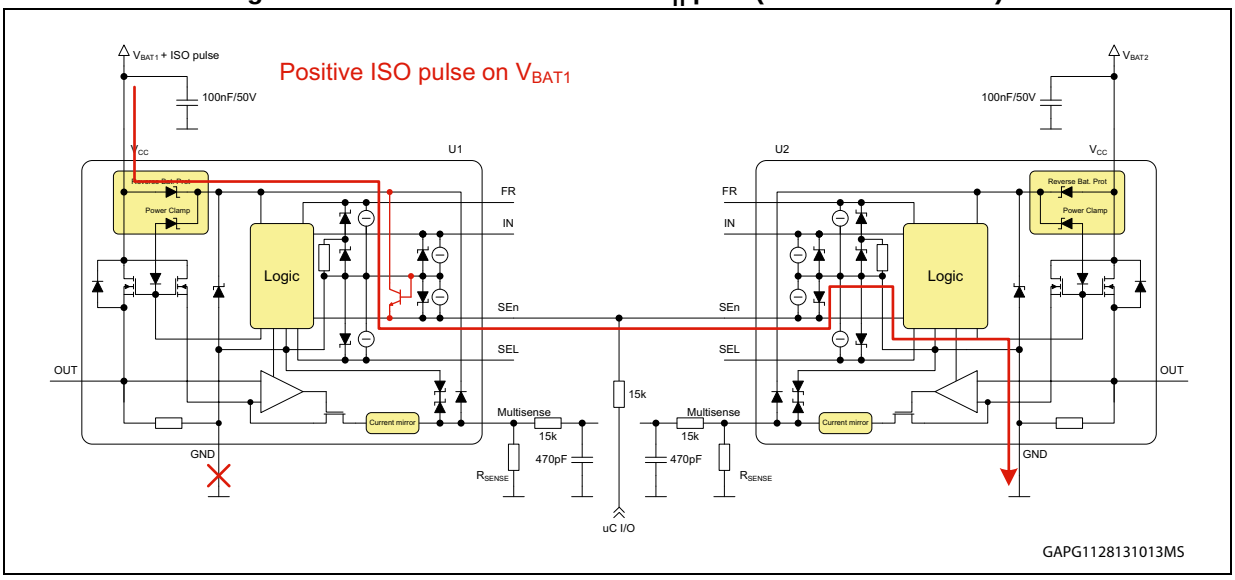
Figure 124. Proper connection of SE_n pins



8.1.2 Hybrid HSDs supplied from different supply lines

Paralleling of SE_n pins of hybrid HSDs is possible; however some precautions in schematic should be applied if the HSDs are supplied from different supply lines. Direct connection of SE_n pins (as shown in *Figure 125*) is not safe.

Figure 125. Direct connection of SE_n pins (not recommended)



Direct connection of SE_n pins is not safe in the following cases:

- Loss of GND connection

If the GND connection of one device is lost, positive as well as negative ISO pulses on the associated supply line are not clamped anymore (considering no other devices connected to this supply line). If the transient voltage is big enough to activate a parasitic NPN bipolar structure of one SE_n pin and the clamp structure of second SE_n pin, there could be unlimited current flow between both supply lines through SE_n pins (same mechanism as already described in case of monolithic devices). This current could lead to malfunction or even failure of one or both of the HSDs. The parasitic current path is shown graphically on *Figure 125*.

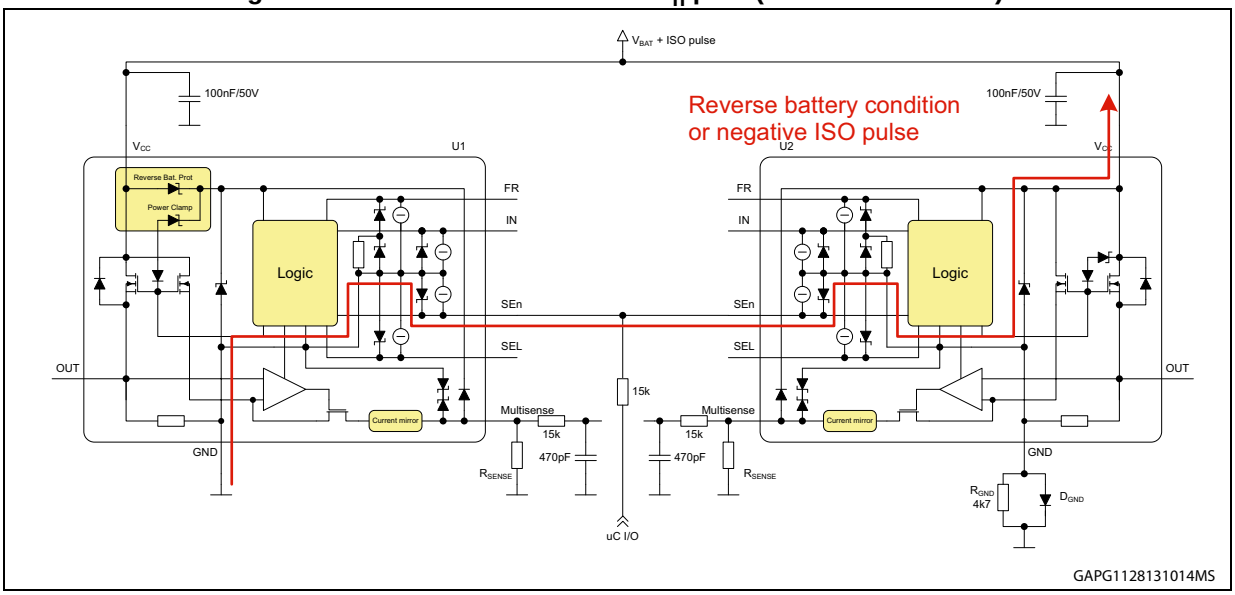
In order to avoid such failures it is recommended to add a 15 KΩ resistor in series to each SE_n pin (in the same way as already described in case of monolithic devices – see previous chapter).

In principle the same applies to all other logic input pins as well (since the clamp structure is similar).

8.1.3 Mix of monolithic and hybrid HSDs

Paralleling of SE_n pins of monolithic and hybrid HSD is possible, however some precautions in schematic must be applied. The direct connection of SE_n Pins (as shown in *Figure 126*) is not safe (even if we consider the same power supply for both devices).

Figure 126. Direct connection of SE_n pins (not recommended)

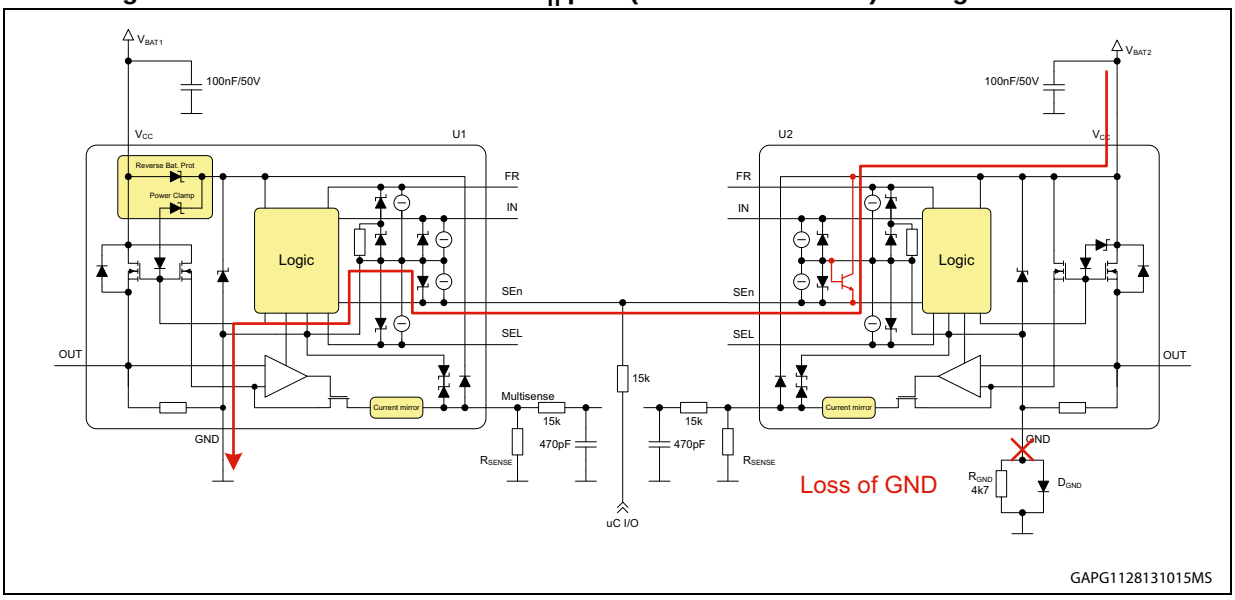


Direct connection of SE_n pins is not safe in the following cases:

- Reverse battery (single supply line considered)
- Negative ISO pulse (single supply line considered)
- Loss of GND connection (separate supply lines considered) + ISO pulse

Due to the different concepts of reverse battery protection of hybrid and monolithic devices, there is a way for unlimited current flow between both devices in case of reverse battery condition. The hybrid device has an integrated reverse battery protection in V_{CC} line, while the monolithic device needs an external diode/resistor in series with GND pin (refer to *Chapter 2: Reverse battery protection* of this document). The different potential on each GND pin (hybrid: ~ 0 V, monolithic: $-V_{BAT}$ - 0.7 V) is leading to the activation of both SE_n clamp structures when V_{BAT} is below ~ -7.5 V ($V_{SEnCLAMP}$ + two diode voltage drop). The resulting current can lead to malfunction or even failure of one or both of the HSDs.

Figure 127. Direct connection of SE_n pins (not recommended) during loss of GND



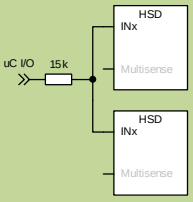
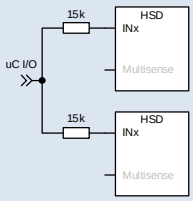
In configuration of separate supply lines where the GND connection of one device is lost, positive as well as negative ISO pulses on the associated supply line are not clamped anymore (considering no other devices connected to this supply line). If the transient voltage is big enough to activate involved structures, there could be unlimited current flow between both supply lines through SE_n pins. This current could lead to malfunction or even failure of one or both of the HSDs.

In order to avoid such failure it is recommended to add a 15 KΩ resistor in series to each SE_n pin (in the same way as already described in case of paralleling of monolithic devices – see previous chapter).

In principle the same applies to all other logic input pins as well (since the clamp structure is similar).

The following table is summarizing possible combinations of HSDs with paralleled inputs relative to the used power supply networks.

Figure 128. Paralleling of inputs summary

Texchnology	The same power supply network (VBAT + GND network)	Different supply networks (different VBAT or different GND protection network)
Monolithic + Monolithic	Single resistor on uC side, HSD inputs in parallel 	Each HSD use separate protection resistor 
Hybrid + Hybrid		
Monolithic + Hybrid		

8.2 Paralleling of MultiSense

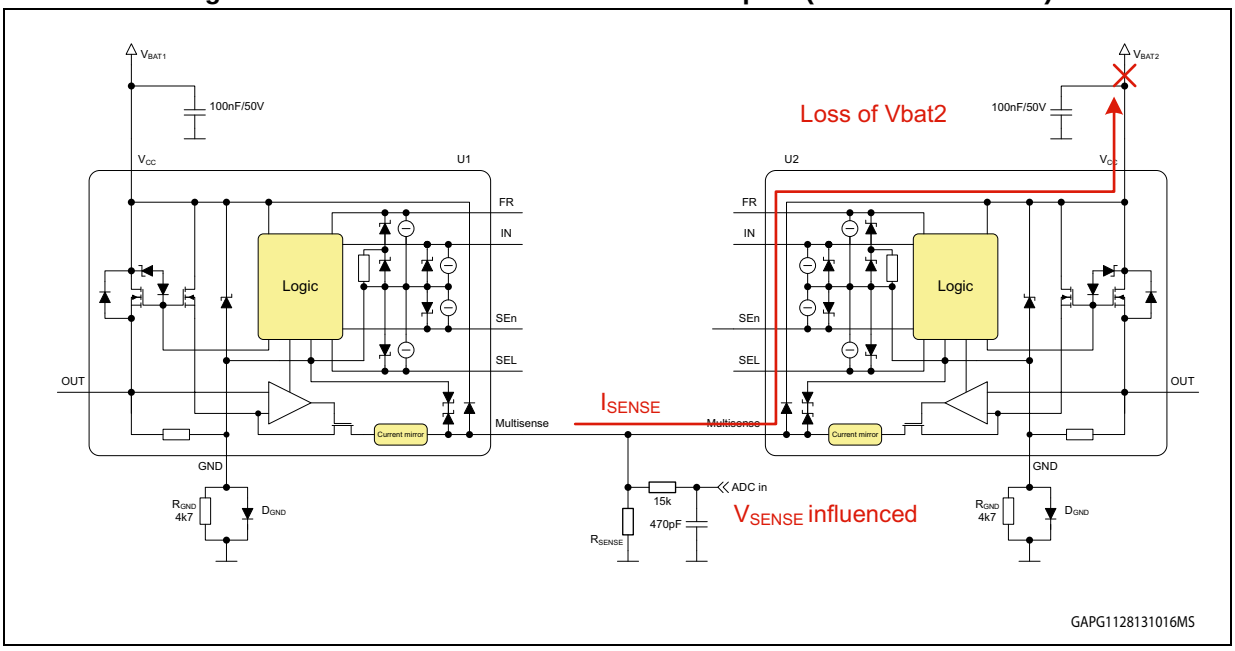
The following chapters describe the paralleling of MultiSense pins of HSDs, taking into account device technology (monolithic HSDs or hybrid HSDs) and supply line configuration (either the same or separate supply line for each HSD).

Direct connection of MultiSense pins is an allowed operation without any restriction when the devices are supplied from one supply line, sharing the same GND network. In case of separated supply lines or separated GND protection networks, we should use additional components to ensure a safe operation under conditions in automotive environment (ISO pulses, reverse battery …).

8.2.1 Monolithic HSDs supplied from different supply lines

Paralleling of MultiSense pins of monolithic HSDs is possible; however some precautions in schematic should be applied if the HSDs are supplied from different supply lines. Direct connection of MultiSense pins (as shown in the next picture) is not safe.

Figure 129. Direct connection of MultiSense pins (not recommended)



Direct connection of MultiSense pins is not safe in the following cases:

- Negative voltage surge on either on V_{BAT1} or V_{BAT2}
- Positive voltage surge either on V_{BAT1} or V_{BAT2} while:
  - Device GND pin disconnected
  - D_{GND} not used (resistor protection only)
  - Positive pulse energy higher than the HSD (or D_{GND}) capability - all paralleled devices could be damaged
- Loss of V_{BAT1} or V_{BAT2}

A negative voltage surge (ISO 7637-2 pulse 1, 3a) either on V_{BAT1} or V_{BAT2} is directly coupled to the MultiSense pin through the internal V_{CC} - MultiSense clamp structure. If the negative voltage on MultiSense line is big enough to activate the V_{CC} - MultiSense clamp

structure, there could be an unlimited current flow through both MultiSense pins. This current could lead to malfunction or even failure of one or both of the HSDs.

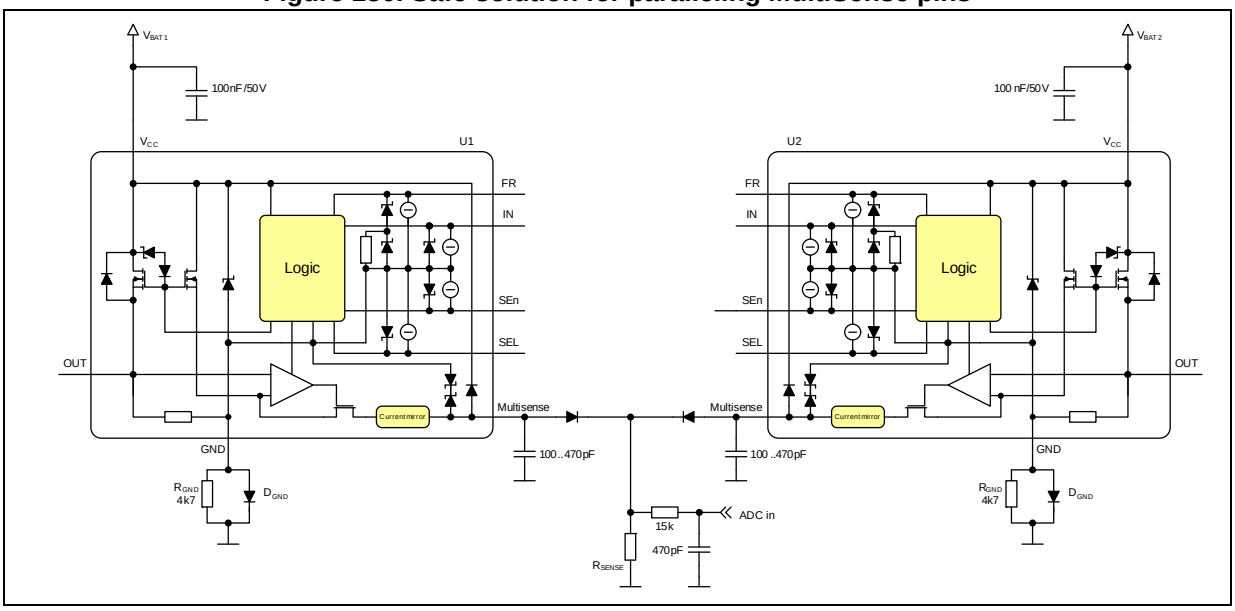
A positive voltage surge (ISO7637-2 pulse 2a, 3b) either on V_{BAT1} or V_{BAT2} together with missing D_{GND} (D_{GND} not used, D_{GND} failure or GND pin disconnected) can activate the V_{CC} - MultiSense clamp structure (clamp voltage similar to V_{CC} - GND clamp). As soon as this occurs there could be an unlimited current flow through both MultiSense pins. This current could lead to malfunction or even failure of one or both of the HSDs.

Loss of either V_{BAT1} or V_{BAT2} is leading to a wrong current sense signal. If V_{BAT2} is lost, U2 (and other components connected to V_{BAT2}) is supplied by U1 current sense signal through the internal V_{CC} - MultiSense clamp structure. Therefore the voltage on MultiSense bus will drop to almost 0V and we'll have no valid V_{SENSE} reading anymore.

In order to protect the devices during ISO pulses and to ensure valid current sense signal as well, we can add a diode in series to each MultiSense pin (as shown in the following schematics). In order to suppress the rectification of noise injected to the sense line, it is recommended to add a ceramic filter capacitor between each CS pin and ground.

However, the voltage drop on diodes in series with MultiSense pin can have an influence on the dynamic range of current sense, temperature and current sense accuracy. There must be also taken in account voltage drop over protection diode while MultiSense output is switched in voltage mode (V_{BAT}/Temperature signal output or V_{SENSEH} fault flag).

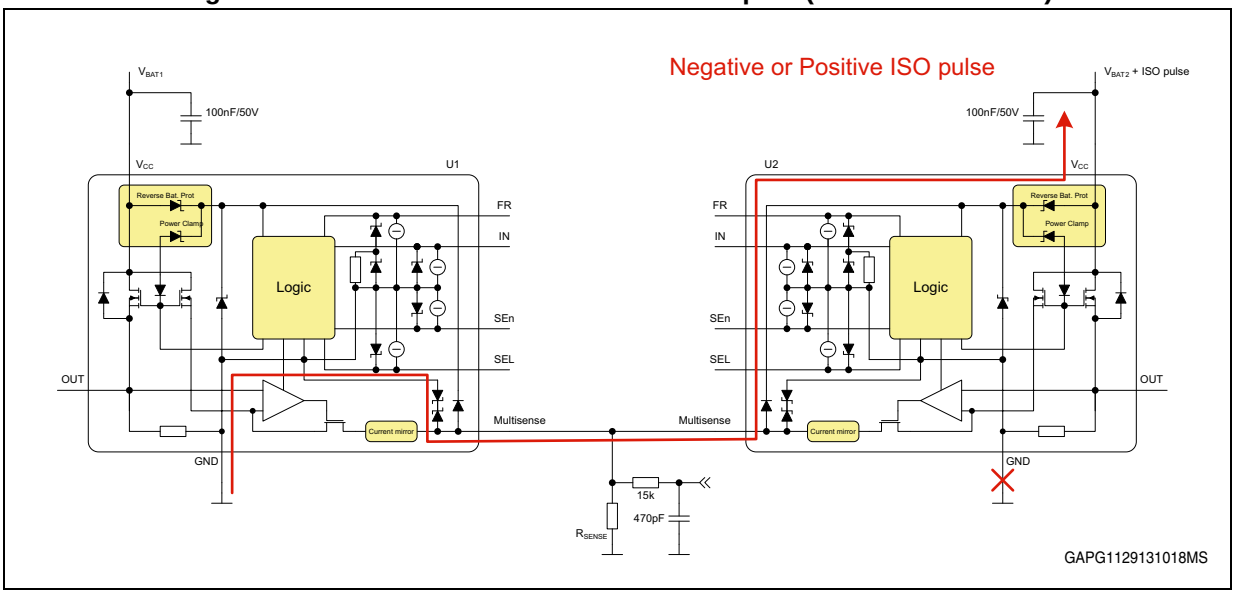
Figure 130. Safe solution for paralleling MultiSense pins



8.2.2 Hybrid HSDs supplied from different supply lines

Paralleling of MultiSense pins of hybrid HSDs is possible; however some precautions in schematic should be applied if the HSDs are supplied from different supply lines. Direct connection of MultiSense pins (as shown in the next picture) is not safe.

Figure 131. Direct connection of MultiSense pins (not recommended)



Direct connection of MultiSense pins is not safe in the following case:

– Loss of GND connection

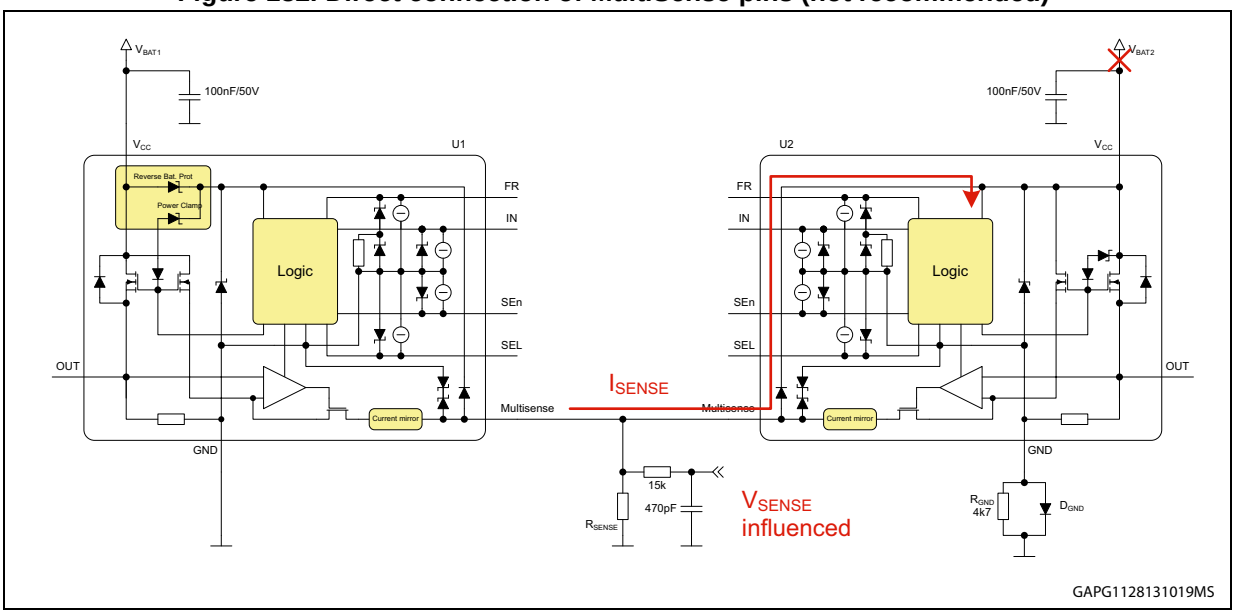
If the GND connection of one device is lost, positive as well as negative ISO pulses on the associated supply line are not clamped anymore (considering no other devices connected on this supply line). If the transient voltage is big enough to activate involved clamp structures, there could be an unlimited current flow between both supply lines through the MultiSense pins. This current could lead to malfunction or even failure of one or both of the HSDs. The mechanism (current path) is graphically explained on *Figure 131*. The ISO transient is applied on supply line of device U2. In case of negative ISO pulse, the current flows via negative clamp of internal reverse battery protection and MultiSense structure of device U2 (~17 V drop) and MultiSense-GND clamp of device U1 (-15 V clamp). In case of positive ISO pulse, the current flows via V_{CC} - MultiSense clamp of device U2 (50 V clamp) and MultiSense-GND clamp of device U1 (7 V clamp).

In order to ensure a valid current sense signal and to protect devices in all previously described cases, we can add a diode in series to each MultiSense pin (in the same way as already described in case of monolithic devices–see previous chapter).

8.2.3 Mix of monolithic and hybrid HSDs supplied from different supply lines

Paralleling of MultiSense pins of monolithic and hybrid HSDs is possible, however some precautions in schematic should be applied if the HSDs are supplied from different supply lines. Direct connection of MultiSense pins (as shown in the next picture) is not safe.

Figure 132. Direct connection of MultiSense pins (not recommended)



Direct connection of MultiSense pins is not safe in the following cases:

- Negative ISO pulse on V_{BAT2}
- Loss of V_{BAT1} or V_{BAT2}
- Loss of GND connection

A negative voltage surge (ISO7637-2 pulse 1, 3a) on V_{BAT2} is directly coupled to the MultiSense pin through the internal V_{CC} - MultiSense clamp structure. If the negative voltage on MultiSense line is big enough to activate the MultiSense - GND clamp structure, there could be an unlimited current flow through both MultiSense pins. This current could lead to malfunction or even failure of one or both of the HSDs.

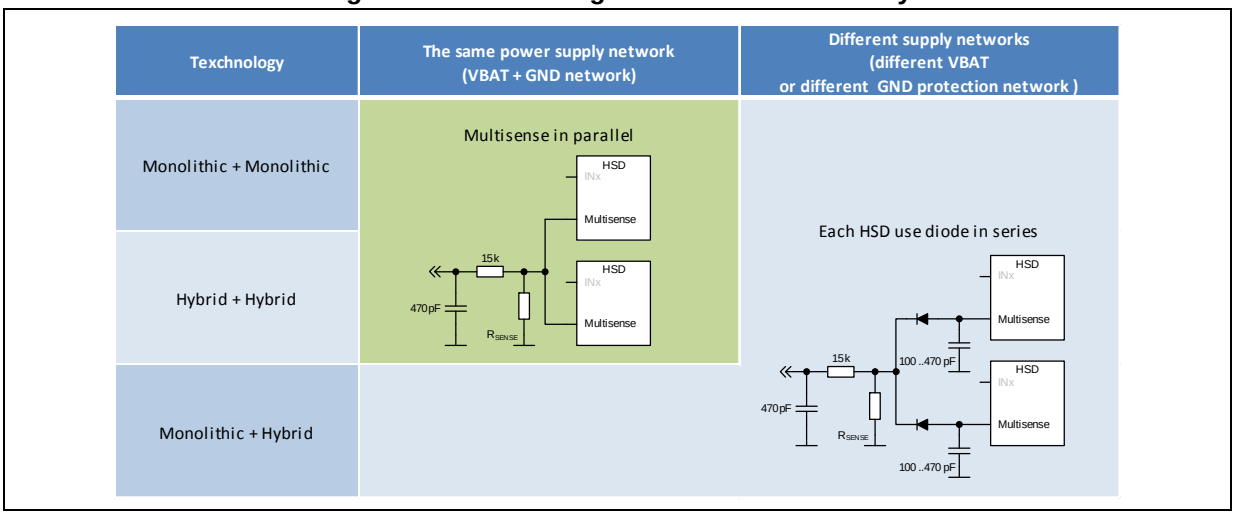
Loss of either V_{BAT1} or V_{BAT2} is leading to wrong current sense signal. If V_{BAT2} is lost, U2 logic part is supplied by U1 current sense signal through the internal V_{CC} - MultiSense clamp structure. Therefore the voltage on MultiSense bus will drop and we'll have no accurate V_{SENSE} reading anymore.

If the GND connection of one device is lost (D_{GND} not used, D_{GND} failure or GND pin disconnected), positive as well as negative ISO pulses on the associated supply line are not clamped anymore (considering no other devices connected to this supply line). If the transient voltage is big enough to activate the involved clamp structures, there could be an unlimited current flow between both supply lines through the MultiSense pins. This current could lead to malfunction or even failure of one or both of the HSDs.

In order to ensure a valid current sense signal and to protect devices in all previously described cases, we can add a diode in series to each MultiSense pin (in the same way as already described in case of monolithic devices–see previous chapter).

The following table is summarizing possible combinations of HSDs with paralleled MultiSense outputs relative to the used power supply networks.

Figure 133. Paralleling of MultiSense summary



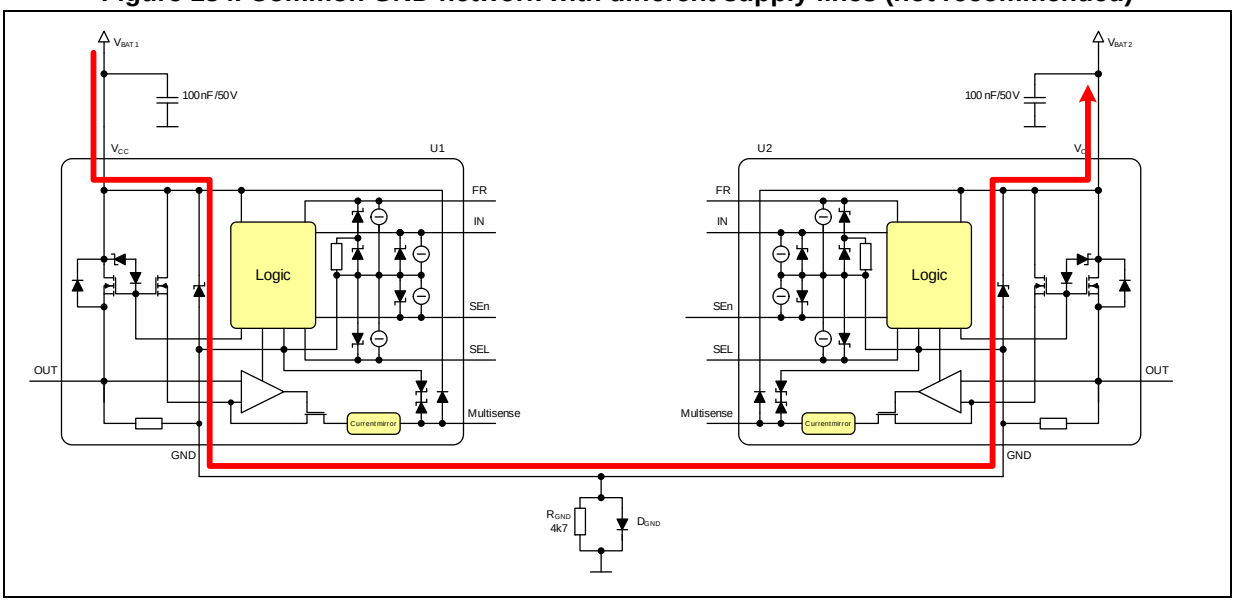
8.3 Paralleling of GND protection network

Sharing common ground protection network of monolithic HSDs is safe in case of using the same power supply line. If different supply lines are required, an external clamp must be present on both supply lines to clamp the negative transients to a voltage lower than the minimum V_{CLAMP}, so that $V_{BAT} + |V_{NEG\_PEAK}| < 40$ V. During the negative voltage exposure, the outputs of all paralleled devices linked to stable battery line turns-on (since the logic input thresholds are exceeded by pulling the GND pins negative).

Applying different supply lines (without an external clamp protection) is not safe in case of:

- Negative ISO pulse on V_{BAT1} or V_{BAT2}

Figure 134. Common GND network with different supply lines (not recommended)



8.4 Paralleling of outputs

Paralleling of outputs (within one device) is usually considered when higher current capability is needed. In this section is showed the device behavior with paralleled outputs and highlight potential issues (especially in combination with inductive loads). Considerations and conclusions concerning this chapter are based on experimental measurements on a limited sample size for each indicated part number.

8.4.1 Current balancing with resistive load

Following experimental measurements show the current sharing between the channel and behavior of current sense with different load current. Two M0-7 devices (one high and one low ohmic) are considered.

- V_{BAT}: 14 V
- Temperature: 25 °C
- Device
  - VND7020AJ (OUT0 + OUT1 paralleled)
  - VND7140AJ (OUT0 + OUT1 paralleled)
- To be checked:
  - Sharing of load current & current sense
  - Behavior at low current (V_{ON} regulation)

Figure 135. Test setup – paralleling of outputs (load current sharing)

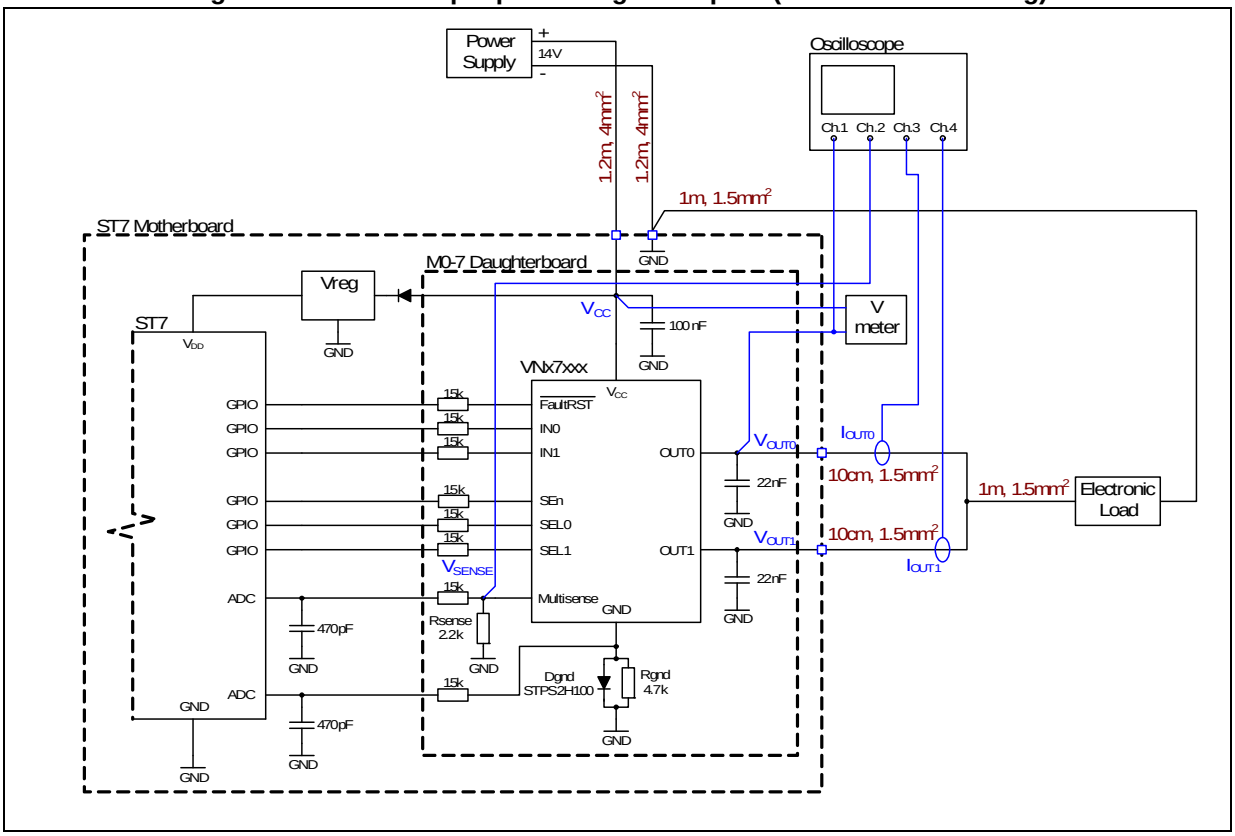


Figure 136. Sharing of load current, V_{ON} regulation (VND7020AJ)

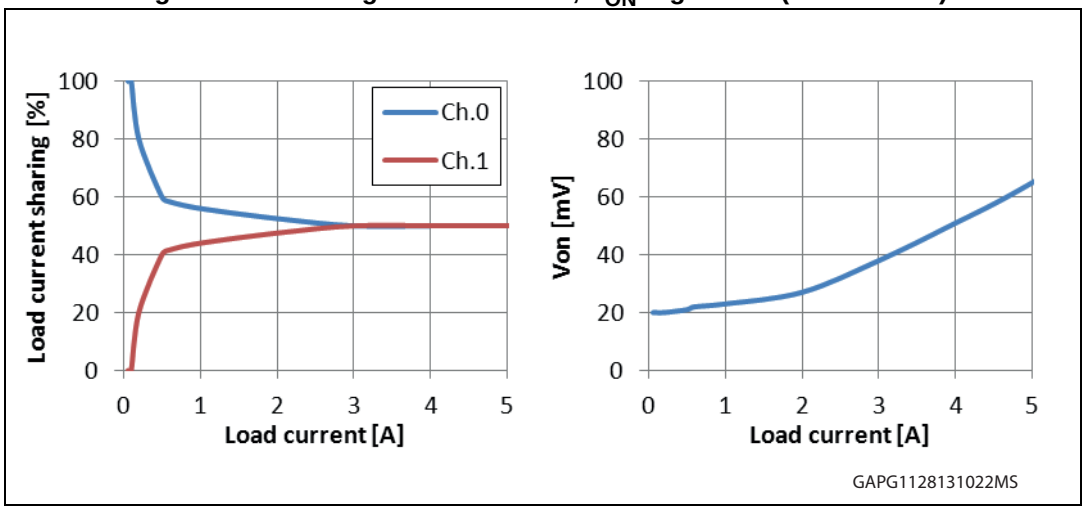


Figure 137. Current sense behavior at low current (VND7020AJ)

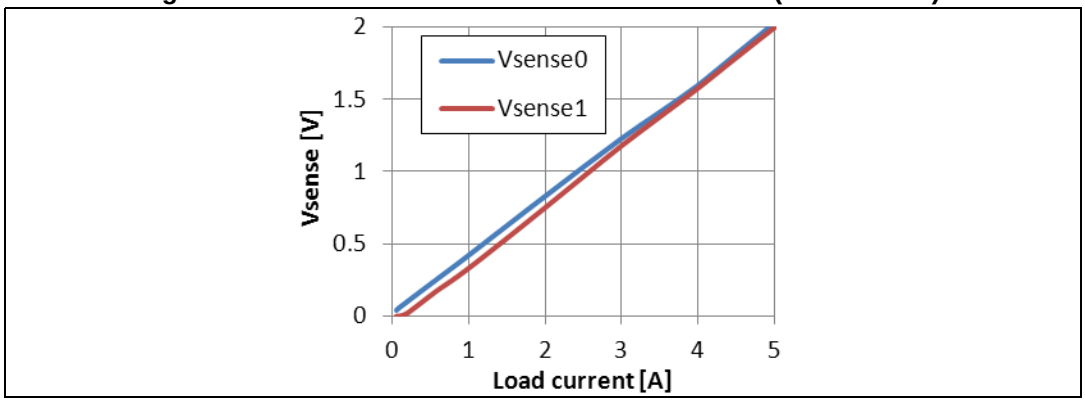


Figure 138. Sharing of load current, V_{ON} regulation (VND7140AJ)

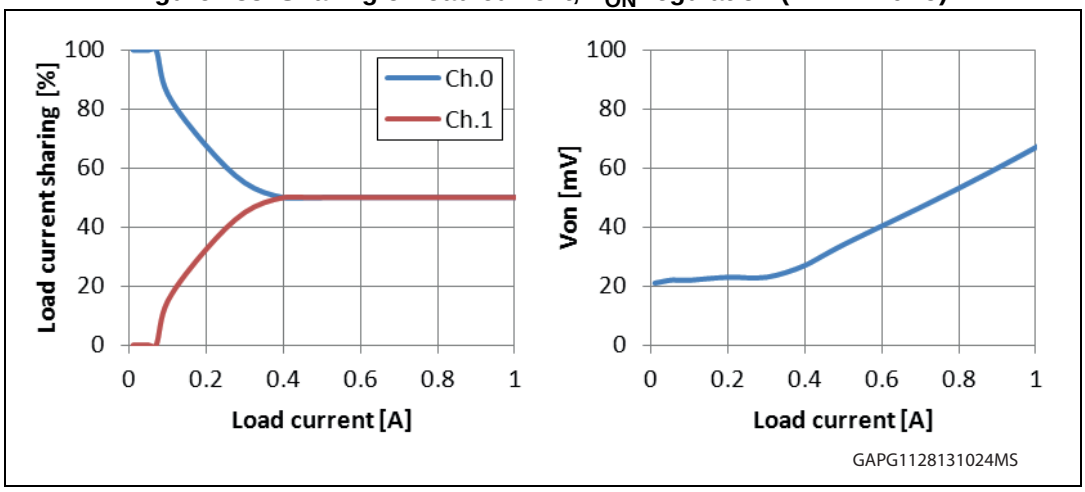
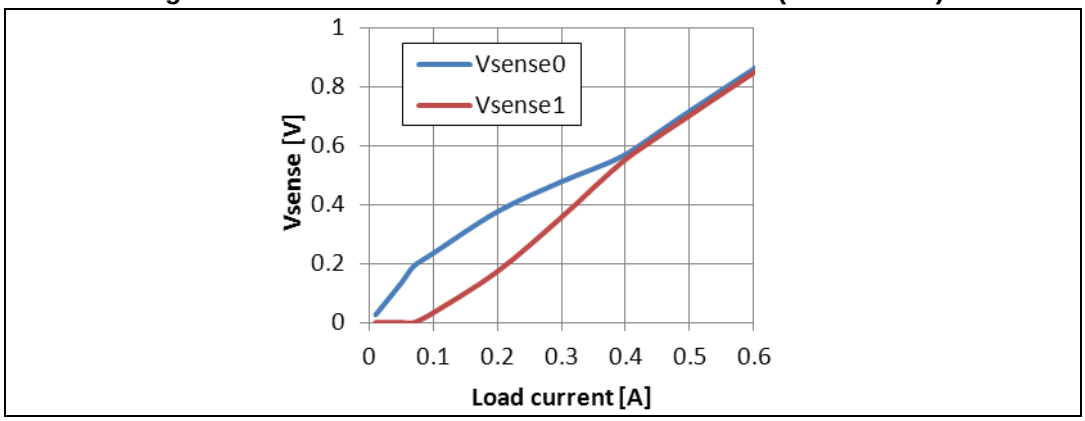


Figure 139. Current sense behavior at low current (VND7140AJ)



Conclusion:

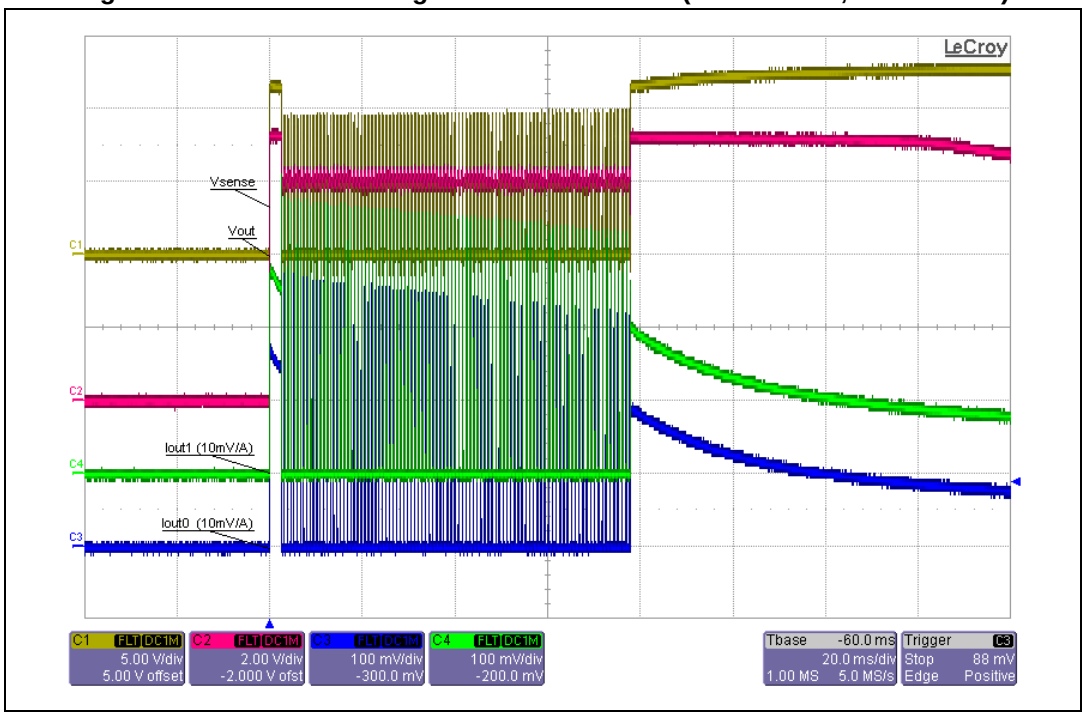
The current balancing is very good at high current levels, when the Drain Source voltage is above 30 mV (approximately half of the nominal output current). Reducing the load current increases the current unbalance (up to 100 % at very low current levels) since the outputs operates in voltage regulation mode (20 mV typically). The current sense values well correspond to actual output currents. This leads to the requirement for reading of both current sense values at low current levels (only the sum of these values will ensure correct diagnostic).

8.4.2 Overload behavior with resistive loads

This experiment shows the behavior during the overload conditions on a VND7040AJ sample with paralleled outputs (same test setup as for the load current sharing test).

- V_{BAT}: 14 V
- Temperature: 25 °C
- Device
  - VND7040AJ (OUT0 + OUT1 paralleled)
- To be checked:
  - Behavior during overload condition (cold bulb startup)

Figure 140. Behavior during overload condition (VND7040AJ, Ch.0 + Ch.1)



Conclusion:

After turn-on of both channels in overload condition, both channels are in current limitation and contribute equally to the total load current. The current regulation is stable on both channels. The first intervention of power limitation (turn-off) comes almost synchronously on both channels. However, the next power limitation or thermal shutdown cycling is asynchronous. The cycling frequency is the same but the phase shift is varying.

8.4.3 Driving inductive loads

The following part checks the load current sharing during the demagnetization phase at various load conditions (standard load with long wire harness, high inductance load with or without external freewheeling on VND7040AJ device with paralleled outputs).

- V_{BAT}: 14 V
- Temperature: 25 °C
- Device & Load
  - VND7040AJ (OUT0 + OUT1 paralleled)
    Bulb + 10 µH wire harness
    2 mH / 2.8 Ω (with or without external freewheeling)
- To be checked:
  - Demagnetization phase-sharing of load current & current sense
  - With or without external freewheeling

Figure 141. Test setup–paralleling of outputs (inductive loads)

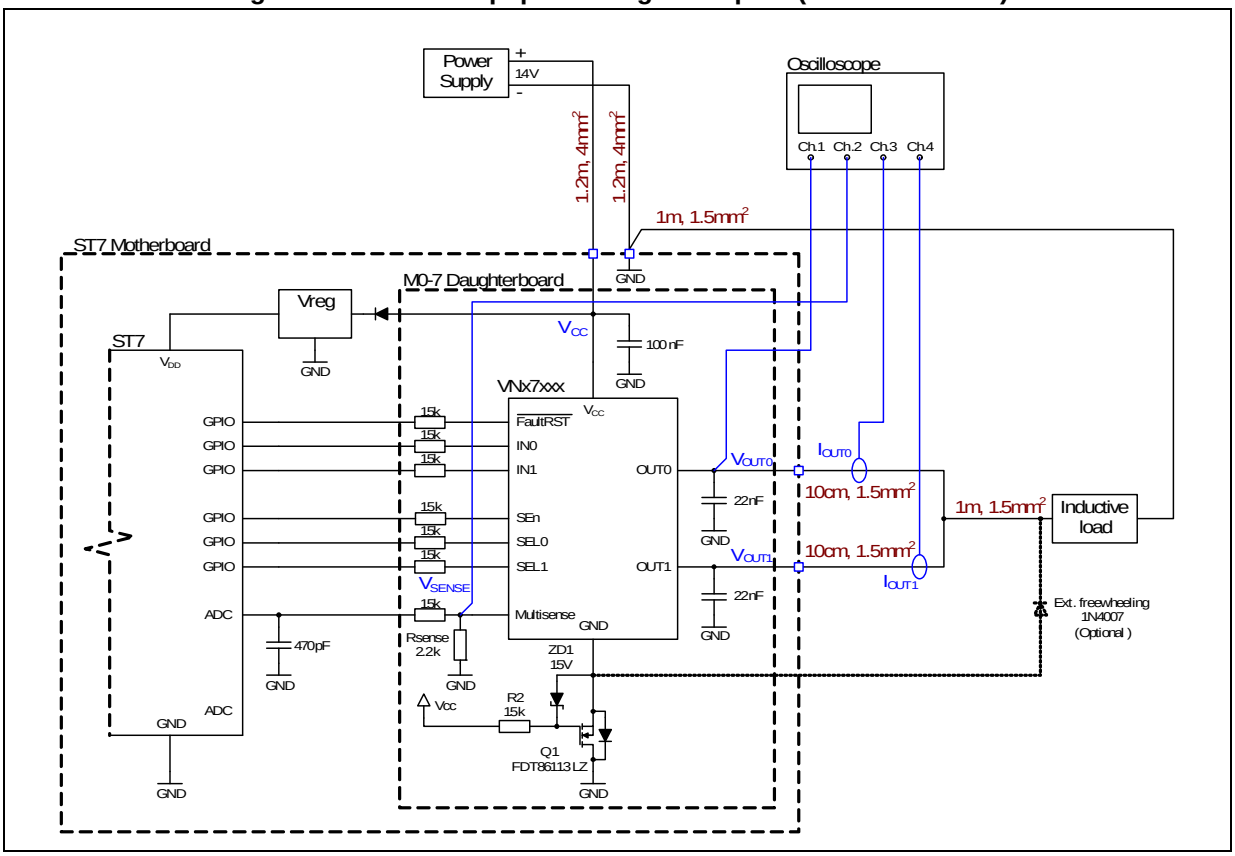


Figure 142. Bulb with 10 µH (VND7040AJ, Ch.0 + Ch.1)

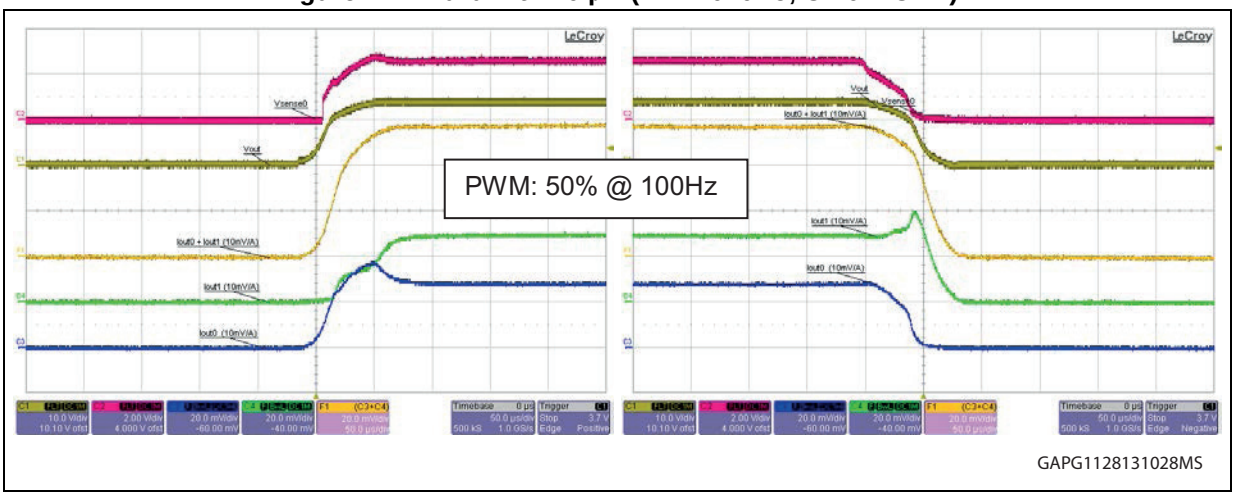


Figure 143. 2 mH / 2.8 Ω (VND7040AJ, Ch.0 + Ch.1)

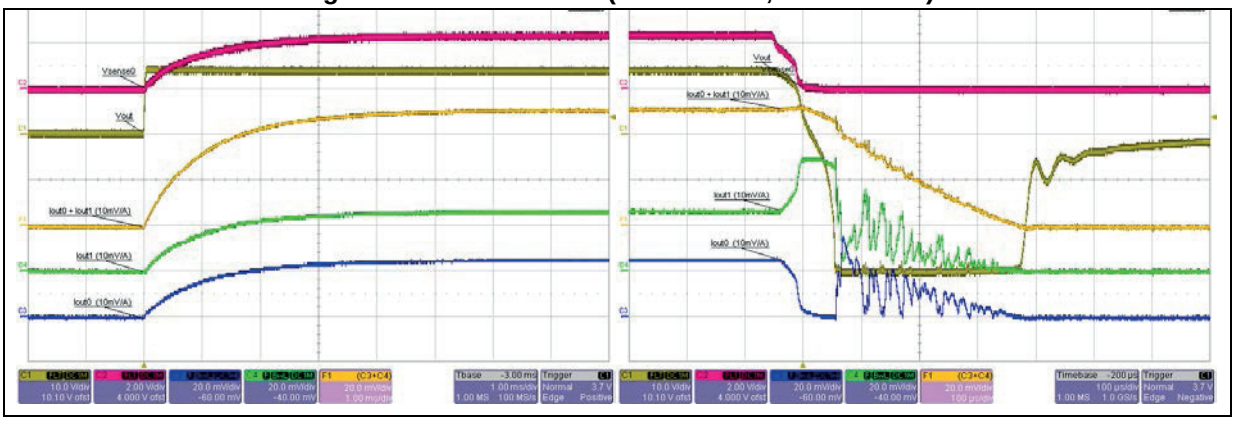
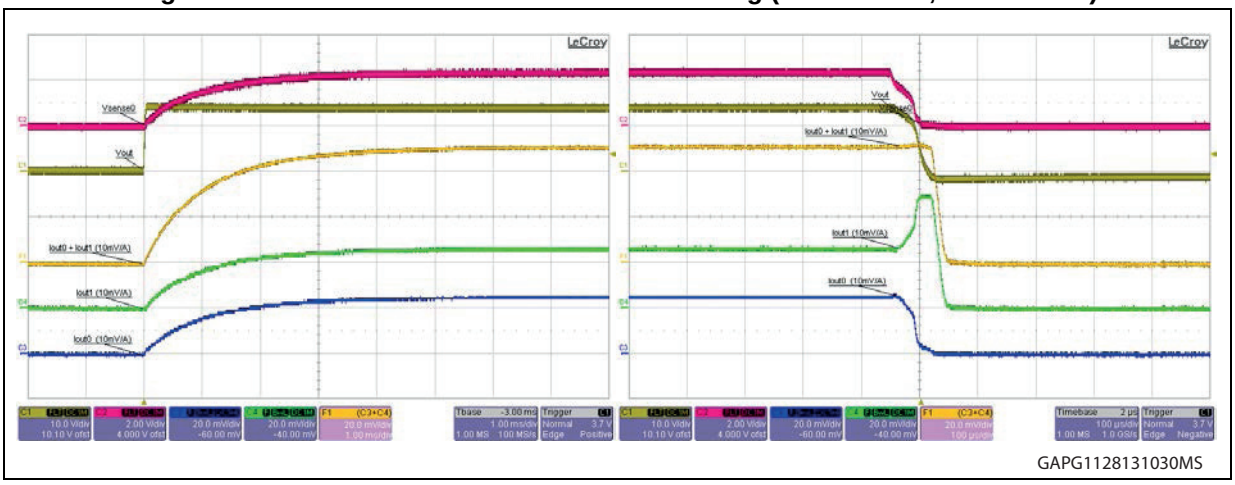


Figure 144. 2mH / 2.8Ω with external freewheeling (VND7040AJ, Ch.0 + Ch.1)



Significant current imbalance is observed during the turn-off phase, even at relatively low inductance values (10 µH) or with external freewheeling. Nevertheless this behavior does not impact the total power dissipation in the device or functionality in steady state conditions. The load current sharing during the demagnetization phase is unstable (see measurement with 2 mH/2.8 Ω). This leads to the conclusion that, in the worst case, total demagnetization energy could be dissipated in one channel only. Therefore the energy capability of a single channel must be sufficient to sustain the whole demagnetization energy. If this is not the case, an external protection must be added (refer to *Section 6.3: Inductive loads*).

The following measurement demonstrates the overload condition (turn-on into the short circuit) on VND7020AJ device with paralleled outputs, configured in latch mode:

- V_{BAT}: 14 V
- Temperature: 25 °C
- Device
  - VND7020AJ (OUT0 + OUT1 paralleled)
- Short circuit parameters
  - 5 µH / 50 mΩ (coil from 1.5 mm^2 cable)

Figure 145. Test setup – inductive short circuit test with paralleled outputs

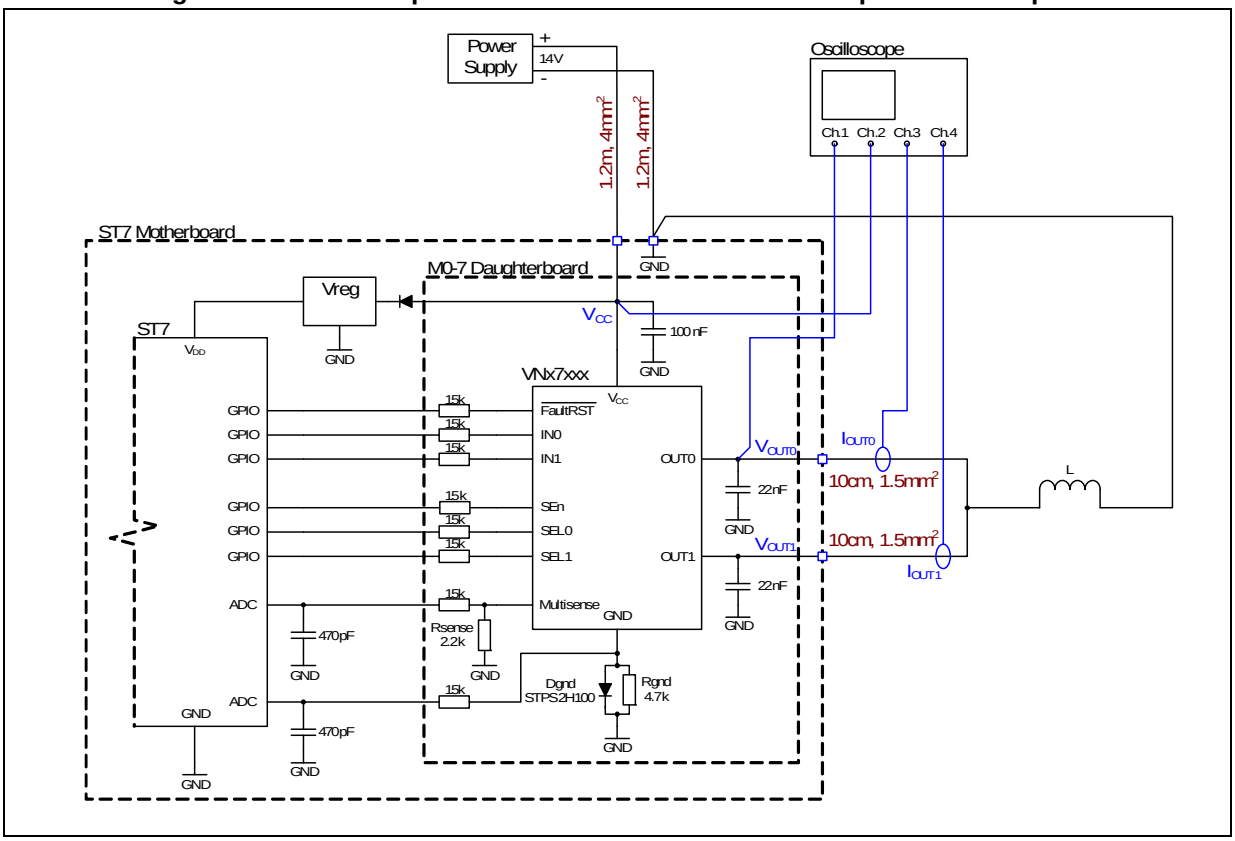
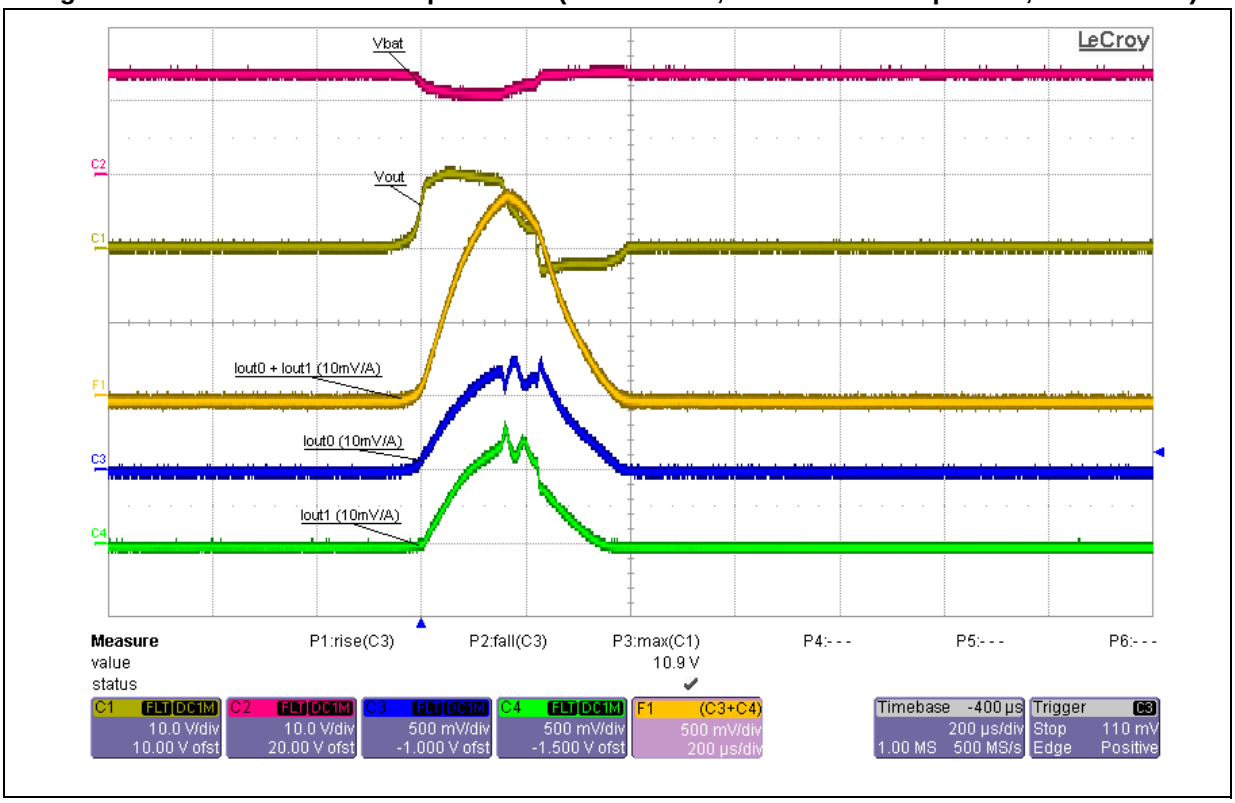


Figure 146. Inductive short – 5 µH/50 mΩ (VND7020AJ, Ch0 and Ch1 in parallel, Latch mode)



As seen from the measurement the device latches-off after the first power limitation pulse while the current among the channels is distributed almost equally.

Conclusion:

Paralleling of output channels should be restricted to exceptional cases. Due to the significant stray inductance of the wire harness, a paralleling of output channels implies the exposure to a critical high demagnetization energy in case of short circuit conditions impacting the component lifetime. Even a small difference between the channels (turn-off shapes, actual clamping voltage) could lead to almost 100 % current imbalance during the demagnetization phase. In worst case, all inductive energy is dissipated by only one channel. Since the inductive energy is proportional to the square of the load current, the stress in the channel could be four times higher in comparison with non-parallel operation at half of the current with same inductance. Therefore, there is a potential risk of damage even at relatively low inductance values in range of standard wire harness.

In case the paralleling of outputs is required, the devices must be configured in latch mode, to avoid the repetitive demagnetization stress during the power limitation or thermal shutdown cycling.

A special care must be taken in case of inductive V_{BAT} connection (long wire harness). Even a few µH of inductance of the supply line can generate a positive over-voltage pulse on V_{CC} pin at turn-off (latch-off) of the outputs in case of short circuit conditions. This positive pulse could activate the V_{CC} - GND signal clamp and cause damage of the device. Therefore it is recommended, in case of long battery cables, to add >100 µF low ESR electrolytic capacitor between the V_{CC} pin and GND in order to keep the V_{CC} peak voltage safely below the minimum clamping voltage V_{CLAMP}. It is always recommended to run an experimental verification on module level to confirm the correct dimensioning and placement of the

capacitor. Practical experiments on M0-7 HSDs show that this capacitor is not needed in case of paralleling of two channels of high ohmic devices (VND7140AJ).

9 Inverse output current behavior

9.1 Introduction

The objective of this chapter is to describe the robustness of M0-7 monolithic devices submitted to disturbances injected on output in a typical application scheme.

Sometimes, devices operate in condition where the Output voltage can be higher than the supply voltage V_S, for instance because the device is driving a Capacitive (see *Figure 148*) or Inductive Load (for example in case of a DC motor driven in H-Bridge configuration (see *Figure 149*), or because accidentally the Outputs are wired to the battery (see *Figure 149*) or moreover in case of ripples induced by a disturbance sources (for instance ISO pulses on battery which could create transient voltages on Output Power Stage).

Figure 147. Inverse current injected by a capacitive load

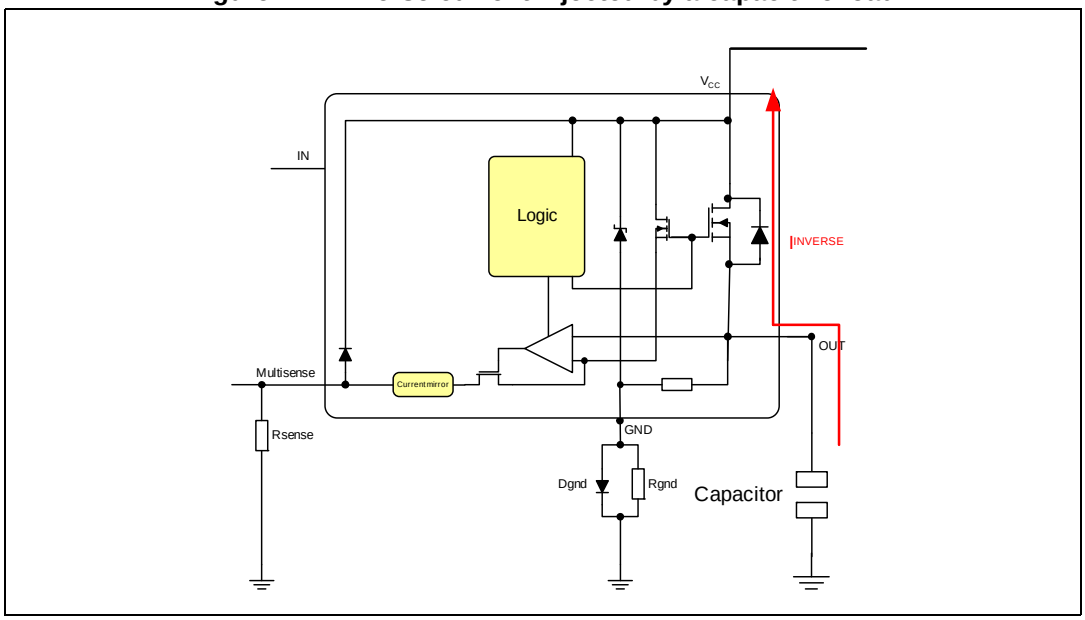


Figure 148. Inverse Current injected by an inductive load in the high-side driver of an H-Bridge

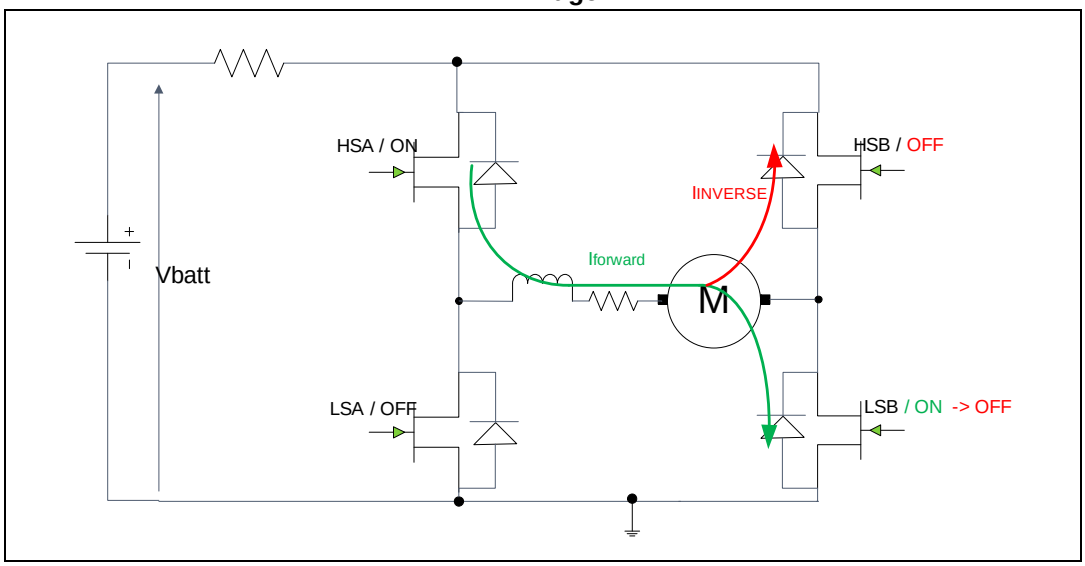
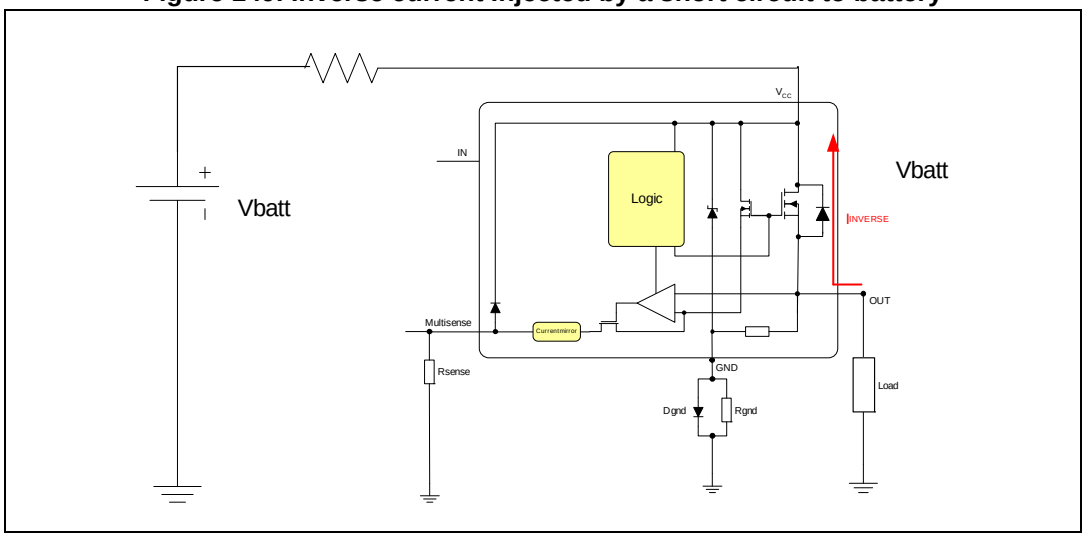


Figure 149. Inverse current Injected by a short circuit to battery



We define $I_{INVERSE}$ the current that flows into the device from the output.

Generally, the conditions above described could become permanent, in case of output short circuit to battery, creating an extra stress on the solid switch.

9.2 Device capability versus inverse current

Considering a generic multichannel high-side driver, in case of inverse current disturbance injected into output, several cases can occur depending on the combination of channels operating conditions (ON or OFF state). A single channel HSD can be intended as a subset of a generic multichannel high-side driver.

The inverse current ($I_{INVERSE}$) could modify the behavior of the channel under test (ChUT) and of the others close by. The analysis is performed both while the channels operate in

static way (permanent operation) and while they are dynamically controlled (PWM operation). The first $I_{INVERSE}$ value that modifies the expected channels behavior is called $I_{INVERSE(th)}$ (Inverse current threshold).

In case of static operation (channel permanently ON or OFF) the $I_{INVERSE(th)}$ changes either the ChUT and the others previous state.

In case of dynamic operation, the $I_{INVERSE(th)}$ inhibits the effect of the input command used to change the channel state (for instance the $I_{INVERSE(th)}$ inhibits the turn ON of the ChUT and the others while are in OFF state at the time the inverse current is applied).

Moreover the effects of the $I_{INVERSE}$ are reported looking at the behavior of the diagnostic that could be modified by this current injection.

Effects of $I_{INVERSE}$ are reported in the two following operating conditions:

1. Device in steady operation (DC operation)
2. Device in PWM operation

9.2.1 Device in steady state

Based on channels permanent status, three major cases can be identified as reported below:

1. Device sensitivity of channels permanently ON for dynamic inverse output current:
   Device state: all channels in ON state (Inputs high) and loaded
   Test execution: Increasing Inverse Current is injected in a channel (the ChUT), up to the $I_{INVERSE(th)}$
2. Device sensitivity of channels permanently OFF for dynamic inverse output current:
   Device state: all channels in OFF state, with all channels loaded (inputs low)
   Test execution: Increasing Inverse Current is injected in a channel up to the $I_{INVERSE(th)}$
3. Device sensitivity of channels either permanently ON or OFF for dynamic inverse output current while ChUT state is opposite to the one of the adjacent channel
   i) Channel “ch_i” set in OFF state while other Channel “ch_j” is in ON state, and loaded
   ii) Channel “ch_i” set in ON state while other Channel “ch_j” is in OFF state, and loaded

Table 29. Example of channels configuration on a dual channels HSD

Test ID	Channels configuration Chi/Chj	ChUT	mcs status	Signals monitored			
1.	ON / ON	Chi	Enable	V_{OUT}	CurrentSense and diagnostic flag	V_{CC} feedback	T_{CASE} feedback
3.-i	OFF / ON						
3.-ii	ON / OFF						
2.	OFF / OFF						
1.	ON / ON		Disable				
3.-i	OFF / ON						
3.-ii	ON / OFF						
2.	OFF / OFF						

This analysis results are reported in *Table 33*. Test conditions: V_{BAT} = 12 V, and room temperature (values in the table are representative of experimental results on a limited sample base.

In the *Table 33* following symbols are given:

- [V_F] is the body-diode forward voltage at room temperature
- [d] is a delta voltage between V_{CC} and V_{OUT}, with a value lower than V_F.
- [V_{SENSEH}] is the fault MultiSense voltage.
- [V_{OL}] is the OFF state open-load detection threshold

Table 30. Inverse current threshold experimental values according to channels status (Ch0 is the channel under test, Ch0 = ON)

Part number		Channel configuration (MultiSense enabled in current monitor mode)									
		Ch0 = ON; Ch1 = ON					Ch0 = ON; Ch1 = OFF				
		RL_ch0 = 10 k / RL_ch1 = 10 k					RL_ch0 = 10 k / RL_ch1 = 10 k				
		I_injected on Ch0[mA]	V_{OUT} [V]		V_{SENSE} configuration		I_injected on Ch0[mA]	V_{OUT} [V]		V_{SENSE} configuration	
			Ch0	Ch1	Cs0	Cs1		Ch0	Ch1	Cs0	Cs1
VND7020AJ		26800	V_{CC}+d	V_{CC}	0	0	27600	V_{CC}+d	0	0	0
	$I_{INVERSE(th)}$	29200	V_{CC}+V_F	V_{CC}	V_{SENSEH}	0	28400	V_{CC}+V_F	>V_{OL}	V_{SENSEH}	V_{SENSEH}
VND7140AJ		3500	V_{CC}+d	V_{CC}	0	0	3500	V_{CC}+d	0	0	0
	$I_{INVERSE(th)}$	3700	V_{CC}+V_F	V_{CC}	V_{SENSEH}	0	3700	V_{CC}+V_F	>V_{OL}	V_{SENSEH}	V_{SENSEH}
VN7010AJ		45000	V_{CC}+d	—	0	—	—	—	—	—	—
	$I_{INVERSE(th)}$	50000	V_{CC}+V_F	—	V_{SENSEH}	—	—	—	—	—	—
VND7040AJ		13700	V_{CC}+d	V_{CC}	0	0	13000	V_{CC}+d	0	0	0
	$I_{INVERSE(th)}$	14500	V_{CC}+V_F	V_{CC}	V_{SENSEH}	0	14100	V_{CC}+V_F	>V_{OL}	V_{SENSEH}	V_{SENSEH}
VND7012AJ		41000	V_{CC}+d	V_{CC}	0	0	42900	V_{CC}+d	0	0	0
	$I_{INVERSE(th)}$	41400	V_{CC}+V_F	V_{CC}	V_{SENSEH}	0	44300	V_{CC}+V_F	<V_{OL}	V_{SENSEH}	0

Table 30. Inverse current threshold experimental values according to channels status (Ch0 is the channel under test, Ch0 = ON) (continued)

Part number		Channel configuration (MultiSense enabled in current monitor mode)									
		Ch0 = ON; Ch1 = ON					Ch0 = ON; Ch1 = OFF				
		RL_ch0 = 10 k / RL_ch1 = 10 k					RL_ch0 = 10 k / RL_ch1 = 10 k				
		I_injected on Ch0[mA]	V_{OUT} [V]		V_{SENSE} configuration		I_injected on Ch0[mA]	V_{OUT} [V]		V_{SENSE} configuration	
			Ch0	Ch1	Cs0	Cs1		Ch0	Ch1	Cs0	Cs1
VN7004AH-E		201800	V_{CC}+d	—	0	—	—	—	—	—	—
	$I_{INVERSE(th)}$	212800	$V_{CC}+V_F$	—	V_{SENSEH}	—	—	—	—	—	—

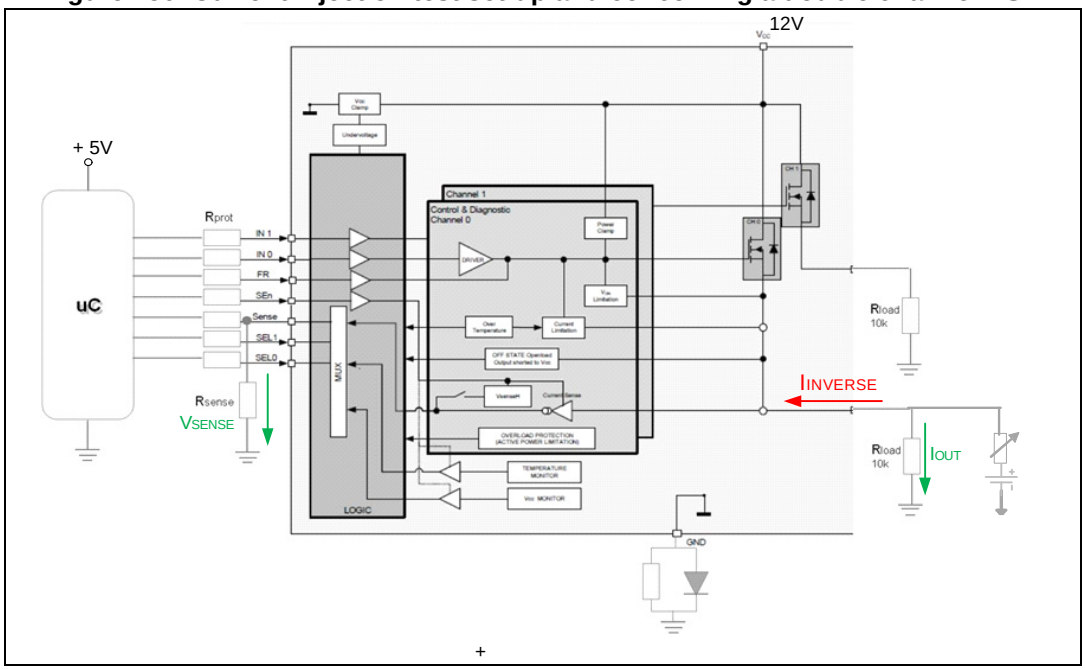
Table 31. Inverse current threshold experimental values according to channels status (Ch0 is the channel under test, Ch0 = OFF)

Part number		Channel configuration (MultiSense enabled in current monitor mode)									
		Ch0 = OFF; Ch1 = ON					Ch0 = OFF; Ch1 = OFF				
		RL_ch0 = 10 k / RL_ch1 = 10 k					Ch0 = floating / RL_ch1 = 10 k				
		I_injected on Ch0[mA]	V_{OUT} [V]		V_{SENSE} configuration		I_injected on Ch0[mA]	V_{OUT} [V]		V_{SENSE} configuration	
			Ch0	Ch1	Cs0	Cs1		Ch0	Ch1	Cs0	Cs1
VND7020AJ		0.7	V_{CC}+d	V_{CC}	V_{SENSEH}	0	0.7	V_{CC}+d	0	V_{SENSEH}	0
	$I_{INVERSE(th)}$	30	$V_{CC}+V_F$	V_{CC}	V_{SENSEH}	0	30	$V_{CC}+V_F$	>0, <V_{OL}	V_{SENSEH}	0
VND7140AJ		0.7	V_{CC}+d	V_{CC}	V_{SENSEH}	0	0.7	V_{CC}+d	0	V_{SENSEH}	0
	$I_{INVERSE(th)}$	30	$V_{CC}+V_F$	V_{CC}	V_{SENSEH}	0	30	$V_{CC}+V_F$	>0, <V_{OL}	V_{SENSEH}	0
VN7010AJ		0.7	V_{CC}+d	—	V_{SENSEH}	—	—	—	—	—	—
	$I_{INVERSE(th)}$	30	$V_{CC}+V_F$	—	V_{SENSEH}	—	—	—	—	—	—

Table 31. Inverse current threshold experimental values according to channels status (Ch0 is the channel under test, Ch0 = OFF) (continued)

Part number		Channel configuration (MultiSense enabled in current monitor mode)									
		Ch0 = OFF; Ch1 = ON					Ch0 = OFF; Ch1 = OFF				
		RL_ch0 = 10 k / RL_ch1 = 10 k					Ch0 = floating / RL_ch1 = 10 k				
		I_injected on Ch0[mA]	V_{OUT} [V]		V_{SENSE} configuration		I_injected on Ch0[mA]	V_{OUT} [V]		V_{SENSE} configuration	
			Ch0	Ch1	Cs0	Cs1		Ch0	Ch1	Cs0	Cs1
VND7040AJ		0.7	V_{CC}+d	V_{CC}	V_{SENSEH}	0	0.7	V_{CC}+d	0	V_{SENSEH}	0
	$I_{INVERSE(th)}$	30	V_{CC}+V_F	V_{CC}	V_{SENSEH}	0	30	V_{CC}+V_F	>0, <V_{OL}	V_{SENSEH}	0
VND7012AJ		0.4	V_{CC}+d	V_{CC}	V_{SENSEH}	0	0.4	V_{CC}+d	0	V_{SENSEH}	0
	$I_{INVERSE(th)}$	10	V_{CC}+V_F	V_{CC}	V_{SENSEH}	0	10	V_{CC}+V_F	>0, <V_{OL}	V_{SENSEH}	0
VN7004AH-E		0.4	V_{CC}+d	—	V_{SENSEH}	—	—	—	—	—	—
	$I_{INVERSE(th)}$	10	V_{CC}+V_F	—	V_{SENSEH}	—	—	—	—	—	—

Figure 150. Current Injection test set-up and concerning a double channel HSD



9.2.2 Device driven in PWM

Effects of $I_{INVERSE}$ are evaluated for devices driven in PWM as well. Based on channels dynamic status, four major cases can be identified as below reported:

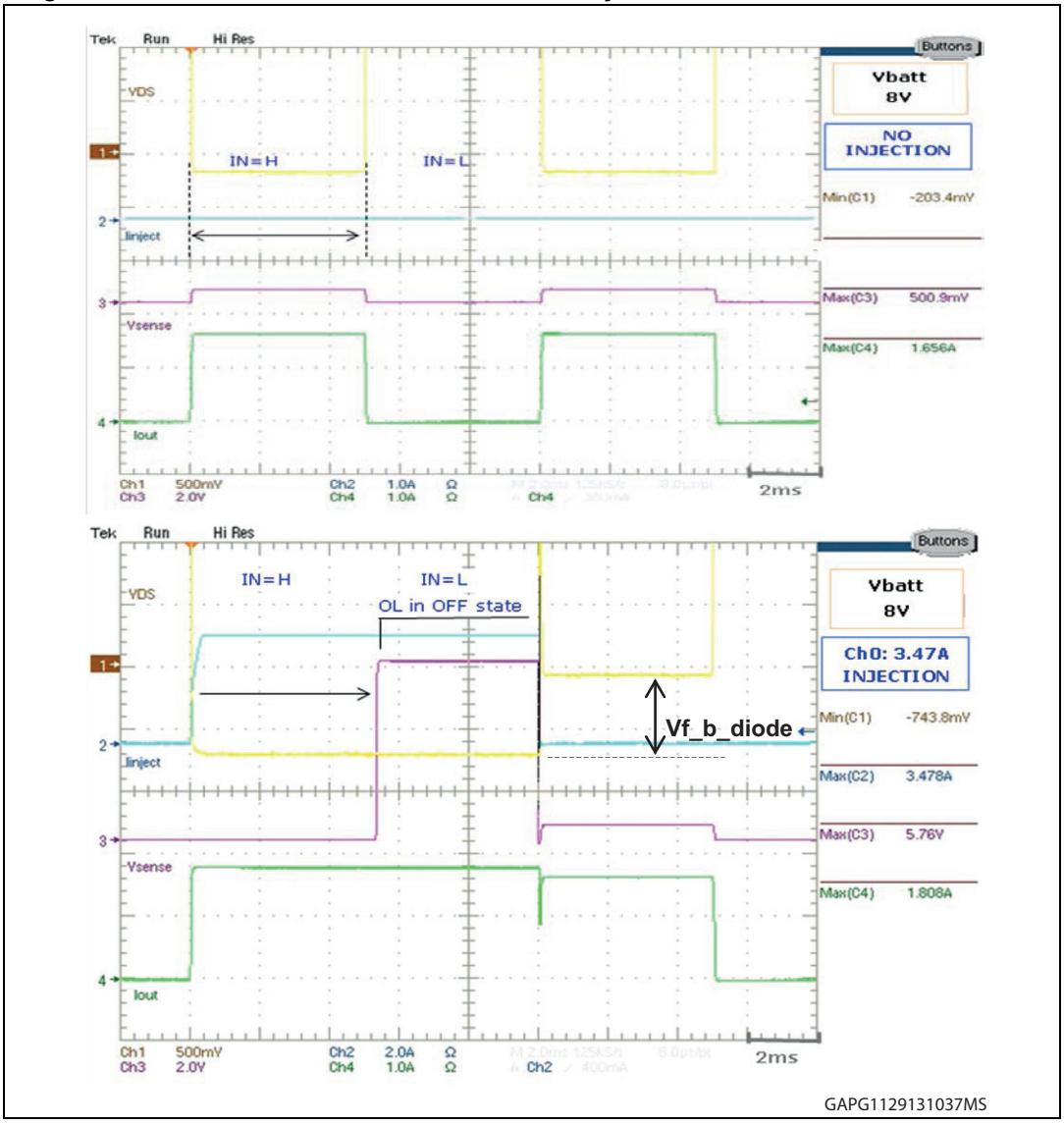
1. Device state: ChUT in PWM.

   Test execution: Increasing Inverse Current is injected in a channel (the ChUT) up to the $I_{INVERSE(th)}$ while the ChUT is driven OFF

In that case if the INPUT goes from low to high, during inverse current injection, the output stage is kept OFF and cannot be switched back ON until $I_{INVERSE}$ disappears.

As soon as $I_{INVERSE(th)}$ is reached, the ChUT sense signal is set to high impedance or V_{SENSEH}, depending if it is in ON or OFF state respectively. The MultiSense current monitor behavior can be identified as an open load indication (see *Figure 151*).

Figure 151. Waveforms related to the inverse injection on a channel driven in PMW



2. Device state: ChUT in PWM. Test execution: Increasing Inverse Current is injected in a channel (the ChUT) up to the $I_{INVERSE}$ while the ChUT is driven ON

The $I_{INVERSE(th)}$, in this case is much higher than case a). The ChUT is turned OFF and there is no possibility to switch it back ON.

3. Device state: ChUT in PWM.
   Test execution: Increasing Inverse Current is injected in a channel (the ChUT) up to the $I_{INVERSE(th)}$ while all others are permanently ON.

Regardless of the ChUT dynamic state (either ON or OFF), no influence on the other channels behavior is reported.

In such condition the diagnosis of channels not under test is correct and reflects real output current.

4. Device state: ChUT in PWM. Test execution: Increasing Inverse Current is injected in a channel (the ChUT) up to the $I_{INVERSE(th)}$ while all others are permanently OFF.

As soon as the $I_{INVERSE}$ is applied all other channels show increased $I_{L(Off)}$ position dependent. The closer is the channel to the ChUT, the higher is the $I_{L(Off)}$.

During injection, any variation of V_{CC} signal due to the influence of current injected into the output can be well monitored by the multi-sense functionality set in V_{CC} mode.

9.3 Conclusions

In case of inverse current disturbance injected into output, device works properly and the output stage follows the state of the IN pin, as long as the injected current does not exceed a certain threshold.

The inverse current threshold value, which modifies the device functionality depends on channels Status (ON or OFF state).

In particular, the inverse current which inhibits device operation, with channels in ON state, is proportional to the ratio between V_F and R_{ON}:

$$I_{INVERSE(th)} \propto \frac{V_F}{R_{ON}}$$

where:

- V_F is the body-diode forward voltage at room temperature: typical value is 0.7 V
- R_{ON} is the value of ON state resistance of PowerMOS at room temperature

Instead, in case of channels OFF, the threshold current is almost constant and does not depend on R_{ON} value. Its value is about 0.6 mA for monolithic devices and 0.4 mA for hybrid devices.

The reason behind this different behavior between the ON and OFF channel state can be explained by the device structure itself.

The triggering event that modifies the channel under test behavior when in OFF state and during inverse current injection is the (V_{OUT}-V_{CC}) value. As soon as this value approaches the threshold of the intrinsic anti-parallel diode or, in other words, as soon as some current flows through this diode, NPN bipolar parasitic components between PowerMOS gate and battery pin (V_{CC}) are triggered. This does not allow to switch the channel under test back on.

10 ESD protection

10.1 EMC requirements for ESD at module level

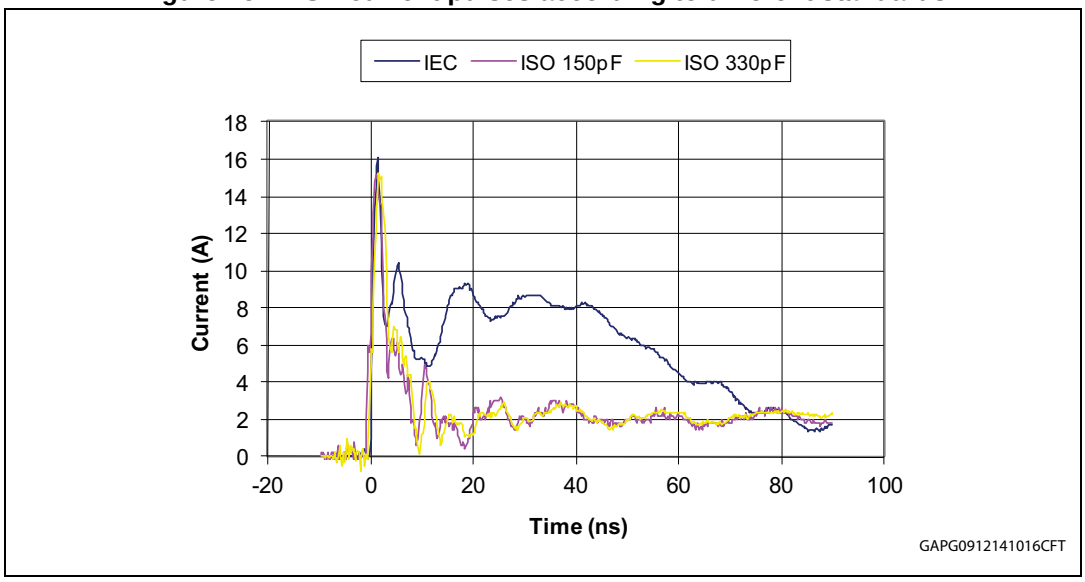
An Electrostatic Discharge (ESD) pulse on any ECU connector pin is an expected event during the life of a car. A transfer of discharge when a person approaches the ECU (for example during maintenance, reparation or installation) is a typical event that could damage the ECU and in particular an IC whose pins are connected to the outside environment.

Standards and limits are applied in order to simulate those events but they strongly depend on the car maker specification and on the application. Some international standards for testing schemes and requirements have been introduced for the electrical systems such as car modules. They include IEC 61000-4-2 and the automotive standard ISO 10605.

The two standards use different values for the C/R components. IEC 61000-4-2 uses a 330 Ω resistor and a 150 pF capacitor. ISO 10605 uses a 2000 Ω resistor but different capacitances depending on condition. A 150 pF capacitor is used to simulate a person reaching into an automobile (for example a module loads repair or change can be reproduced by this standard). A 330 pF capacitor is used to simulate ESD events for a person sitting in the passenger compartment in a vehicle.

Such ESD pulses are made by two components: a capacitive and a resistive one; the first one, made by a pure peak current in the first nanoseconds of the pulse, strongly depends on the distributed capacitance of the ESD simulator body. The resistive one is made by the RC content of the standard used (see *Figure 152*).

Figure 152. ESD current pulses according to different standards



Typical car makers ESD requirements at module level are the following:

1. Module not powered during the test.

   This test simulates any possible handling of the module before being assembled in the car.

   Connector pins to test are normally the ones that go out of the module:

   – Supply pins protected and/or filtered as per datasheet;
   – Output pins protected and/or filtered as per typical design practice (e.g. ceramic capacitor).

   Standard applied is the ESD HBM Automotive acc. IEC61000-4-2 (150 pF/330 Ω).

   Required acceptance limits are in ± 4 KV - ± 8 KV range (contact discharge).

   Test execution requires a sequence of 3 to 5 ESD pulses applied with fixed delay time (1s typically). Pulses are applied either by touching the pin under test with the ESD gun (contact discharge) or without touching it (air discharge).Test is passed if no pin to pin I/V characteristic degradation is reported after pulses exposure. This test simulates any possible handling of the module before being assembled in the car. In some cases extra test with a modified HBM network (for example 150 pF/2 KΩ) contact discharge are required.

2. Module powered during the test

   This test normally simulates any possible stress that could be applied to the connector pins with module already assembled in car.

   The standard typically applied is the ISO10605 (330 pF/2 KΩ).

   Acceptance limits are in the ± 8 KV range (contact discharge) and ± 15 KV (air discharge).

   In some cases, if higher pulse level is required, the applied network changes in (150 pF/2 KΩ).

   Test execution requires a sequence of 3-5 ESD pulses applied with fixed delay time. Real car battery must be used.

   Module must be inserted in a test environment that simulates a car. It is normally ESD tested in real configuration (loads on, load off, driver in PWM…).

   Pulses are applied to the pins that go out of the module such as outputs, transceivers pins.

   Test is passed if no pin to pin I/V characteristic degradation is reported after pulses exposure.

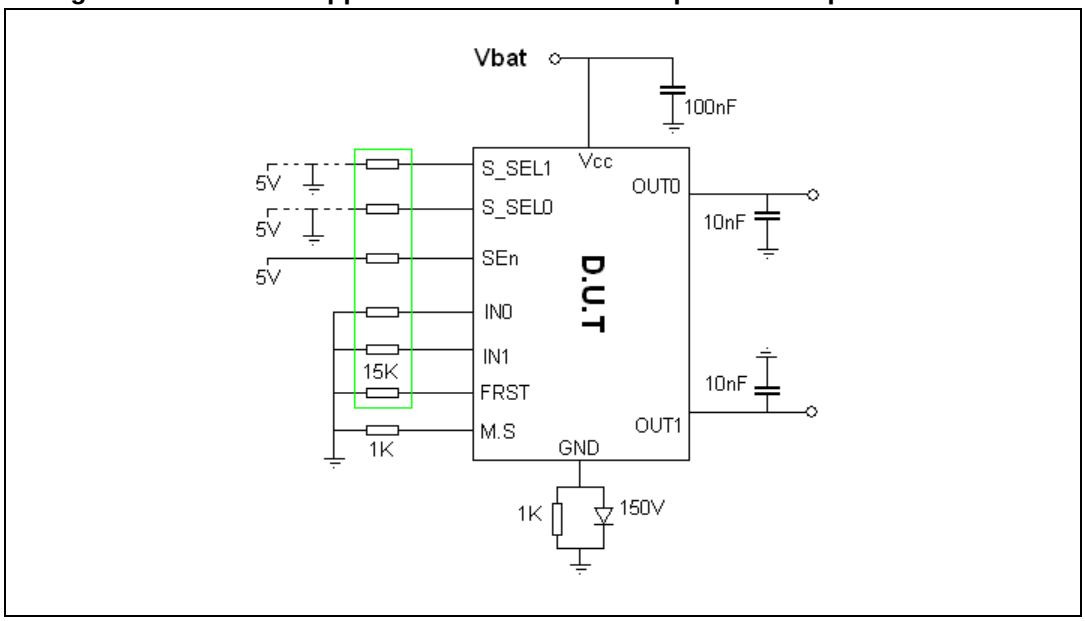
   ESD pulses are applied between the pin under test and module ground connected to the ESD GND plane by a minimum wire.

   It has been demonstrated some variability of the ESD. Main causes of such variability are in general the environmental conditions (humidity mainly), the ESD simulator pulse spread (specifically of the initial current pulse) and the test execution as well.

   The M07 HSDs are characterized with powered and unpowered module ESD tests.

   In *Figure 153* the application schematic for a powered test performed on a dual channel device which is the Device Under Test (DUT) is shown:

Figure 153. ESD test application scheme for HSD placed on a powered module



Test set-up:

- The wire length between V_{BAT} and DUT V_{CC} and between board GND and ESD ground plane is minimized. ESD Simulator ground is identical to battery ground. Both are connected on GND plane;
- DUT Board is placed above GND plane by means 50 mm thick insulating support;
- Filtering ceramic (X7R series) capacitors are placed on V_{CC} and on outputs.
- DUT outputs not loaded;
- In case of unpowered module test, the supply voltage is not present and the device signal pins are connected to GND via the commonly used protection resistances.

Test conditions:

- V_{BAT} from real car battery = 12.6 V (in case of powered module test only);
- Room temperature;

Test execution:

- Tests are performed on two typical device configurations, in case of powered module test;
- ESD discharges are applied on output board trace.

Test procedure:

- Incremental discharge voltage levels from 1 KV up to 30 KV are applied with 1 KV voltage step
- 5 discharges on discharge pad OUTx with delay time of 1sec are applied
- failure test by I/V curve check
- previous points are repeated till failure (if any)

Devices performances are guaranteed by margin to failure reported during characterization.

The test is performed on specific ESD test boards where general ESD layout rules are applied.

The ESD characterization has demonstrated the capability of M0-7 HSDs to pass the ESD levels normally required. Following results are reported:

Table 32. M0-7 HSDs ESD results

	ESD at module level (powered)	ESD at module level (unpowered)
Sustained ESD pulse level	> |+/-8 KV|	> |+/-8 KV|

10.2 EMC Requirements for ESD at device level

ESD tests for electrical components such as integrated circuits include:

- Human Body Model (HBM),
- Charged Device Model (CDM).

Those ESD test methods for integrated circuits are intended to insure that the circuits can be safely handled in an ESD controlled environment during manufacture.

HBM:

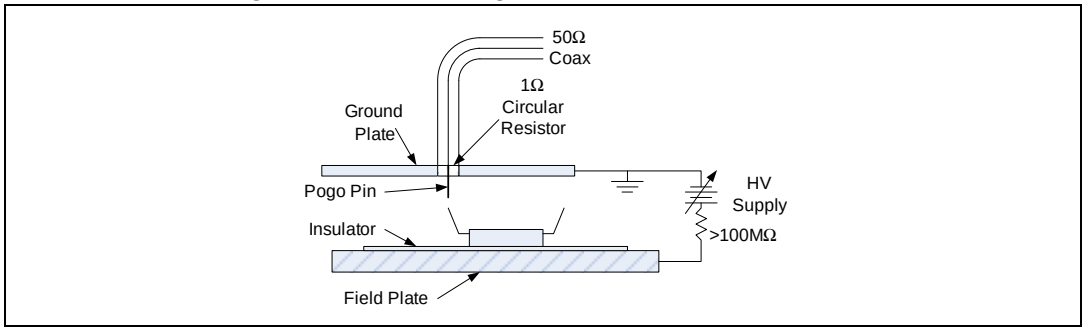
It is intended to simulate a charged person touching an integrated circuit. A person has approximately 100 pF of capacitance and skin and body resistance limit the current during a discharge. HBM tests results, according to JEDEC 22A-114F and CDM-AEC-Q100-011, are reported in M0-7 datasheets' Absolute Maximum Ratings.

CDM:

This test (CDM-AEC-Q100-011) emulates an integrated circuit which becomes charged and discharges when it touches a grounded metal surface. There is no fixed value of a capacitor to discharge; the capacitance to be charged is the capacitance of the integrated circuit to its surroundings. The discharge path, consisting only of the circuit's pin and the arc formed between pin and the metal surface, has very little impedance to limit current.

In the Field Induced CDM, the most popular implementation, the integrated circuit is placed pins up, on top of a field plate, with only a thin insulator between the circuit and the field plate. The thin space between the circuit and the field plate creates a capacitance whose value depends on the size of the integrated circuit and the package geometry. A ground plane is positioned by a pogo pin over the field plate as shown in *Figure 154*.

Figure 154. ESD charge device model test scheme



To perform the CDM test an uncharged circuit is placed on the field plate. The field plate is charged to a high voltage and the circuit's potential tracks the field plate. The ground plane is then moved so that the pogo pin touches the integrated circuit, grounding it. The result is

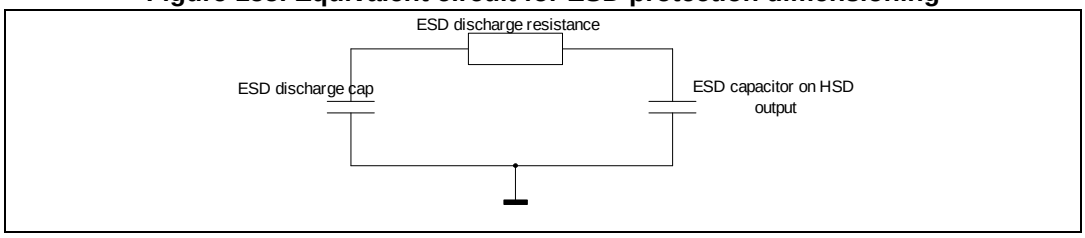
a very fast redistribution of charge between the field plate to ground plate capacitance and the integrated circuit to field plate capacitances. 500V is the commonly used value.

Results relevant to CDM-AEC-Q100-011 are reported in M0-7 datasheet's Absolute maximum Values. Devices performances are guaranteed by margin to failure reported during characterization.

10.3 Design and layout basic suggestions to increase ESD failure point level

When the ESD pulse level required to be passed exceeds the standalone device capability, the HSD needs an external protection. The easiest and less expensive design practice is the use of a ceramic capacitor on the output. The capacitor goal is to limit the voltage and then the energy discharged into the device. This external capacitor builds a capacitive divider with the internal ESD pulse one (see *Figure 155*).

Figure 155. Equivalent circuit for ESD protection dimensioning



A preliminary estimation of the capacitor value can be obtained applying the following formula:

$$V_{Final} = V_{ESD} \cdot \left(\frac{C_{ESD}}{C_{ESD} + C_{EXT}} \right)$$

Where V_{ESD} is the ESD pulse level required, C_{ESD} is the ESD simulator capacitor value and V_{final} is the maximum allowed voltage across the HSD (typically around 45 V).

It is in any case necessary to verify the choice of the external capacitor, given by the above formula, with the real test. The main reason of that is the behaviour of the capacitor impedance over the frequency. More specifically, since an ESD pulse has frequency content in the range of hundreds of MHz the capacitive value of a real capacitor is lower than the theoretical one.

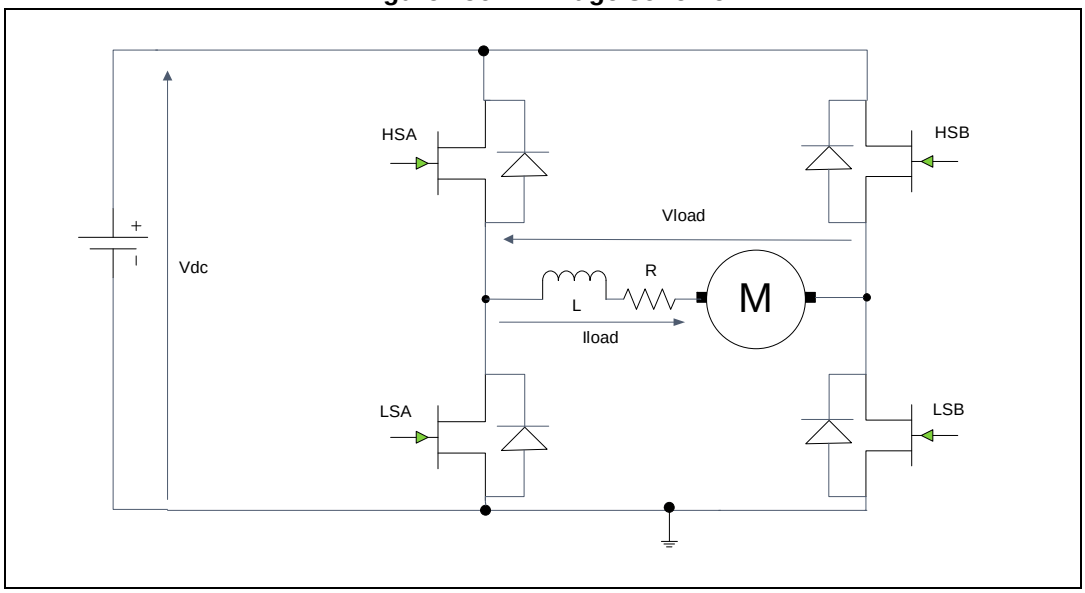
The ESD pulse destruction value strongly depends on the module layout. In order to make the module pass the required stress level, it is recommended to add a ceramic capacitor to the output close to the connector whose value could be in the range of tens of nF. This capacitor decreases both the applied voltage gradient and the maximum output voltage seen by the HSD.

11 Usage in “H-Bridge” configurations

11.1 Introduction

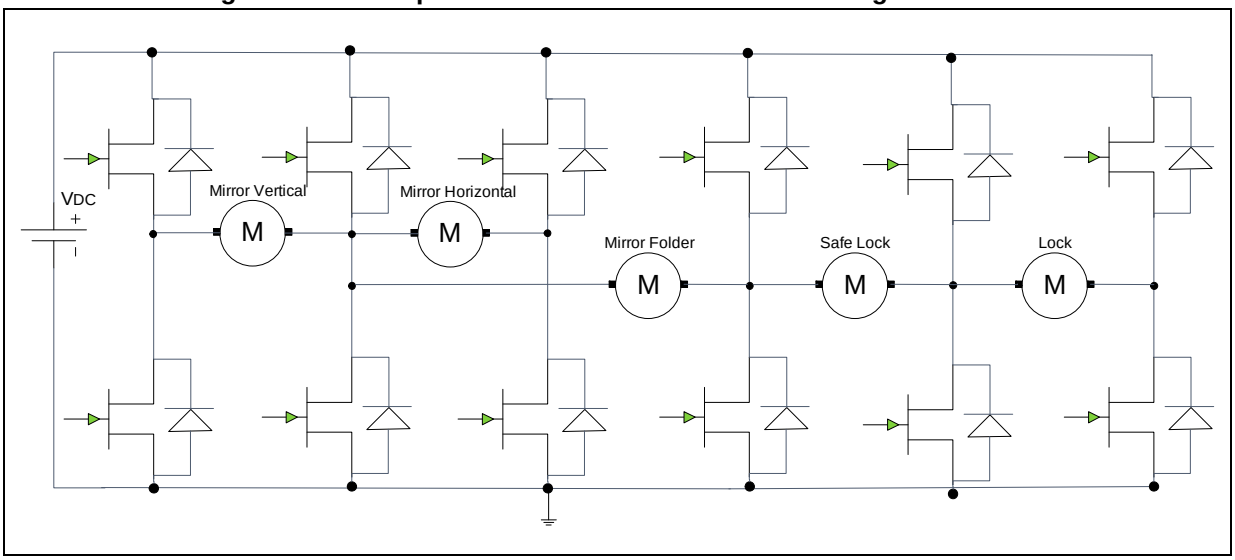
The term H-Bridge refers to the typical graphical representation of such a circuit. An H bridge is built with four switches (solid-state or mechanical). Two of them are connected between the battery and the load (high-side switches), the other two between the load and the ground (low-side switches). When the switches HSA and LSB (according to the *Figure 156*, where a basic circuit with four MOSFETs driving a bidirectional DC motor is shown) are closed (and HSB and LSA are open) a positive voltage will be applied across the motor. By opening HSA and LSB switches and closing HSB and LSA switches, this voltage is reversed, allowing reverse operation of the load (in most cases a DC Motor).

Figure 156. H-Bridge scheme



Using the nomenclature above, the switches HSA and LSA (or HSB and LSB) should never be closed at the same time, as this would cause a short circuit on the input voltage source. This condition creates the so called cross current. A simpler configuration called *Half Bridge,* consists of a single high-side driver which opens or closes the load towards the battery, the loads itself which is directly grounded and a low-side driver in parallel to the load (normally inductive), which is activated only to connect the load to ground. The low-side driver in this way absorbs the inductive energy which otherwise would be completely discharged through the high-side driver with a consequent possible damage in case the energy exceeds its capability. In case of a DC motor, the low-side driver, when turned on after having turned the high-side driver off, brakes the motor safely to ground and stops it. Finally more than two Half Bridges can be connected together in order to drive at least two different loads in cascaded configurations (see in *Figure 157* an example of an automobile front door system with a total of five motors). The independent activation and diagnostic reading of each switch gives large flexibility in those configurations.

Figure 157. Example of automobile multi-motor driving connection



11.2 M0-7 high-side drivers in “H-Bridges”: specific considerations

The M0-7 high-side drivers, single and multichannel, can be used to drive various bidirectional loads in H Bridges configurations. Some general guidelines, should by the way, be applied in order to avoid issues. An overview of some potential issues is given in the following paragraphs.

11.2.1 Short circuit event to ground and to battery

In case of short of one output of the H-Bridge to GND the M0-7 high-side driver protects the H Bridge with its well know protections circuitry (Current Limitation, Power Limitation, Thermal Shutdown with autorestart or latch off). MultiSense pin will signalize V_{SENSEH} like already explained in *Section 7.2.4: Impact of the output voltage to the MultiSense output*.

In case of short circuit of one output of the H Bridge to V_{CC}, the H-Bridge needs an external protection during ON-state because in this case the low-side of the faulty leg will be submitted to the total battery voltage (in case of hard short circuit) or to a part of it (in case of a weak short circuit) with its possible damage. A possibility to guarantee the protection in this conditions would be to implement a drain-source monitoring of the low-side drivers directly via the microcontroller I/Os or to use fully protected low-side drivers (for example LSD belonging to ST’s OMNIFET families).

11.2.2 Cross current events

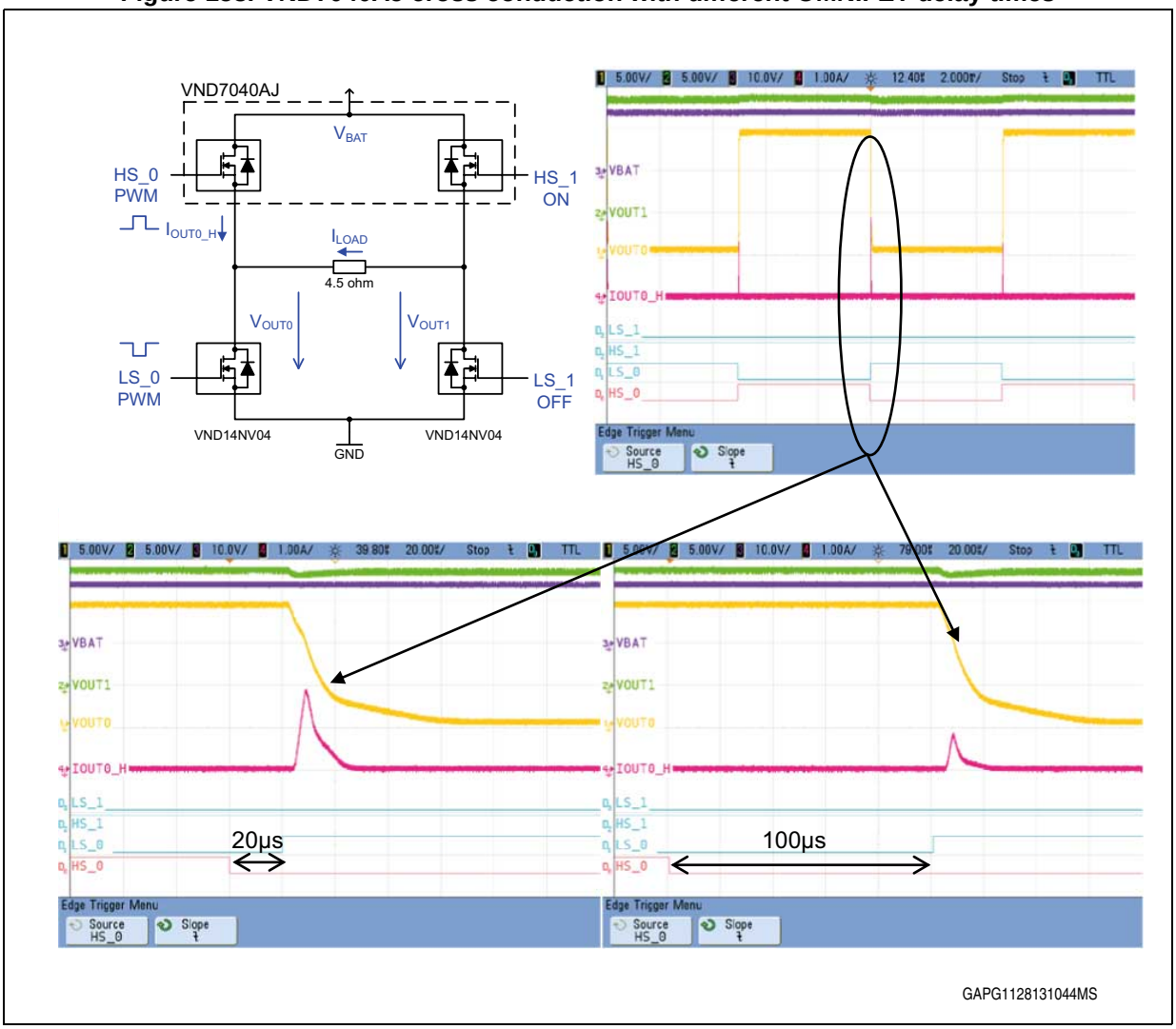
Cross conduction due to MOSFETs delay times

A common issue which can affect one leg of a H-Bridge occurs when both HSD and LSD are on at the same time. This condition, called cross current, can happen even if it is not intended to drive the HSD and LSD simultaneously and can cause significant extra power dissipation which can become critical especially during PWM driving. For instance, when the HSD is turned off and the LSD is turned on (in order for example to change a motor

direction), logic propagation delay and the time required to discharge and charge respectively the HSD and LSD gate capacitances can cause the HSD still to be half on when the LSD is turned on.

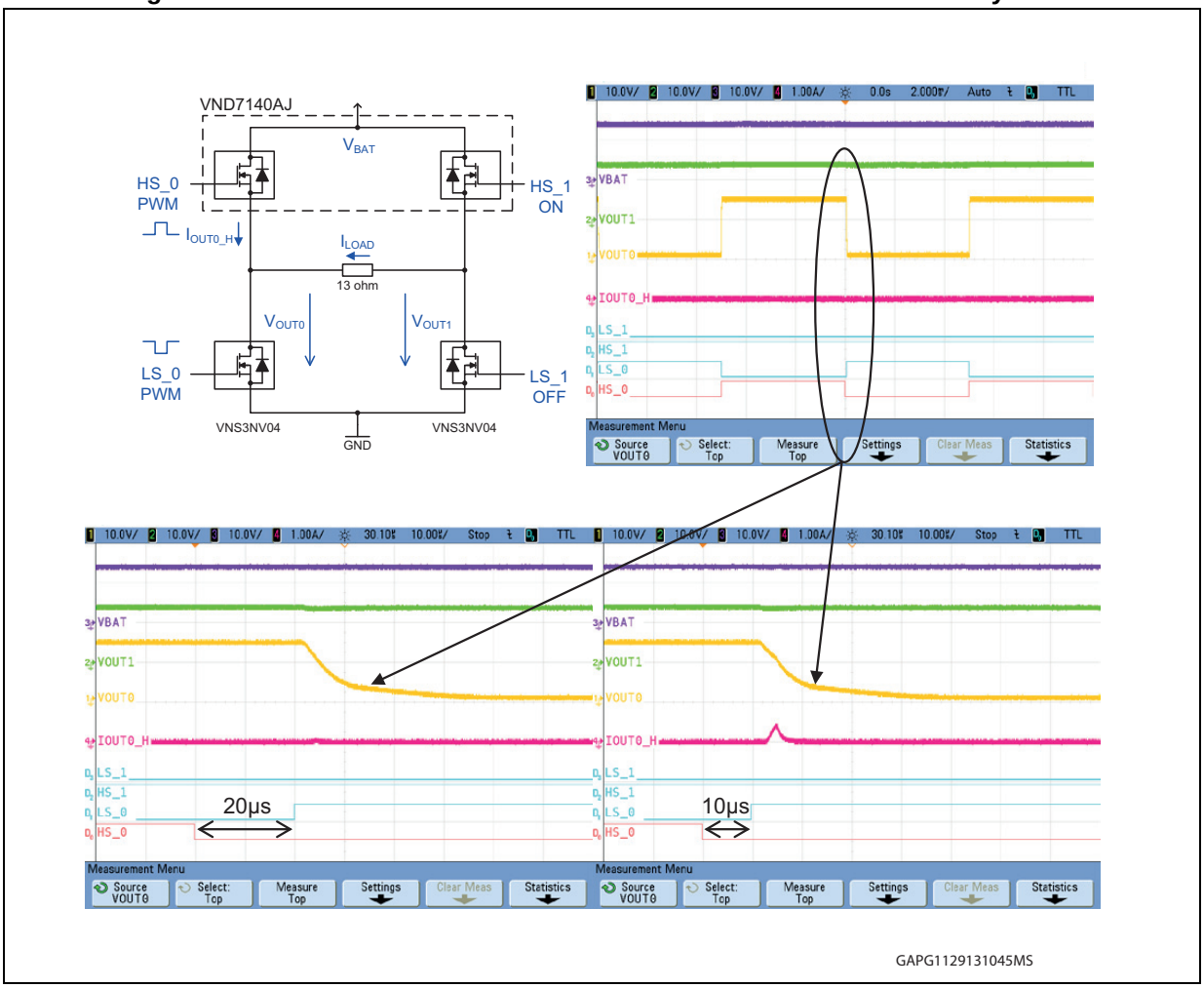
Let us consider a practical example where a VND7040AJ is used in combination with two VND14NV04 (belonging to the OMNIFET II family) to build an H-Bridge. For the sake of simplicity, a resistive load of 4.5 Ω is driven. The HSD_0 and LSD_0 on the left leg are driven complementary with a PWM signal and with different delay times between switching off of the HSD_0 and switching on of the LSD_0; in order to see the effect of the cross conduction and how it can be attenuated or eliminated, a delay has to be introduced. Let us quantify in this example the delay. Current in HSD_0 is plotted.

Figure 158. VND7040AJ cross conduction with different OMNIFET delay times



In the left side plot of *Figure 159* a delay of 20 µs only is given, on the right side a delay of 100 µs is given and still it is possible to see a residual cross current.

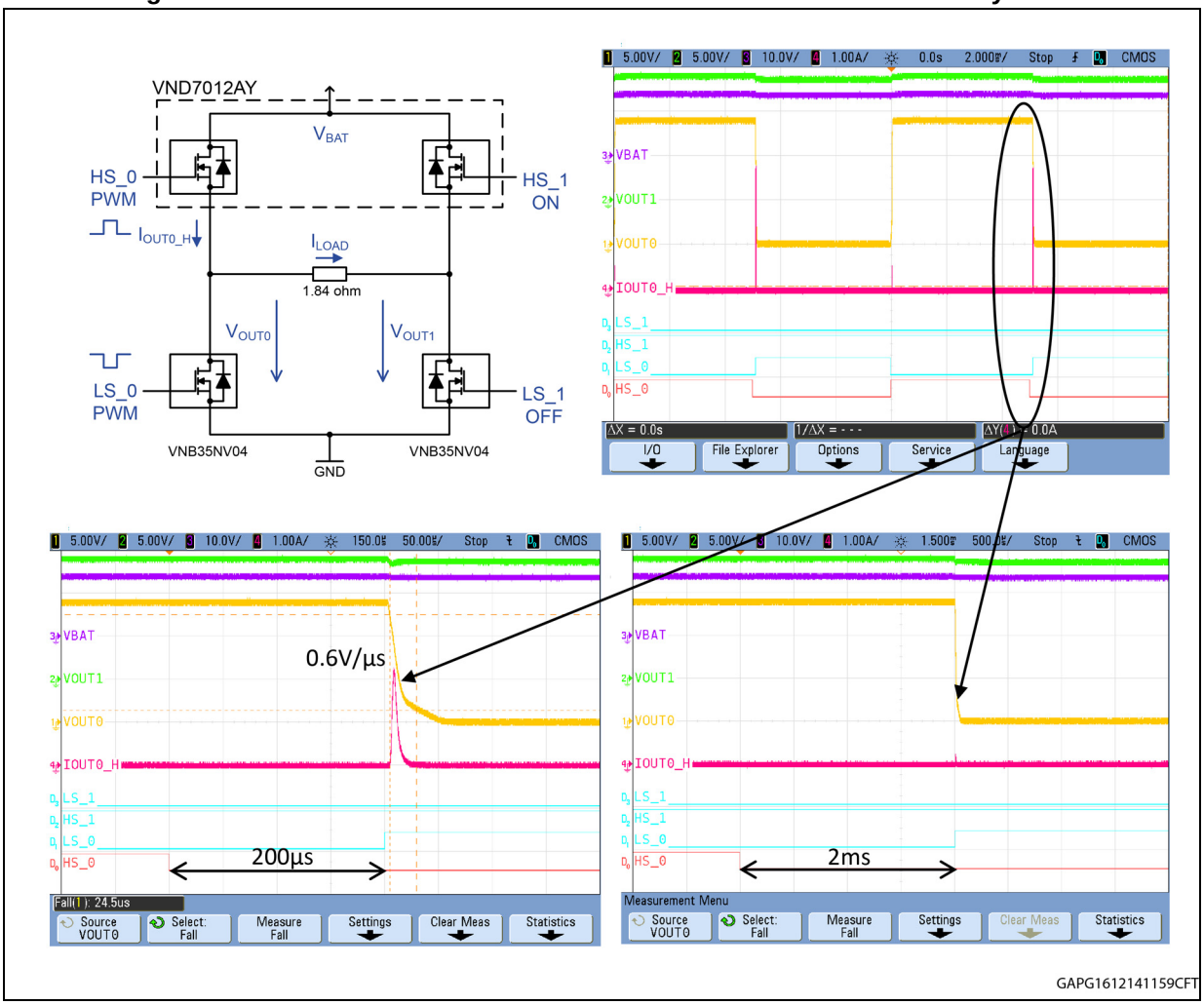
Figure 159. VND7140AJ cross conduction with different OMNIFET delay times



In *Figure 159* same conditions are applied to one VND7140AJ in combination with two VNS3NV04P-E and driving a 13 Ω resistance. At 20 µs in this case, the cross current spike is eliminated. Similar considerations can be applied when the HSD must be switched on after the LSD is switched off, but in this case the switching off times of the OMNIFET II are much shorter than the switching times of the HSD, so in this case the cross conduction shall not take place. In order to avoid the cross conduction due to the mechanism explained before, the low-side drivers have to be driven with delay times, named also “dead times” when for example, in case of a DC motor, it is requested to change direction in the rotation. As general rule for Monolithic M0-7 HSD, minimum dead time to be introduced in the low-side driver is about 250 µs.

In *Figure 160*, the same measurement is shown for one dual channel HSD VND7012AY and two LSD VNB35NV04-E driving a 1.84 Ω resistance. In this case, a significant cross current spike is visible when the delay time between HSD deactivation and LSD activation is below 2 ms. However, the minimum required delay time to avoid any cross condition may be much longer, depending on slew rate of the LSD (can be adjusted by the input pin serial resistor value). Experimental verification shows that with increased slew rate of LSD (from 0.6 V/µs to 1.2 V/µs), the cross conduction spike is visible up to the 5 ms delay time. Therefore, the minimum dead time must be determined case by case. As general rule for hybrid M0-7 HSD, minimum dead time to be introduced in the Low Side Driver is typically 2 ms.

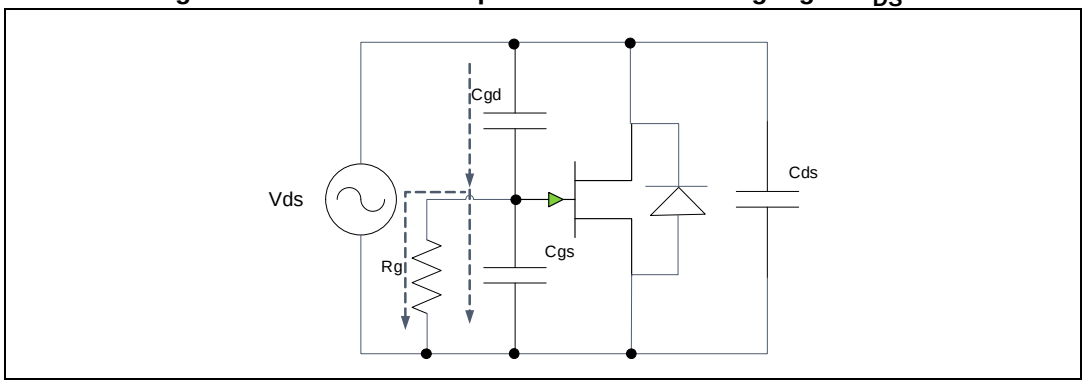
Figure 160. VND7012AY cross conduction with different OMNIFET delay times



Cross conduction due to MOSFETs capacitances

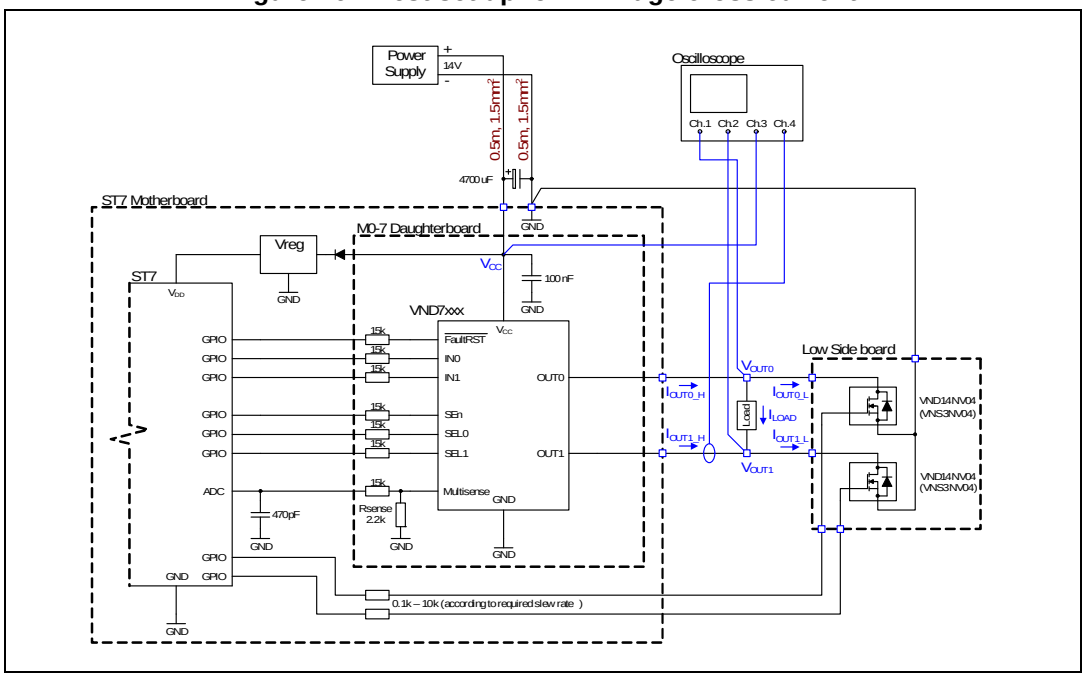
Another event causing cross conduction is related to dynamical effects inside HSD and LSD and precisely to high voltage gradient which can occur across them. Let us consider an H-Bridge in which one of the two MOSFETs of one leg (e.g. HS_1) is completely off and the LSD_1 is switched on. Due to this, the drain-source voltage of HS_1 is submitted to a fast increase (high dV_{ds}/dt) and considering the simplified equivalent model of the MOSFET of the HS_1 (represented in *Figure 162*) this gradient injects a current in the gate-drain capacitance and the gate-source capacitance. The current component flowing on the C_{gs} causes the gate voltage to increase, and if the gate voltage reaches the PowerMOS threshold a consequent turn on of the HS_1 takes place. As this event occurs, the HS_1 and LS_1 conduct for a limited time simultaneously creating a cross conduction event, in this case called also “shoot-through”.

Figure 161. PowerMOS capacitance effect during high dV_{DS}/dt



A practical example follows in which (see *Figure 162*) a test set up with two VND14NV04 (OMNIFET II family) and one VND7020AJ connected in H-Bridge configuration is aimed to reproduce the shoot-through.

Figure 162. Test set up for H-Bridge cross current



Test set up contemplates driving through a microcontroller of HSDs and LSDs. The latter can be set with adjustable switching times via different input series resistors (OMNIFET II). In this way it is possible to measure the sensitivity to shoot-through of the HSD according to decreasing LSD input resistances (this means increasing switching slopes). A 4.5 Ω resistance is supplied by turning HS_0 and LS_1 on and LS_1 is submitted to a 100Hz PWM. So the shoot-through relevant critical element is HS_1 (driven OFF). Result is that in this case the shoot-through is eliminated with slopes below 5 V/µs.

The shoot through mechanism is a limitation factor of PWM frequency of H-Bridge with Standard M0-7 HSDs (frequently used in case of speed control of DC Motors can be up to 30 kHz) because at each period an extra power dissipation, due to the cross current, is summed up to the existing continuous and switching losses of each element. Therefore the frequency of M0-7 HSD should be carefully evaluated. In *Table 33* a summary of the

maximum switching slopes measured on a typical sample which cause no shoot-through in the given test set up for VND7020AJ, VND7040AJ, VND7140AJ and VND7012AY is shown.

Table 33. Maximum switching slopes which do not cause cross current due to MOSFETs capacitances (measurements on a sample on each component)

Device	Max. slew rate of the low-side switch (no parasitic activation of the HSD)
VND7020AJ	5 V/µs (4.5 Ω load resistance)
VND7040AJ	8 V/µs (4.5 Ω load resistance)
VND7140AJ	14 V/µs (13 Ω load resistance)
VND7012AY	13 V/µs (1.84 Ω load resistance)

11.2.3 Usage of MultiSense T_{CHIP} in H-Bridges

The MultiSense chip temperature monitor can be used to aid the thermal management in case critical conditions are forecasted in the application. This features of M0-7 HSDs can be applied to cyclic loads (loads which are statically activated for a certain time and then switched off again for a certain number of times). During prototyping of the application board in order to monitor the temperature of the package for a certain operating cycling profile (for example 20 consecutive activations of a DC motor driving the opening/closure of the car trunk) the application engineer can evaluate if, with given activation cycles, the HSD does not reach a too high temperature.

11.2.4 Freewheeling current of inductive loads

The driving in PWM of inductive loads is a common technique to control the average load power according to application requirement (acting as speed control for example in case of DC motors).

If the PWM signal is applied to the LSD, during its off state the inductive load current re-circulates in the body diode of theM0-7 HSD. If during this phase, the HSD input is driven ON, the current will keep on flowing through the body diode whilst the HSD remains turned off (therefore no active freewheeling is possible). In *Figure 163* an example with VND7140AJ combined with two OMNIFET II LSDs, driving an inductance explains this behavior (the current in HS_0 output is plotted as well).

Figure 163. H-Bridge formed by one VND7140AJ and two OMNIFETs II showing the high-side freewheeling phase.

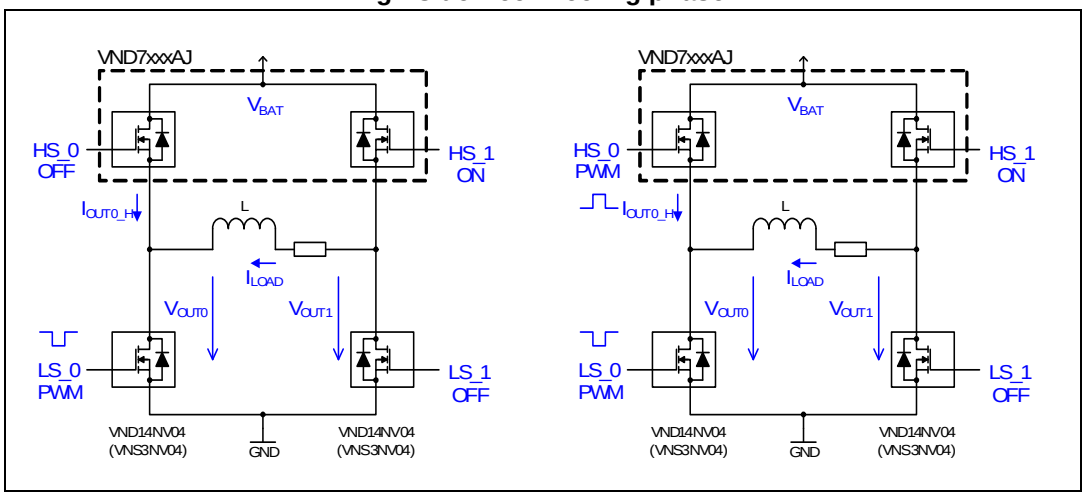
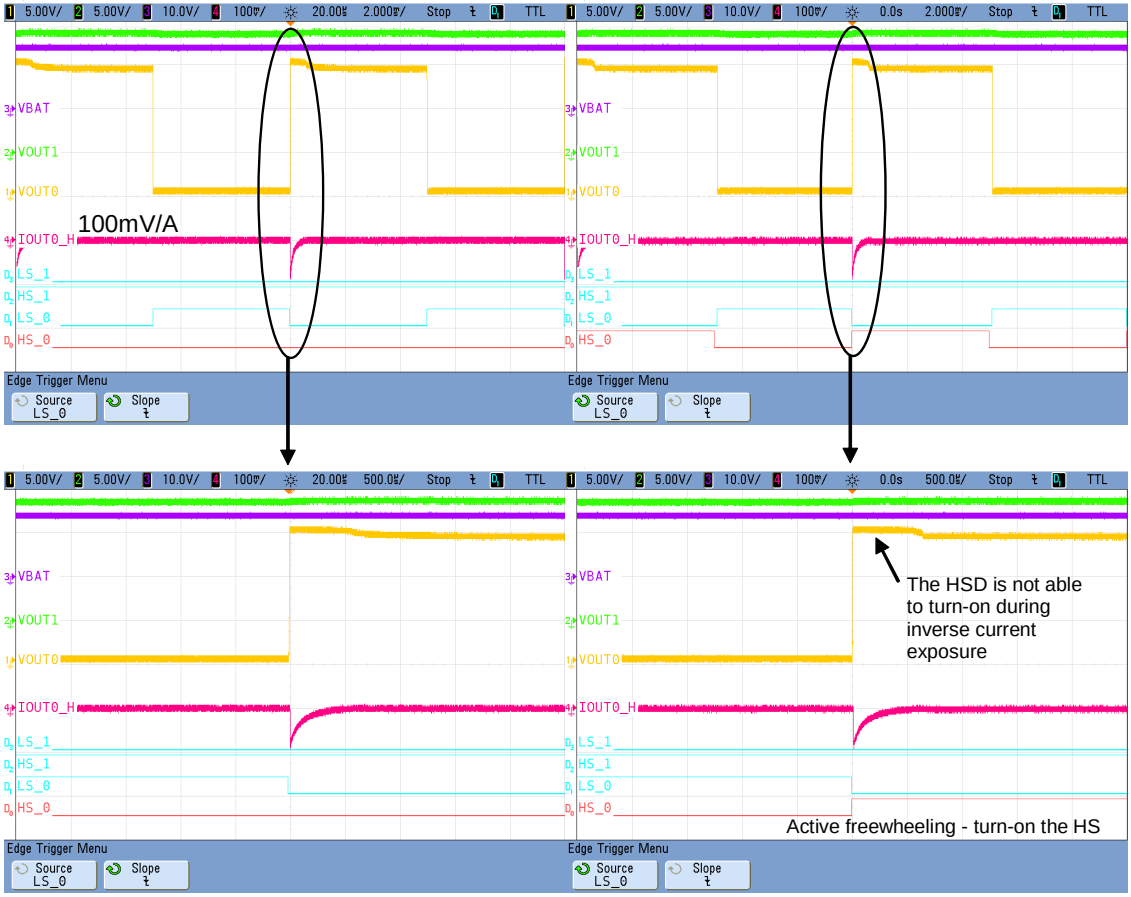
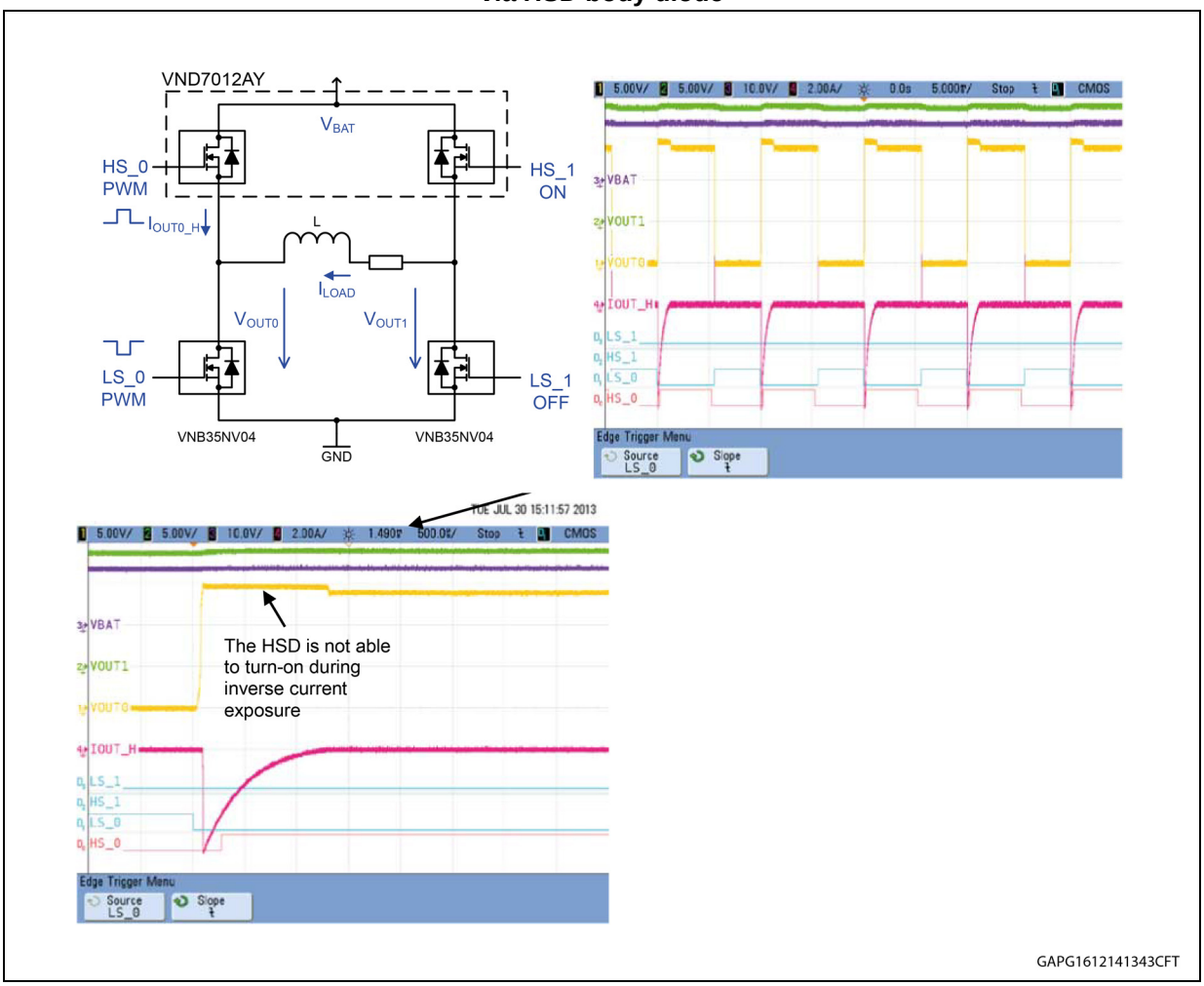


Figure 164. H-Bridge formed by one VND7140AJ and two OMNIFETs II showing the high-side freewheeling phase



Another example with one VND7012AY and two VNB35NV04-E is shown in *Figure 165*. As seen from the measurement, the HSD is not able to turn-on during the freewheeling phase when the demagnetization current flows to the battery line via the body diode (same behavior as in case on monolithic device in previous example). Therefore, no active freewheeling is possible.

Figure 165. H-Bridge formed by one VND7012AY and two OMNIFETs II showing the freewheeling via HSD body diode



Appendix A References

1. CISPR 25 – Vehicles, boats and internal combustion engines – radio disturbance characteristics – limits and methods of measurement for the protection of on-board receivers
2. ISO 7637-2:2004(E) – Road Vehicles – Electrical disturbances from conduction and coupling (second edition)
3. ISO 7637-2:2011(E)– Road Vehicles – Electrical disturbances from conduction and coupling (third edition)
4. LV 124: 2009-10 - Electrical and Electronic components in motor vehicles up to 3.5t; General requirements, test conditions and tests
5. ISO 16750-2:2010(E) – Road Vehicles – Environmental conditions and testing for electrical and electronic equipment
6. ISO 10605 – Road Vehicles – Test methods for electrical disturbances from electrostatic discharge
7. IEC 61000-4-2 – Electromagnetic compatibility (EMC)
8. Double channel high-side driver with MultiSense analog feedback for automotive applications (VND7020AJ, DocID027393)

Revision history

Table 34. Document revision history

Date	Revision	Changes
29-Jul-2015	1	Initial release.