LX7302

5V to 26V Synchronous Step Down DC-DC Controller
Production Datasheet

Description

The LX7302 is a single phase step down DC-DC controller IC designed to drive a high side N-channel MOSFET and a low side N-channel synchronous rectifier. The LX7302 uses a fixed on-time hysteretic control approach for fast transient response. Regulation is accomplished on a pulse-by-pulse basis without the need for an integrating error amplifier. The constant on-time is determined by the product of the ratio of the input to output voltage and the user adjustable switching period.

The output voltage is programmable by an external reference applied to RS1 (in External Reference Mode) or by the VID pins (in self referenced mode). When using the VID pins, there are four possible reference levels programmed by resistors attached to the RS# pins. A droop function is supported to reduce the output voltage under heavy loads minimizing overshoot upon load release.

The LX7302 has protection functions that latch off the power MOSFETs in the event of a fault. Fault conditions are under voltage, over voltage and over temperature. A power good indicator is provided. A cycle-by-cycle current limit will limit the peak current in the lower MOSFET. If the output voltage should drop as a result of sustained current limit, the under voltage detect will trip and shut off the converter. Under voltage lock out (UVLO) keeps the converter off in the event the VCC voltage is too low.

Features

- Integrated High & Low Side Drivers
- Input Voltage Range 5V to 26V
- 200kHz to 1MHz Switching Frequency
- Differential Feedback
- Inductor Current Sensing
- Droop Control
- Enable/Disable
- VID Control or Ext Reference
- Power Saving Mode
- OCP, OVP, UVP, OTP, UVLO

Applications

- Microprocessor Core
- DDR Memory
- Notebook Computers

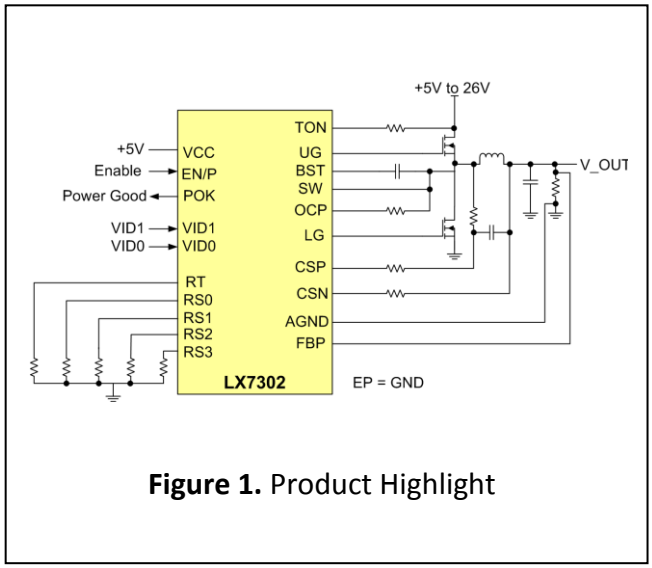

Figure 1. Product Highlight

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Typical Application Diagrams

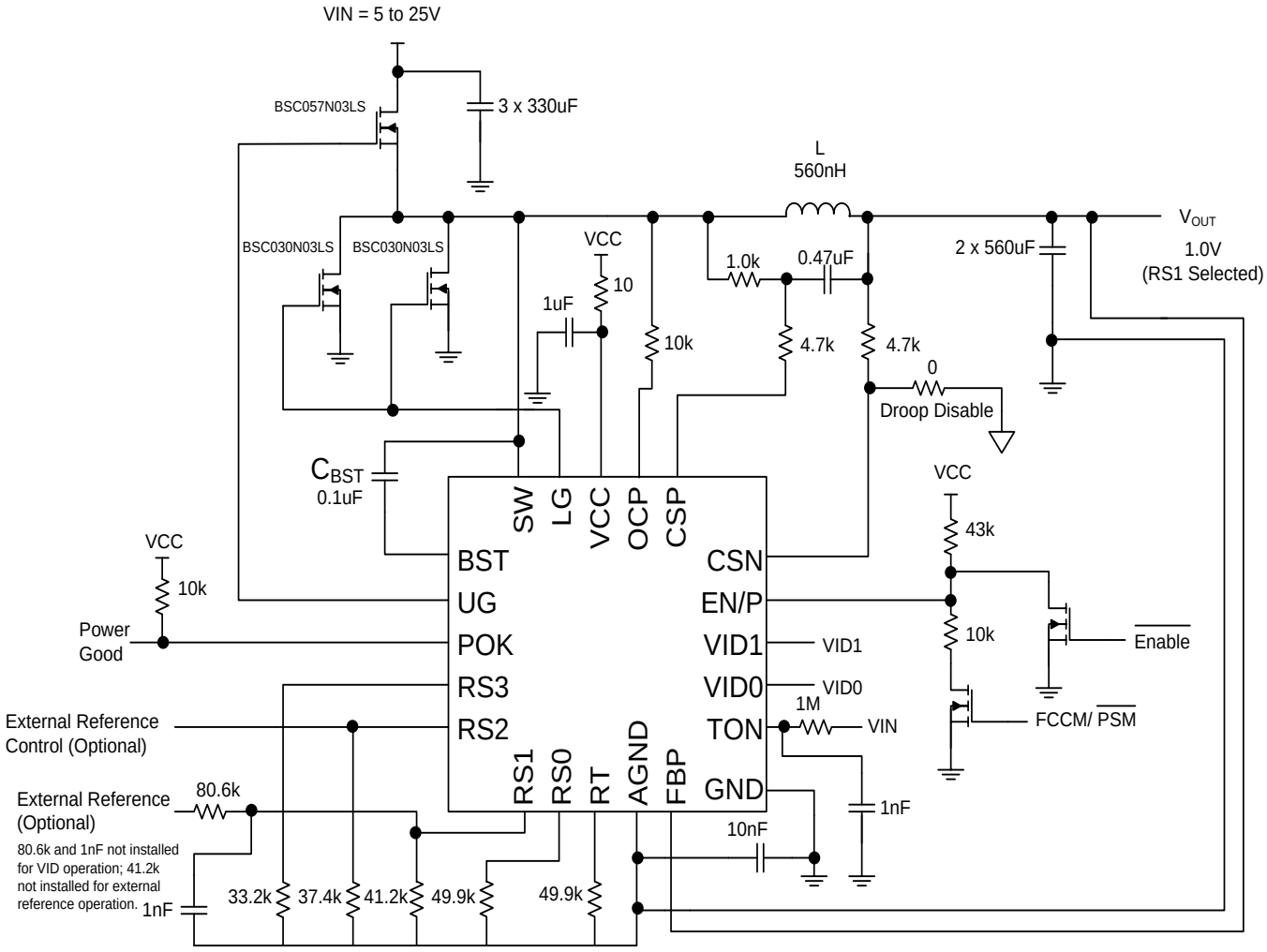
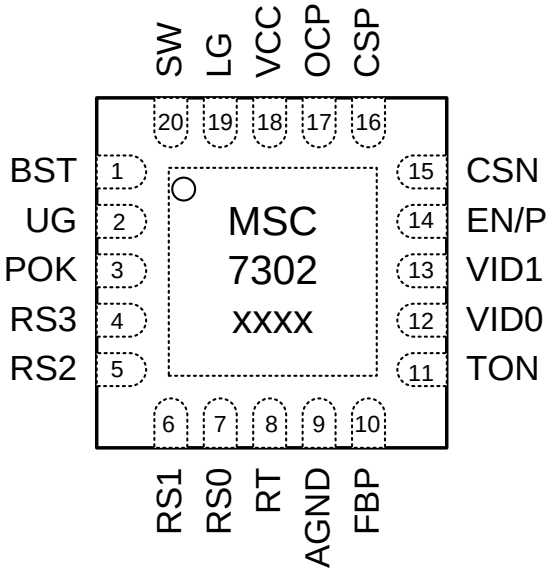


Figure 2: Typical Application Diagram

Pin/Ball Configuration



LQ PACKAGE
(Top View)
Exposed Pad = GND

RoHS / Pb-free 100% Matte Tin Finish
Figure 3: Pinout

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
0°C to 85°C	RoHS compliant, Pb-free	QFN 3x3 20L	LX7302CLQ	Bulk/Tube
			LX7302CLQ-TR	Tape and Reel

Thermal Properties

Thermal Resistance	Min	Typ	Max	Units
θ_{JA}		39		°C/W

Note: The θ_{Jx} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Pin Description

Pin Number	Pin Designator	Description
1	BST	Boost - Power pin - Used for the upper MOSFET driver charge pump. Connect a 100nF capacitor from the BST pin to the SW pin.
2	UG	Upper Gate – Power Pin - Connect to the gate of the High side N-ch MOSFET(s).
3	POK	Power OK – Logic Output Pin – Open drain logic; hi – Z indicates power good.
4	RS3	Resistor 3 – Signal Pin - Reference voltage 3 is programmed using a resistor to ground. The reference current based on the value of RT will flow through the RS3 programming resistor.
5	RS2	Resistor 2 – Signal Pin - Reference voltage 2 is programmed using a resistor to ground. The reference current based on the value of RT will flow through the RS2 programming resistor. This dual use pin is also used to program the reference mode so the IC uses either internal or external reference. Grounding RS2 selects the internal reference mode.
6	RS1	Resistor 1 – Signal Pin - Reference voltage 1 is programmed using a resistor to ground. The reference current based on the value of RT will flow through the RS1 programming resistor. When using an external reference, (with RS2 grounded), the external reference is applied to the RS1 pin.
7	RS0	Resistor 0 – Signal Pin – Reference voltage 0 is programmed using a resistor to ground. The reference current based on the value of RT will flow through the RS0 programming resistor.
8	RT	Resistor Switching Period – Signal Pin – Sets the reference current for the IC. Reference current is V_{RT}/R_{RT}. For normal operation, R_{RT} should be 49.9kΩ to AGND.
9	AGND	Analog Ground Reference – Signal Pin – Connect to ground at the point of regulation.
10	FBP	Feedback Positive – Signal Pin – Connect to the output at the point of regulation.
11	TON	TON programming – Signal pin – This pin is used to control the switch on-time and indirectly controls the switching frequency in the steady state. A resistor connects from this pin to the input voltage for the power converter.
12	VID0	Voltage Programming 0 – Logic Input – Logic input used to select one of 4 possible resistor programmable reference levels. Connect to system ground when not used.

Pin Number	Pin Designator	Description
13	VID1	Voltage Programming 1 – Logic Input - Logic input used to select one of 4 possible resistor programmable reference levels. Connect to system ground when not used.
14	EN/P	Enable/Power Save – Signal Pin - Tri level "logic" pin used to enable the IC and to select either FCCM mode or PSM mode. Low level disables the IC; float this pin to select FCCM; connect to VCC to select PSM.
15	CSN	Current Sense Negative – Signal Pin – This pin is used as the reference pin for the measuring the current in the external inductor for the droop function. Grounding this pin disables the droop function.
16	CSP	Current Sense Positive – Signal Pin – This pin is used to measure current in the external inductor to be used for the droop function. May be left floating when not used (CSN connected to GND).
17	OCP	OCP – Signal Pin - This pin is used to set the switch current limit. A programming resistor connects from this pin to the SW pin.
18	VCC	VCC (Chip Power Supply) – Power Pin – This pin provides power to the IC. It should be decoupled to GND with at least 100nF.
19	LG	Lower Gate – Power Pin – Connect to the gate of the Synchronous rectifier N-ch MOSFET(s).
20	SW	Switch Node – Power Pin - This pin connects to the line or input side of the power inductor and the common point of the high side and low side switches.
EP	GND	Ground – Power Pin – The Exposed Pad of the IC is to be connected to the GND plane. When connecting to the ground plane 12 mil diameter vias spaced on a 47mil matrix should be used to keep inductance low and to provide a path for thermal conduction.

Functional Block Diagram

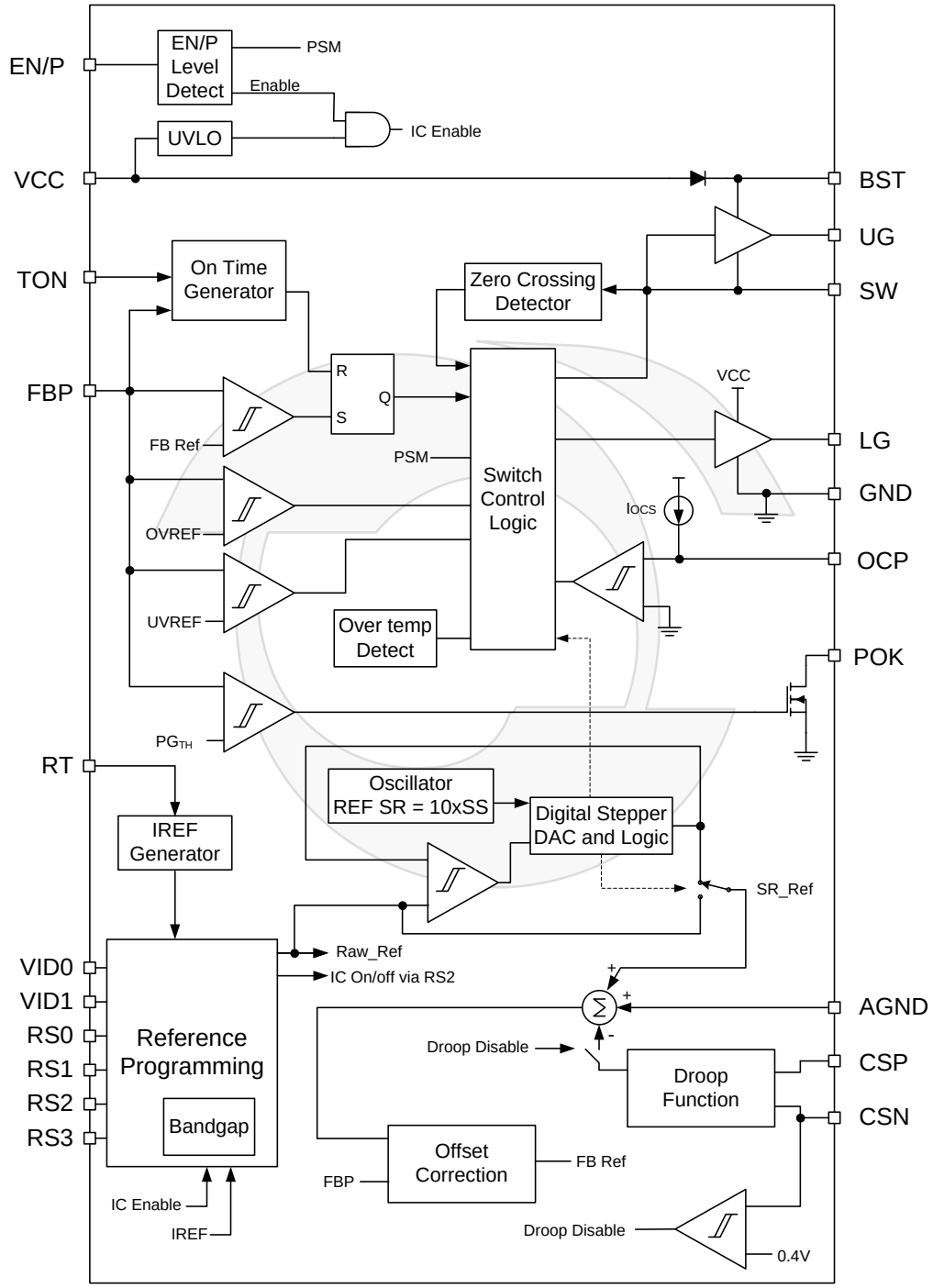


Figure 4: Block Diagram

Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability.

	Min	Max	Units
VCC to GND	-0.3	7	V
BST, UG to SW	-0.3	7	V
SW to GND	-0.3	27	V
LG to GND	-0.3	VCC + 0.3	V
TON, SW to GND (<100ns)	-0.3	40	V
BST to GND (<100ns)	-0.3	47	V
UG to SW (<100ns)	-5	7	V
LG to SW (<100ns)	-5	VCC + 0.3	V
AGND to GND	-0.3	0.3	V
All other pins to GND	-0.3	VCC + 0.3	V
Operating Junction Temperature	0	150	°C
Storage Junction Temperature	-25	150	°C
Package Peak Temp for Solder Reflow (40 seconds maximum exposure)		260	°C

Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

	Min	Max	Units
VCC	4.5	5.5	V
VIN	5	26	V
VOUT	0.6	2.5	V
Ambient Temperature	0	85	°C

Note: Corresponding Absolute Max Junction Temperature is 125°C.

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Electrical Characteristics

The following specifications apply over the operating ambient temperature of $0°C \leq T_A \leq 85°C$ except where otherwise noted with the following test conditions: V_{IN}=12V, VCC =5V, AGND = GND, R_{RT} = 49.9k, V_{CSN} = 0V. Typical parameter refers to T_J = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Operating Current						
I_{ccS}	VCC Input Current at no switching	FB is 110% higher than V(RSET1)		1.8	2.5	mA
I_{ccQ}	VCC Input Current at Switching	Switching, HDrv and LDrv has no capacitive load		3	6	mA
I_{ccSD}	Input Current at Shutdown	EN = GND (including BST current)		70	120	µA
VCC UVLO						
VCC	Under Voltage Lockout	VCC rising	3.9	4.1	4.5	V
		VCC falling	3.7	3.9	4.3	V
VCC	UVLO Hysteresis			200	300	mV
T_{UVLO}	Filter			2		µS
REFIN Shutdown						
V_{RS1}	REFIN Enable Threshold	Measured relative to GND	300	375	450	mV
V_{RSH}	Hysteresis			75	120	mV
FB Accuracy						
V_{FBR}	FB OFFSET in REFIN Mode	When MODE/RSET2 = AGND, RS1 = 1.00V	0.980	1.00	1.010	V
V_{FBV}	FB Voltage in VID MODE	VID0 = X, VID1 = X. $R_{RT} = R_{RS0} = R_{RS1} = R_{RS2} = R_{RS3}$	1.225	1.250	1.275	V
I_{FB}	FB Pin Input Current		-30		0.1	µA
V_{FB}	Feedback Voltage range		0.5		2.2	V
Start up Timing Sequence						
T_D	Start-up Delay	From the application of enable until sampling RS2 for mode detection.		1		ms

Symbol	Parameter	Conditions	Min	Typ	Max	Units
dV_{FB}/dt	Soft-start Rate of Change		703	965	1227	mV/ms
T_{TRP}	Total Start-up Time	TD + TSS; To V_{FB} = 1V			5	ms
T_{DF}	Power On Default Voltage Period	Delay after completion of soft-start until VID programming becomes active	14.6	25.8	37.0	ms
Reference Programming Slew Rate Limit						
dV_{FB}/dt	VID change Slew rate		6.88	9.5	12.12	mV/µs
Adaptive On-time Control						
I_{TON}	TON Operating Current		5	15	25	µA
T_{ONMIN}	Minimum Controllable On-time			35	65	ns
T_{ON}	On-time Control	V_{IN} = 9V, V_{OUT} = 0.75V; R_{TON} = 1M	312	390	468	ns
T_{OFF}	Minimum Off Time	VFB = 90% of V_{REG}	220	430	640	ns
EN/PSM						
$V_{ES/P}$	Off to FCCM Mode	Off-to-FCCM enable (threshold rising)	6.7	10	14.2	%VCC
		FCCM-to-off hysteresis	0.3	1.65	3.0	
	FCCM Mode to PSM mode	FCCM-to-PSM enable (threshold rising)	29.6	33.3	37.1	
		PSM-to-FCCM hysteresis		3	3.5	
	State with EN/PSM Floating	Enabled and in FCCM mode	0.9	1	1.1	V
$I_{ES/P}$	Input Current		-3	0	3	µA
VID Logic						
$V_{VID\#}$	Logic Threshold		0.7	0.9	1.1	V
$V_{VID\#H}$	VID Input Hysteresis		15	40	65	mV
$I_{VID\#}$	Pin Current		-5		5	µA
REFIN						
I_{RS1}	RS1 Current in REFIN MODE		-100		100	nA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Power-good						
V_{PG}	Power-good Transition High Threshold	V_{FB} rising, In percentage of output voltage set-point	87	90	93	$\%V_{REG}$
Z_{POK}	Power GOOD Internal FET Rdson			60		Ω
	Power Good Leakage Current		-5	1	5	µA
Output Driver						
R_{UGH}	High-side Driver Upper Impedance			1.5		Ω
R_{UGL}	High-side Driver Pull Low Impedance			1.5		Ω
R_{LGH}	Low-side Driver Pull High impedance			1.5		Ω
R_{LGL}	Low side driver pull low Impedance			0.5		Ω
t_{DBLH}	Deadband Time from SW Going Low to LDrv Going High			10		ns
t_{DBHL}	Deadband Time from LDrv Going Low to High Side Going High			30		ns
Zero Crossing Comparator						
V_{ZCC}	Built-in Offset			5		mV
T_{ZCC}	Comparator Delay			20		ns
A_{ZCC}	Comparator Overall DC gain			80		DB

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Current Limit Comparator						
V_{OCP}	Current Limit Threshold		-8	0	8	mV
I_{OCP}	OCP Pin Programming Current		11.5	13.5	15.5	µA
T_{ZCC}	Comparator Delay			20		ns
Droop Amplifier (Droop Disable Resistor removed for this section)						
A_{DRP}	Droop Amplifier Gain	ADRP = ΔVFB / Δ (VDRP – VCSN); RCSP = 4.7k; V_{CSN} > 500mV R_{SNS} = 1.2k	1.5	2.75	4	V/V
$V_{CSP-VCSN}$	Droop Amplifier Input Offset	(Positive offset cannot result in positive FB shift); V_{CSN} > 500mV	-7		7	mV
I_{CSN}	Input Current	VCSN = 1V; VCSP = 0.95V	-100	-7.5	+100	nA
I_{CSP}	Input Current	VCSN = 1V; VCSP = 0.95V		-25		nA
V_{CSN}	Droop Enable Threshold	Rising threshold with 2% typical hysteresis	6	8	10	%VCC
FB UV/OV Detect						
V_{FB-UV}	FB UV Threshold	Falling	40	50	60	$\%V_{REG}$
V_{FB-OV}	FB OV Threshold	Rising	100	130	150	$\%V_{REG}$
$T_{FB-FILT}$	Analog Filter			2		µS
T_{FB-DF}	Digital Filter			6		CLK
Soft Shutdown						
R_{SSD}	Soft Shutdown Resistance			30		Ω
BST Pin						
V_{BST}	BST Pin Voltage	With VSW = GND	Vcc-0.5			V
Thermal Shut Down						
T_J	Thermal Shutdown Threshold	TJ rising		160		°C
T_J	Threshold Hysteresis			15		°C

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Typical Performance Curves

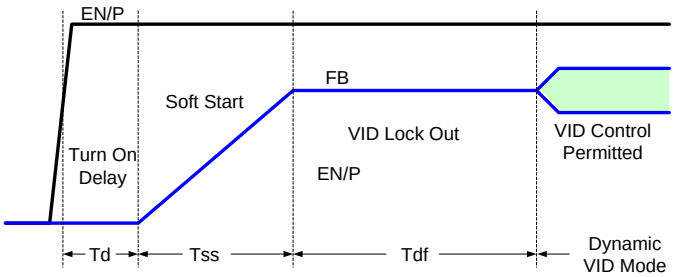


Figure 5. VID Mode Power On Timing

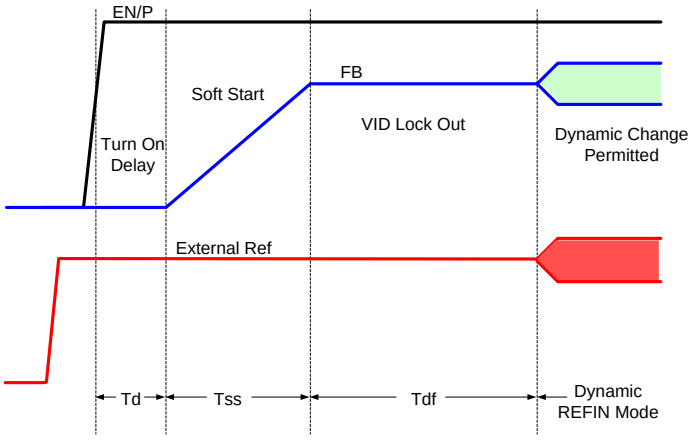


Figure 6. REFIN Power On Timing – Case 1

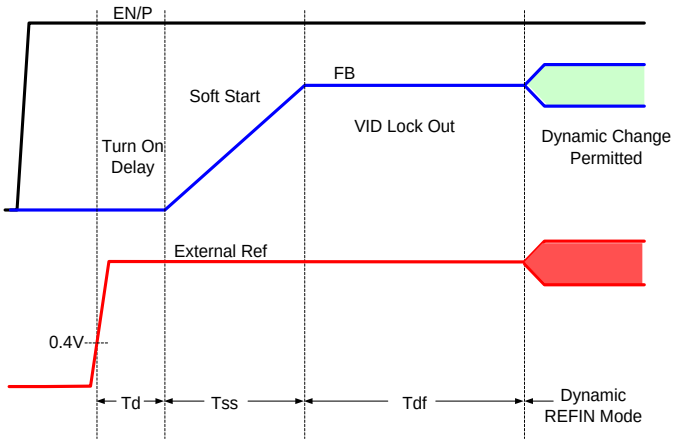


Figure 7. REFIN Power On Timing – Case 2

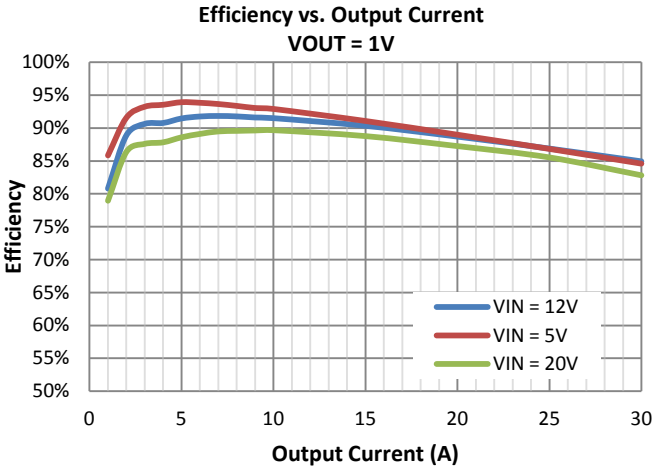


Figure 8. Efficiency

Typical Performance Curves (Continued)

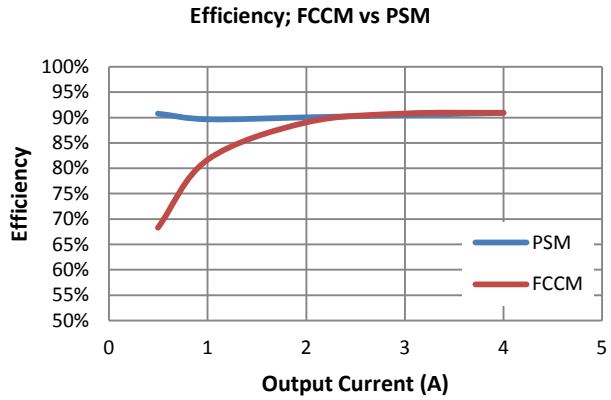


Figure 9. PSM vs. FCCM Efficiency

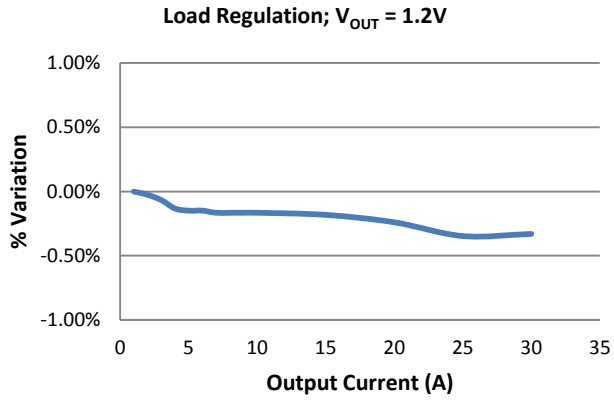


Figure 10. Load Regulation

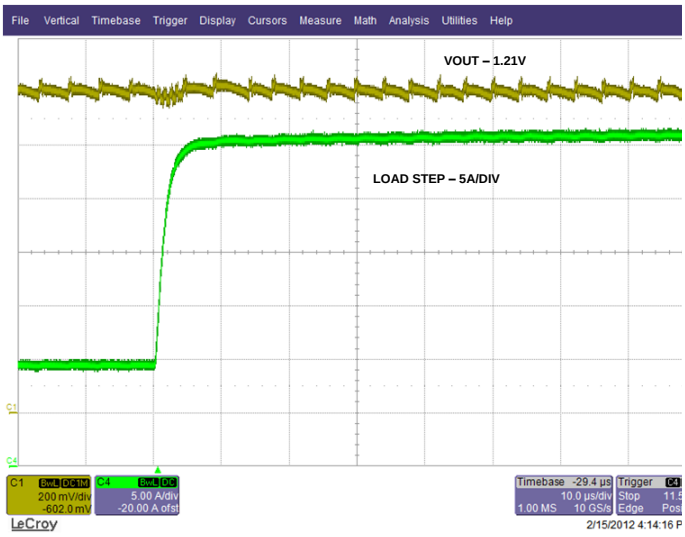


Figure 11. Transient Response – Load Step

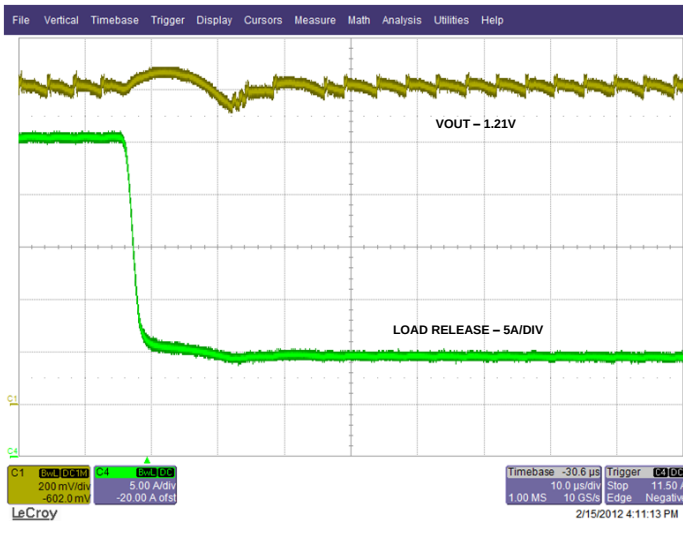


Figure 12. Transient Response – Load Release

Typical Performance Curves (Continued)

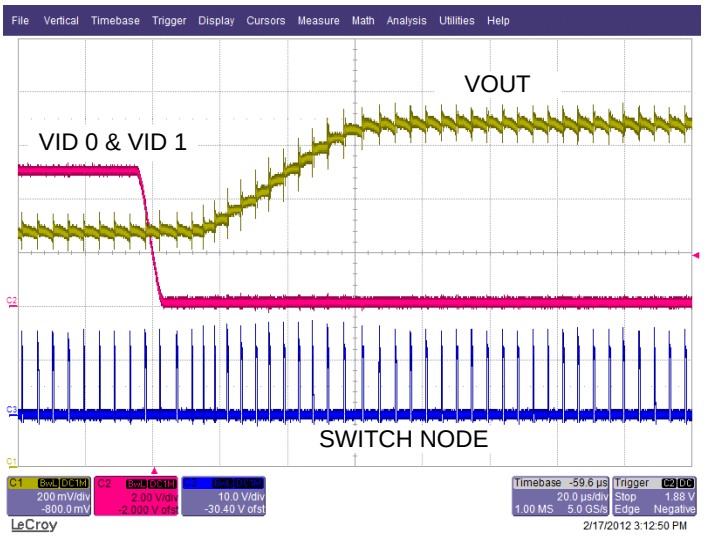


Figure 13. VID Change – Low to High

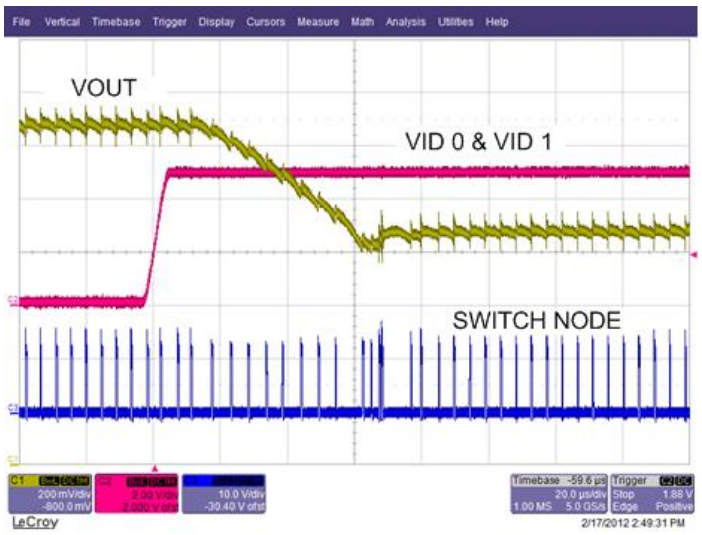


Figure 14. VID Change – High to Low

Operation Theory

DC-DC Switching Step Down Controller

The DC-DC converter is a voltage mode hysteretic controller that uses a calculated constant "on-time" for the upper MOSFET switch. The constant on-time is a function of VIN. The switching frequency is a function of V_{OUT}; the value of the resistor at TON scales the switching frequency and inversely scales the on-time. The lower MOSFET switch or synchronous rectifier turns on after the upper MOSFET switch turns off. The lower MOSFET remains on until the output voltage drops below the feedback threshold or when in PSM, the current in the inductor changes direction and begins to flow into ground. A new turn on cycle for the upper MOSFET begins when the output voltage drops below the feedback threshold.

The hysteretic nature of the DC-DC converter responds very quickly to load transients. There is no error amp integrator to introduce a response delay and there is no loop compensation necessary since the loop responds on a cycle-by-cycle basis. The cycle-by-cycle calculated on-time and frequency results in a nearly constant switching frequency under static loading conditions.

On-Time And Frequency Calculation

An internal one-shot timer turns on the high side driver with an on-time which is proportional to the input supply, V_{IN} and inversely proportional to the output voltage, V_{OUT}.

The equation for the on-time is:

$$T_{ON} = \frac{4.45 \times 10^{-12} \times R_{TON} \times V_{OUT}}{V_{IN} - 0.5V}$$

The equation for the switching frequency is:

$$F_{SW} = \frac{V_{OUT}}{V_{IN} \times T_{ON}}$$

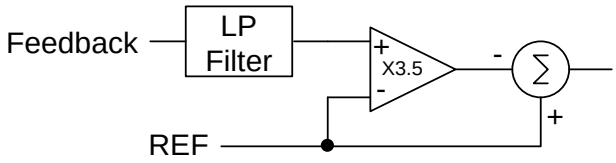
Light Load Operation

There are two possible modes of light load operation that are selectable using the EN/P pin: Forced Continuous Conduction Mode (FCCM) and Power Saving Mode (PSM). Under light loading, the current in the inductor can discharge to zero current and if allowed to, even reverse direction (start flowing into ground). This current flow into ground is unnecessary from a power conversion standpoint and results in some light load efficiency loss. In FCCM, the synchronous rectifier switch is held on for nearly the entire rectification portion of the switching period. Allowing current to flow into ground will effectively discharge the output capacitor which when sensed by the feedback comparator will cause the switching cycle to remain repetitive at the desired switching frequency. In PSM, a zero-crossing detector senses the reverse current flow and turns off the synchronous rectifier. There may be a significant delay time for the output capacitor to discharge when the synchronous rectifier has been shut off; the start of the next switch cycle is delayed until this occurs. In FCCM, the switching frequency remains continuous under light loading, but in PSM, the switching frequency will reduce under light loading.

Operation Theory (Continued)

Ripple Offset Cancellation

The Constant On-Time control triggers the start of a new switch cycle based on the output ripple voltage crossing the feedback threshold. This would result in a positive offset to the output equal to the ripple voltage divided by 2. The ripple correction provides a small offset to the feedback reference to shift the output voltage slightly such that the average feedback voltage is set nearly equal to the reference voltage.



Modes: Internal or External Reference

There are two possible modes of operation for the LX7302 depending on the voltage applied to the RS2 pin when the LX7302 is enabled with UVLO de-asserted. The table below indicates which mode is selected:

Mode Programming

RS2 Pin Voltage	Mode Selected
VRS2 < 0.3V	External Reference (REFIN)
VRS2 > 0.5V	Self Referenced (VID)

When the REFIN mode is selected, the reference voltage for the regulator and protection functions is applied to the RS1 pin. The current source to RS1 is shut off when in the REFIN mode. For REFIN changes, the slew rate must be limited by an external RC filter at the RS1 pin.

When the VID mode is selected, the LX7302 generates its own reference which can be one of four resistor programmable levels (using pins RS0, RS1, RS2 and RS3) selectable using the VID pins (VID0 and VID1). The table below shows the VID programming selections available in VID mode.

VID Mode Reference Programming

VID1	VID0	Reference Level
0	0	$V_{REF0} = (1.25 \times (R_{RS0} + 1000))/50.9 \times 10^3$
0	1	$V_{REF1} = (1.25 \times (R_{RS1} + 1000))/50.9 \times 10^3$
1	0	$V_{REF2} = (1.25 \times (R_{RS2} + 1000))/50.9 \times 10^3$; $V_{REF2} > 0.4V$
1	1	$V_{REF3} = (1.25 \times (R_{RS3} + 1000))/50.9 \times 10^3$

Note: The reference voltages must be programmed such that $R_{RS1} \parallel R_{RS2} > 17.5k$.

When the VID voltage is changed, the slew rate of change is controlled by an internal DAC that is clocked by an internal oscillator. The DAC steps the output in 20mV steps. For VID changes the DAC steps at a clock rate that is 10x faster than the clock rate used for the soft start slew rate. When the DAC has finished stepping, it will apply the RS# input so that there is no quantization error in the final value.

Operation Theory (Continued)

Soft Start

Soft start is implemented using a digital soft-start technique. In this method the reference voltage for the feedback comparator is increased in 20mV steps at a fixed rate until the programmed output voltage level is reached. Soft-start does not begin unless the UVLO start up criterion is met and the device is enabled via the EN/P pin.

The soft-start process in VID mode initially selects the voltage programmed at the RS2 pin as the reference. After the output is up and settled for delay of "Power On Default Voltage Period", the VID selection inputs are then activated.

The soft-start process in REFIN mode will not begin until the external reference (applied to the RS1 pin) is at least 0.4V. The soft-start process ramps at a fixed dV/dt rate such that higher output voltages take longer to reach.

REFIN Mode Shutdown

If operating in REFIN mode and if the voltage on the RS1 pin is brought below 0.4V, the controller will shutdown (switches become off state; driving external MOSFET VGS = 0). The controller will remain latched off unless VCC is cycled above and below the UVLO threshold or the Enable pin is cycled off, then on.

EN/P Enable/Power Save Mode

The EN/P input programming pin is a dual purpose pin; it provides the enable/disable function and also provides the means to select between the PSM mode/FCCM mode. If allowed to float, the enabled and FCCM mode is selected. The table below describes the function:

EN/P	Voltage	IC State	Mode
Low	< 0.3V	Disable	No Output Switching
Mid (float)	>0.5V;<1.6V	Enable	FCCM
High	>1.8V	Enable	PSM

Over Temperature Protection

The LX7302 monitors internal IC temperature and generates an over temperature fault if the temperature threshold is exceeded. If an over temperature fault occurs, the DC-DC converter will stop switching and the UG and LG outputs will turn the external MOSFET switches off. The driven MOSFETs remain turned off until the VCC power or EN/P pin is cycled.

Output Over/Under Voltage Protection

If an over-voltage fault or under-voltage fault occurs on the output as sensed at the feedback input, the DC-DC converter will stop switching and the UG and LG outputs will turn the external MOSFET switches off. A UVP condition must exist for 3 consecutive PWM cycles, but an OVP condition is triggered immediately. The driven MOSFETs remain turned off until the VCC power or EN/P pin is cycled.

Input Under Voltage Lockout Protection

If there is a loss of IC input power (VCC) such that VCC drops below the UVLO threshold, the DC-DC converter will stop switching and the UG and LG outputs will turn the external MOSFET switches off. The driven MOSFETs remain turned off until the VCC power recovers.

Operation Theory (Continued)

Over Current Protection

Over current protection is achieved by sensing current through the low side MOSFET. A bias current equal to ½ IRT flows through an external resistor connected to the OCP pin to the SW pin; this sets the current limit threshold. The current limit is set by the equation:

$$I_{LIMIT} = 0.5 \times I_{RT} \times \frac{R_{OCP}}{R_{DSON}}$$

Where:

I_{LIMIT} = Output inductor ripple current peak; the magnitude of the inductor peak to peak current is determined by the value of T_{ON}, V_{IN}, V_{OUT}, and the output inductor value. The DC current level will be approximately ½ the inductor peak to peak current less than I_{LIMIT}.

SOFT SHUTDOWN

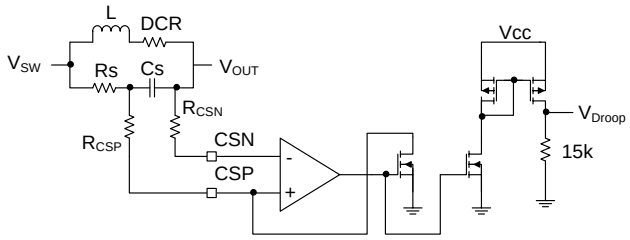
When the output is disabled or shutdown as the result of a fault condition, a soft shutdown switch will close across the output and allow the output capacitor to discharge to GND.

Dynamic Changes of Reference Voltage

When a reference voltage change is detected on REFIN or the VID0 or VID1 pin, the protections for OVP, UVP and OCP are temporarily suspended while the DAC transitions to the new value. Switching mode is forced to FCCM during reference changes. When the digital stepper has transitioned between the initial and final levels, the protection functions are re-enabled, and if active, PSM mode is restored. The DAC does not control the REFIN slew rate, but it does track it and ensures the protection features are disabled and FCCM mode is active when the REFIN is transitioning.

Droop

The output current is monitored by sensing the current flow in the DCR of the inductor. The voltage across the DCR can be measured across the capacitor if the following relationship exists: Cs x Rs = L/DCR



Increasing Rs and Cs will result in lower ripple and a slower response time for the sensed voltage across Cs.

The droop function simulates a resistor in series with the output that provides a voltage drop proportional to the loading current. The droop amplifies the voltage across the sense capacitor with a programmable gain that is determined by the value of RCSP:

$$V_{DROOP} = \frac{V_{CS}}{R_{CSP}} \times 15k\Omega$$

The value of R_{CSN} should be set equal to R_{CSP} to minimize offset error due to op amp bias current. For temperature compensation, a PTC resistor can be used in place of R_{CSP}.

The Droop function can be disabled by grounding the CSN pin.

Power Good

The power good signal is an open drain output that is latched to high impedance when the feedback voltage becomes greater than 90% of the steady state internal reference voltage. POK becomes low impedance to GND if a fault condition occurs.

Application Example

As an example for calculating the component values, assume the following situation:

V_{IN} = 12V_{DC}; F_{SW} = 215kHz; L = 560nH;

L_{DCR} = 1mΩ

Outputs:

VID0 = 1.25V, VID1 = 1.036V, VID2 = 0.943V, VID3 = 0.840V

Switching Frequency

The requirement for on time at a 1.25V output is:

$$T_{ON} = \frac{V_{OUT}}{F_{SW} \times V_{IN}} = \frac{1.25}{215 \times 10^3 \times 12} = 484ns$$

We can then calculate R_{TON}:

$$R_{TON} = \frac{T_{ON} \times (V_{IN} - 0.5V)}{4.45 \times 10^{-12} \times V_{OUT}} =$$

$$\frac{484 \times 10^{-9} \times (12 - 0.5)}{4.45 \times 10^{-12} \times 1.25} = 1.0M\Omega$$

Use a 1M, 1% resistor.

NOTE: In cases with short values for T_{ON}, there can be timing issues created by the additional delays associated with the responsiveness of the MOSFETs, particularly during start up. For these cases it may be necessary to increase T_{ON}.

Droop Calculations (refer to DROOP section above)

Consider a case requiring an additional droop of 50mV when there is 20A of inductor current. With an inductor DCR of 1mΩ, there will be a corresponding DCR voltage drop of 20A x 1mΩ = 20mV. The droop function gain required is 50mV/20mV = 2.5. Using the equations below, the sum of RS and RCSP must equal 6kΩ. It is desirable to keep Rs greater than 400Ω to keep its power dissipation low. The value of RCSP should reflect a standard PTC value. Also keeping RCSP >> Rs helps minimize the offset error by maximizing the Cs voltage. A good compromise is to use RCSP = 4.7kΩ and Rs = 1.3kΩ.

$$\frac{V_{DCR}}{V_{DROOP}} \times 15k\Omega = R_S + R_{CSP}$$

$$= \left(\frac{20}{50} \times 15k\Omega\right) = 6k\Omega = R_S + R_{CSP}$$

For this case:

RCSP = 4.7kΩ for a PTC consider Panasonic ERA-S27J472V.

RCSN = RCSP = 4.7kΩ

Rs = 1.3kΩ

$$Cs = \frac{L}{DCR \times Rs} = \frac{560nH}{1m\Omega \times 1.3k\Omega} = 0.43\mu F$$

Cs = 0.47µF

To temperature compensate for the rise in DCR with temperature it is necessary to match the temperature coefficient of the inductor DCR (winding resistance) to that of RCSP. The copper resistance is about 3500PPM/°C. A PTC like the Panasonic ERA-S27J472V gives a tempco of 2700PPM/°C, which is close to the required tempco in an economical PTC 0805 resistor style.

Application Example (Continued)

VID Calculations

The value of R_{RT} is used to scale the IC reference current which affects the VID programming, slew rate control, and the OCP pin programming current. VID programming voltages are trimmed by the factory with RRT = 49.9kΩ:

$$R_{RS0} = \frac{V_{RS0} \times 50.9 \times 10^3}{1.25} - 1000 = 50.9k\Omega - 1000 = 49.9k\Omega$$

$$R_{RS1} = \frac{V_{RS1} \times 50.9 \times 10^3}{1.25} - 1000 = 42.2k\Omega - 1000 = 41.2k\Omega$$

$$R_{RS2} = \frac{V_{RS2} \times 50.9 \times 10^3}{1.25} - 1000 = 38.4k\Omega - 1000 = 37.4k\Omega$$

$$R_{RS3} = \frac{V_{RS3} \times 50.9 \times 10^3}{1.25} - 1000 = 34.2k\Omega - 1000 = 33.2k\Omega$$

Current Limit Calculations

Over current protection is achieved by sensing current through the low side MOSFET. Therefore, the output DC current limit threshold requires knowledge of the RDS_{ON} value for the lower MOSFET. RDS_{ON} increases with temperature, which must be considered to avoid false current limit detection. Also considered is the inductor ripple current, which will play a role in determining the DC level at the current limit threshold. Inductor ripple current is determined by the value of the output inductor, T_{ON}, V_{IN}, and V_{OUT}.

The exact value of the current limit threshold is difficult to predict due to the number of variables involved; however, a reasonable approximation can be made using worse case conditions.

Using the application schematic as an example, the BSC030N03LS FETs have a specified maximum RDS_{ON} of 4.7mΩ with a 4.5V gate voltage and 25°C junction temperature. Based on the datasheet, the RDS_{ON} increase at 100°C junction is 30%. 4.7mΩ x 1.3 = 6.1mΩ. Two of these FETs in parallel give a combined RDS_{ON} of 3.1mΩ

The inductor is specified as 560nH +/- 20%. Increasing the inductance by 20% gives an inductance value of 672nH.

Based on earlier calculations, T_{ON} = 484ns. V_{IN} and V_{OUT} are 12V and 1.25V, respectively.

For a 30A DC current limit, we set the threshold to 30A plus ½ the inductor peak to peak ripple current:

$$I_{LIMIT} = IDC_{LIMIT} + \left[\frac{(V_{IN} - V_{OUT}) \times T_{ON}}{2 \times L}\right]$$

$$= 30A + \left[\frac{(12 - 1.25) \times 484ns}{2 \times 672nH}\right] = 34A$$

We use 34A to set ILIMIT:

$$R_{OCP} = \frac{I_{LIMIT}}{0.5 \times I_{RT}} \times RDS_{ON} =$$

$$\frac{34}{0.5 \times 24 \times 10^{-6}} \times 0.003\Omega = 8.5k\Omega$$

Where:

I_{RT} = 1.25V/50.9kΩ

Application Example (Continued)

The above example is using one voltage operating point only; In an application where a range of input/output voltages are required, the V_{IN}, V_{OUT}, and TON values that generates the smallest ripple current (highest I_{LIMIT}) would be used in the calculations. Note that the above method takes into account worse case conditions to avoid false current limit detection; under typical conditions the actual current limit will be much higher.

Output Inductor Selection

The output inductor is selected based on the desired amount of ripple current, generally determined as a percentage of maximum output current. The Ripple Factor, or percentage amount, is typically set for 30% to 50% of the maximum output current.
For a Ripple Factor of 30%, and a load current of 30A, the inductor is selected:

$$L_{out} = \frac{T_{ON} \times (V_{IN} - V_{OUT})}{k * I_{OUT}} = \frac{484ns \times (12 - 1.25)}{0.3 * 30} = 578nH$$

Where:
k = 30% ripple factor

Input Capacitor Selection

The input capacitor is selected for minimum ripple voltage and ripple current capability at minimum input voltage. With a minimum input voltage of 10V, calculate the capacitor ripple current as follows:

$$I_{INRIPPLE} = I_{OUT} \times \sqrt{D \times (1 - D)} = 30 \times \sqrt{0.147 \times 0.853} = 10.6A_{RMS}$$

Where:

$$D = \text{Duty Cycle} = \frac{V_{OUT}}{\eta \times V_{IN}} = \frac{1.25}{0.85 \times 10} = 0.147$$

$$\eta = \text{Efficiency}$$

The input capacitor selected is based on the desired minimum input ripple voltage seen by the converter. 500mV or less ripple is recommended. Input ripple voltage magnitude is dependent on both the input capacitor's capacitance and ESR values. For the most part the ESR will dominate, as long as the capacitance value is large enough. To determine the minimum input capacitance and maximum ESR required at V_{IN} = 10V, a good rule of thumb would be to establish minimum capacitance and increase this value by 10x :

$$C_{MIN} = \frac{(I_{OUTDC} - I_{INDC}) \times T_{ON}}{V_{RIPPLE}} \times 10 = \frac{(30 - 4.17) \times 586ns}{0.5} \times 10 = 310\mu F$$

Where:

$$I_{INDC} \approx D \times I_{OUTDC} \approx 0.139 \times 30 \approx 4.17A$$

$$T_{ON}(10V) = \frac{12V - 0.5V}{10V - 0.5V} \times T_{ON}(12V) = \frac{11.5}{9.5} \times 484ns = 586ns$$

Application Example (Continued)

330µF is the closest standard value that will satisfy the above equation.

Next the maximum ESR is determined. For margin decrease the desired ripple voltage by 10%:

$$C_{ESR} = \frac{V_{RIPPLE} \times 0.9}{(I_{OUTDC} - I_{INDC})} = \frac{0.5 \times 0.9}{(30 - 4.17)} = 17m\Omega$$

Output MOSFET Selection

The LX7302 gate drivers output a maximum voltage of VCC; therefore logic-level FETs should be used.

When selecting the output MOSFETs, the power dissipation should be considered. For the Synchronous FET, power dissipation is mostly in conduction loss, so the MOSFET's RDSON rating will be of primary concern.

To determine the power dissipation in the synchronous FET:

$$P_{SYNC} = (1-D) \times I_{OUTDC}{}^2 \times RDS_{ON}$$

Use the maximum specified RDSON of the MOSFET at 100°C. This number can be derived from the manufacturer's graph of RDSON vs. Temperature.

For the Control FET, both switching losses and conduction losses must be considered. Usually a trade-off between low gate charge and low RDSON is considered. Many manufacturers provide a Figure Of Merit (FOM) on their datasheets, which is simply the product of RDS_{ON} and gate charge. Consider the lowest FOM when choosing the Control MOSFET.

To determine switching losses, the Control FET's on and off switching times must first be determined. Switching times are dependent on the LX7302's drive current available during the MOSFET on and off switching period. Each period is divided into two distinct time periods based on gate charge values, QGD and QGS2. QGS2 is the Gate to Source charge that occurs between the MOSFET gate threshold voltage (VTH) and the Miller Plateau voltage. Note that QGS2 is not to be confused with QGS. Most manufacturers do not specify QGS2 or Miller Plateau voltage; however they can be derived easily from the manufacturer's graph of gate voltage vs. charge. See Figure 3 for details.

Once the values for QGS2, Miller Plateau Voltage, and QGD are known, the two switching periods are calculated and then added together for the total switching period:

$$T_{RISE} = \frac{Q_{GS2} \times (R_{GD} + R_G)}{V_{CC} - \left[\frac{V_{TH} + V_{Plateau}}{2}\right]} + \frac{Q_{GD} \times (R_{GD} + R_G)}{V_{CC} - V_{PLATEAU}}$$

$$T_{FALL} = \frac{Q_{GS2} \times (R_{GD} + R_G)}{\left[\frac{V_{TH} + V_{Plateau}}{2}\right]} + \frac{Q_{GD} \times (R_{GD} + R_G)}{V_{PLATEAU}}$$

Where:

V_{TH} = MOSFET Threshold Voltage

$V_{Plateau}$ = MOSFET Miller Plateau Voltage

R_{GD} = LX7302 Drive On Resistance

R_G = MOSFET Gate Resistance

Application Example (Continued)

Switching losses are calculated:

$$P_{SW} = V_{IN} \times I_{OUTDC} \times F_{SW} \times \left(\frac{T_{RISE} + T_{FALL}}{2} \right)$$

To determine the conduction losses, use the following formula:

$$P_{COND} = D \times I_{OUTDC}^{2} \times RDS_{ON}$$

Use the maximum specified RDS_{ON} of the MOSFET at 100°C. This number can be derived from the manufacturer's graph of RDS_{ON} vs. Temperature.

The total Control MOSFET's power dissipation is the sum of the switching and conduction losses:

$$P_{CONTROL} = P_{COND} + P_{SW}$$

As an example, assume the following:
VIN = 12V
VOUT = 1V
Duty Cycle = 0.098
F_{SW} = 215kHz
Continuous Output Load = 25A

Using the BSC057N03LS FET as a Control FET example, we use the following datasheet specifications:

RDS_{ON} (100°C) = 11mΩ
V_{TH} = 1.7V
$V_{Plateau}$ = 3.2V
Q_{GS2} = 3.7nC
Q_{GD} = 3.7nC
R_G = 1.3Ω
R_{GD} = 1.5Ω

Using the BSC030N03LS FET as a Synchronous FET example, we use the following datasheet specification:

RDS_{ON} (100°C) = 6mΩ

First determine the power dissipation in the Synchronous FET. For this application we use 2 MOSFETs in parallel for a combined RDS_{ON} of 3.1mΩ:

$$P_{SYNC} = (1-D) \times I_{OUTDC}^{2} \times RDS_{ON} =$$
$$(1-0.098) \times 25^{2} \times 3m\Omega$$
$$= 1.69W$$

The power dissipation is spread across two FETs, which equals 0.85W each FET.

Application Example

Next determine the losses in the Control FET. Using the example values, determine the switching losses. First determine the switching time period:

$$T_{RISE} = \frac{Q_{GS2} \times (R_{GD} + R_G)}{V_{CC} - \left[\frac{V_{TH} + V_{Plateau}}{2}\right]} + \frac{Q_{GD} \times (R_{GD} + R_G)}{V_{CC} - V_{PLATEAU}}$$

$$= \frac{3.7n \times (1.5 + 1.3)}{5.0 - \left[\frac{1.7 + 3.2}{2}\right]} + \frac{3.7n \times (1.5 + 1.3)}{5.0 - 3.2} = 9.8ns$$

$$T_{FALL} = \frac{Q_{GS2} \times (R_{GD} + R_G)}{\left[\frac{V_{TH} + V_{Plateau}}{2}\right]} + \frac{Q_{GD} \times (R_{GD} + R_G)}{V_{PLATEAU}}$$

$$= \frac{3.7n \times (1.5 + 1.3)}{\left[\frac{1.7 + 3.2}{2}\right]} + \frac{3.7n \times (1.5 + 1.3)}{3.2} = 7.5ns$$

Switching loss is determined:

$$P_{SW} = V_{IN} \times I_{OUTDC} \times F_{SW} \times \frac{T_{RISE} + T_{FALL}}{2} =$$

$$12 \times 25 \times 215kHz \times 8.6ns = 555mW$$

Next, determine conduction loss:

$$P_{COND} = D \times {I_{OUTDC}}^2 \times RDS_{ON} =$$

$$0.098 \times 25^2 \times 11m\Omega = 674mW$$

The total losses are the sum of the switching loss and conduction loss:

$$P_{CONTROL} = P_{COND} + P_{SW} = 0.56 + 0.67 = 1.23W$$

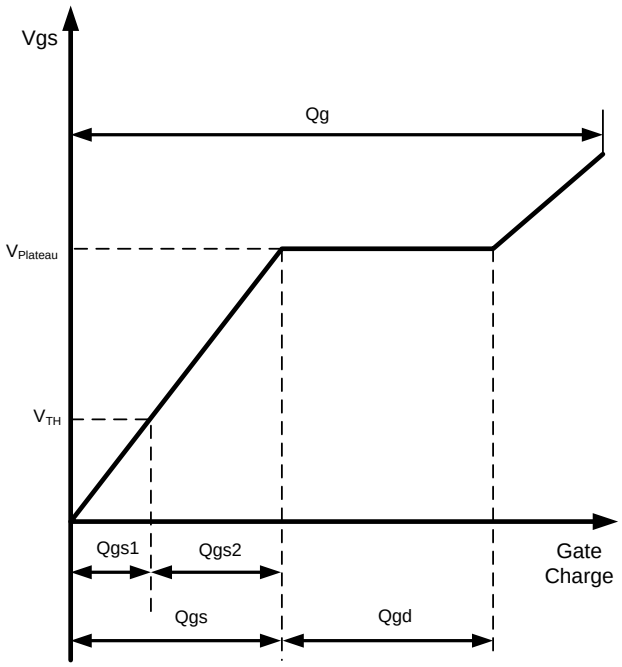
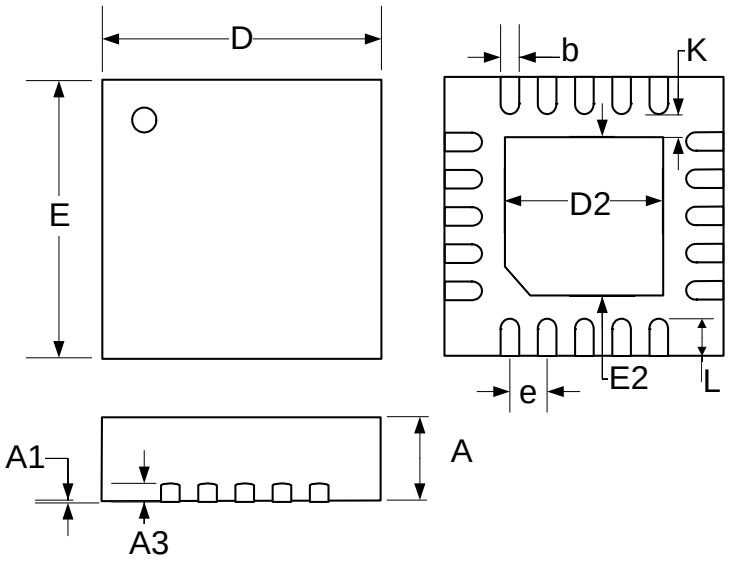


Figure 15. Gate Charge Definitions

Package Dimensions

QFN 3x3mm 20L Exposed Pad



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.80	0.027	0.031
A1	0	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	3.00 BSC		0.118 BSC	
D2	1.55	1.80	0.061	0.071
e	0.40 BSC		0.016 BSC	
E	3.00 BSC		0.118 BSC	
E2	1.55	1.80	0.061	0.071
K	0.2	-	0.008	-
L	0.20	0.50	0.012	0.020

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006”) on any side. Lead dimension shall not include solder coverage.