

Programmable Dual Output Linear Regulator

General Description

The RT9032 is a dual channels, low noise and low dropout voltage regulator sourcing up to 300mA at each channel. The output voltage range is from 1.1V to 3.3V by operating voltage range from 2.5V to 5.5V.

The output voltages of the RT9032 can be programmed by setting the voltage of P1 and P2. There are 9 different voltage settings in one chip. User can choose output voltages easily by setting P1, P2 to VDD, GND or floating.

The RT9032 offers 3% accuracy, low dropout (330mV @300mA) and extremely low ground current, only 32µA per LDO. The shutdown current is near to zero current which is suitable for battery-powered device. Other features include current limiting, over temperature protection and output short circuit protection.

The RT9032 can operate stable with very small ceramic output capacitors, reducing required board space and component cost. The RT9032 is available in WDFN-8L 2x2 and WQFN-8L 1.6x1.6 (COL) packages.

Ordering Information

| | | | |
|--------|--------------------------------------|----|----|
| RT9032 | □ | □ | □ |
| | └─ | └─ | └─ |
| | Package Type | | |
| | QW : WDFN-8L 2x2 (W-Type) | | |
| | QWA : WQFN-8L 1.6x1.6 (COL) (W-Type) | | |
| | Lead Plating System | | |
| | G : Green (Halogen Free and Pb Free) | | |
| | Output Voltage | | |
| | A : Combination A | | |
| | B : Combination B | | |
| | C : Combination C | | |
| | D : Combination D | | |
| | J : Combination J | | |

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

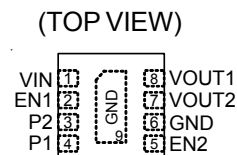
Features

- Wide Operating Voltage Ranges : 2.5V to 5.5V
- Dual LDO Output
- Pin Programmable Output Voltage
- Low-Noise for RF Application
- No Noise Bypass Capacitor Required
- Fast Response in Line/Load Transient
- Low Quiescent Current of 32µA/LDO
- 3% High Output Accuracy
- Current Limiting Protection
- Thermal Shutdown Protection
- Short Circuit Protection
- Tiny WDFN-8L 2x2 and WQFN-8L 1.6x1.6 (COL) Packages
- RoHS Compliant and Halogen Free

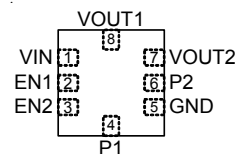
Applications

- Mobile Phone
- Smart Hand-Held Devices
- Digital Still Camera
- Battery-Powered Equipments
- PCMCIA Cards

Pin Configurations



WDFN-8L 2x2



WQFN-8L 1.6x1.6 (COL)

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Typical Application Circuit

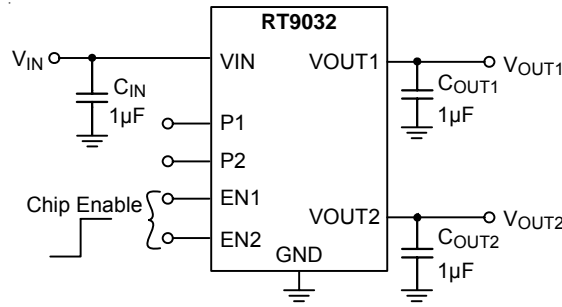


Table for Programmable Output Voltage Setting

Combination A (RT9032A)

| P1 State | P2 State | VOUT1 | VOUT2 |
|----------|----------|-------|-------|
| L | L | 1.5V | 2.8V |
| L | H | 1.8V | 2.9V |
| L | Open | 1.8V | 2.8V |
| H | L | 1.8V | 2.7V |
| H | H | 1.8V | 2.6V |
| H | Open | 2.7V | 2.8V |
| Open | L | 2.8V | 2.8V |
| Open | H | 2.9V | 2.9V |
| Open | Open | 2.8V | 3.3V |

Combination C (RT9032C)

| P1 State | P2 State | VOUT1 | VOUT2 |
|----------|----------|-------|-------|
| L | L | 1.8V | 2.8V |
| L | H | 1.8V | 2.85V |
| L | Open | 1.8V | 3V |
| H | L | 1.85V | 2.85V |
| H | H | 2.6V | 2.7V |
| H | Open | 2.6V | 3.3V |
| Open | L | 2.85V | 3.3V |
| Open | H | 3V | 3.3V |
| Open | Open | 3.3V | 3.3V |

Combination B (RT9032B)

| P1 State | P2 State | VOUT1 | VOUT2 |
|----------|----------|-------|-------|
| L | L | 1.2V | 2.8V |
| L | H | 1.5V | 1.8V |
| L | Open | 1.5V | 2.8V |
| H | L | 1.8V | 2.6V |
| H | H | 1.8V | 2.8V |
| H | Open | 2.8V | 2.8V |
| Open | L | 2.8V | 3.3V |
| Open | H | 3V | 3.3V |
| Open | Open | 3.3V | 3.3V |

Combination D (RT9032D)

| P1 State | P2 State | VOUT1 | VOUT2 |
|----------|----------|-------|-------|
| L | L | 1.8V | 2.9V |
| L | H | 2.6V | 2.8V |
| L | Open | 1.8V | 2.8V |
| H | L | 2.9V | 2.9V |
| H | H | 2.8V | 3.3V |
| H | Open | 2.8V | 2.8V |
| Open | L | 1.8V | 2.6V |
| Open | H | 1.8V | 2.7V |
| Open | Open | 1.5V | 2.8V |

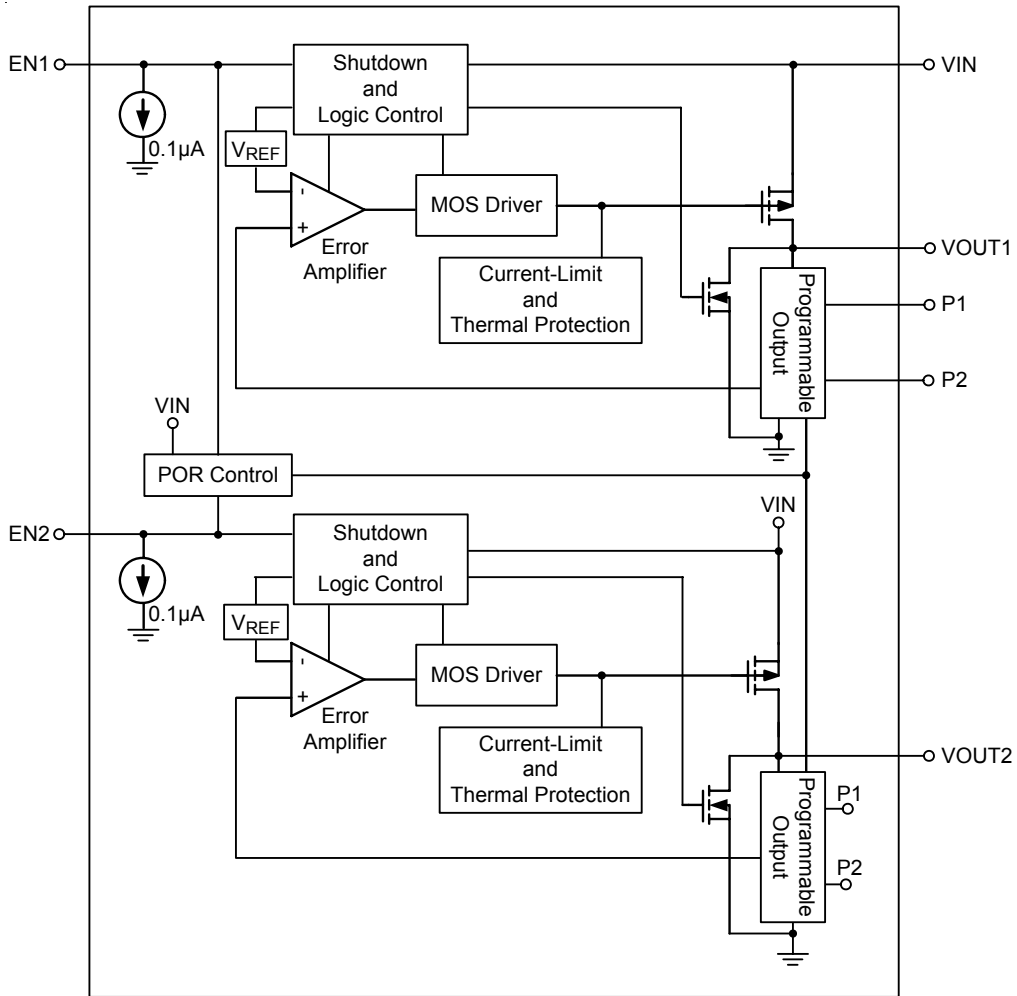
Combination J (RT9032J)

| P1 State | P2 State | VOUT1 | VOUT2 |
|----------|----------|-------|-------|
| L | L | 3.3V | 3.3V |
| L | H | 1.1V | 3.3V |
| L | Open | 1.2V | 2.5V |
| H | L | 1.8V | 3.3V |
| H | H | 1.1V | 1.8V |
| H | Open | 1.1V | 2.5V |
| Open | L | 1.2V | 1.8V |
| Open | H | 1.2V | 3.3V |
| Open | Open | 1.8V | 2.5V |

Functional Pin Description

| Pin Number | | Pin Name | Pin Function |
|-----------------------|--------------------|----------|--|
| WDFN 2x2 | WQFN 1.6x1.6 (COL) | | |
| 1 | 1 | VIN | Supply Input. |
| 2 | 2 | EN1 | Channel 1 Enable Control.(Active High) |
| 3 | 6 | P2 | Programming Input 2. The state of P2 selects one of nine output voltage options. |
| 4 | 4 | P1 | Programming Input 1. The state of P1 selects one of nine output voltage options. |
| 5 | 3 | EN2 | Channel 2 Enable Control.(Active High) |
| 6, 9 (Exposed Pad) | 5 | GND | Common Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |
| 7 | 7 | VOUT2 | Channel 2 Output Voltage. |
| 8 | 8 | VOUT1 | Channel 1 Output Voltage. |

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage (VIN) ----- 6.5V
- I/O Pin Voltage (EN1, EN2, P1, P2, VOUT1, VOUT2) ----- 6.5V
- Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$
 - WDFN-8L 2x2 ----- 0.606W
 - WQFN-8L 1.6x1.6 (COL) ----- 0.571W
- Package Thermal Resistance (Note 2)
 - WDFN-8L 2x2, θ_{JA} ----- 165°C/W
 - WDFN-8L 2x2, θ_{JC} ----- 20°C/W
 - WQFN-8L 1.6x1.6 (COL), θ_{JA} ----- 175°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 - HBM (Human Body Model) ----- 2kV
 - MM (Machine Model) ----- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ----- 2.5V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics

($V_{IN} = V_{OUTX} + 0.7\text{V}$, $V_{ENX} = V_{IN}$, $C_{IN} = C_{OUT1} = C_{OUT2} = 1\mu\text{F}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|------------------------------|-------------------|--|-----|-----|-----|---------------|
| Quiescent Current (Note5) | I_Q | $V_{EN} > 1.5\text{V}$, | -- | 65 | 80 | μA |
| Shutdown Current | I_{SHDN} | $V_{EN} < 0.4\text{V}$ | -- | -- | 1 | μA |
| Output (VOUT1, VOUT2) | | | | | | |
| Output Voltage Range | V_{OUT} | | 1.1 | -- | 3.3 | V |
| Dropout Voltage (Note 6) | V_{DROP} | $I_{OUT} = 300\text{mA}$ | -- | 330 | 500 | mV |
| Output Accuracy | ΔV | $I_{OUT} = 1\text{mA}$ | -3 | -- | +3 | % |
| Line Regulation | ΔV_{LINE} | $V_{IN} = 2.5\text{V to } 5.5\text{V}$ | -- | -- | 0.2 | %/V |
| Load Regulation | ΔV_{LOAD} | $1\text{mA} < I_{OUT} < 300\text{mA}$ | -- | -- | 0.6 | % |
| Power Supply Rejection Rate | PSRR | $f = 100\text{Hz}$, $I_{LOAD} = 10\text{mA}$ | -- | 65 | -- | dB |
| | | $f = 1\text{kHz}$, $I_{LOAD} = 10\text{mA}$ | -- | 60 | -- | |
| | | $f = 10\text{kHz}$, $I_{LOAD} = 10\text{mA}$ | -- | 50 | -- | |
| | | $f = 100\text{Hz}$, $I_{LOAD} = 150\text{mA}$ | -- | 65 | -- | dB |
| | | $f = 1\text{kHz}$, $I_{LOAD} = 150\text{mA}$ | -- | 50 | -- | |
| | | $f = 10\text{kHz}$, $I_{LOAD} = 150\text{mA}$ | -- | 50 | -- | |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit | |
|--|-----------------|---|--|------|-----|----------|----------|
| Output Voltage Discharge Resistance in Shutdown | | $V_{IN} = 5V, EN1 = EN2 = GND$ | -- | 20 | -- | Ω | |
| Output Voltage Temperature Coefficient | | | -- | 100 | -- | ppm/°C | |
| Enable Pin Input (EN1, EN2) | | | | | | | |
| EN Threshold Voltage | Logic-High | V_{IH} | $V_{IN} = 2.5V \text{ to } 5.5V, \text{ Power On}$ | 1.5 | -- | -- | V |
| | Logic-Low | V_{IL} | $V_{IN} = 2.5V \text{ to } 5.5V, \text{ Shutdown}$ | -- | -- | 0.4 | |
| Tri-State Input (P1, P2) | | | | | | | |
| P1/P2 Termination Resistance from input to VDD or GND for setting Hi, Lo, Open States (Note 7) | | $V_{IN} = 2.5V \text{ to } 5.5V$ | Hi, Lo State | -- | -- | 1k | Ω |
| | | $V_{IN} = 2.5V \text{ to } 5.5V$ | Open State | 100k | -- | -- | |
| Decision Time | TD | Open pin with input loading $\leq 50pF$ (Including PAD & PCB trace) | | -- | -- | 20 | μs |
| Protection | | | | | | | |
| Current Limit | I_{LIM} | $R_{LOAD} = 1 \Omega$ | | 330 | 430 | 600 | mA |
| Thermal Shutdown Temperature | T_{SD} | | | -- | 170 | -- | °C |
| Thermal Shutdown Hysteresis | ΔT_{SD} | | | -- | 30 | -- | |

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at $T_A = 25^\circ C$ on a low effective thermal conductivity single-layer test board per JEDEC 51-3. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

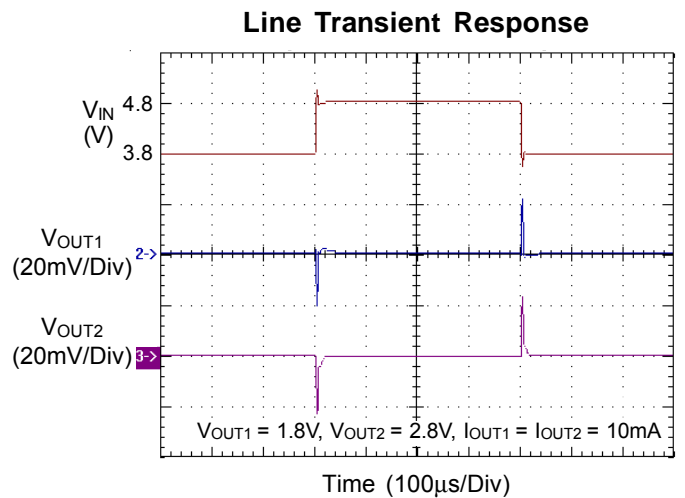
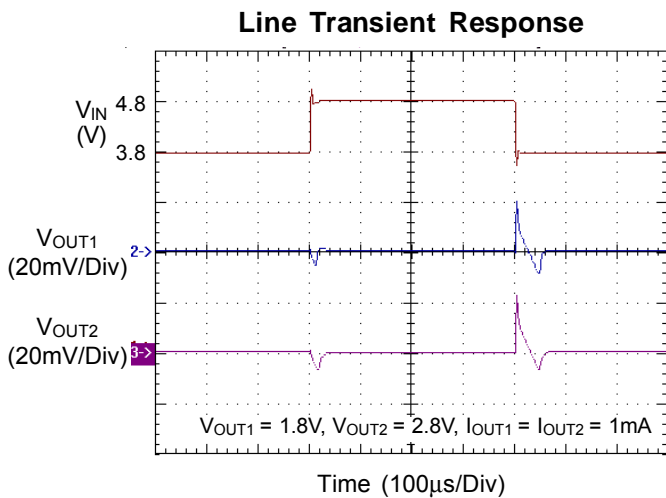
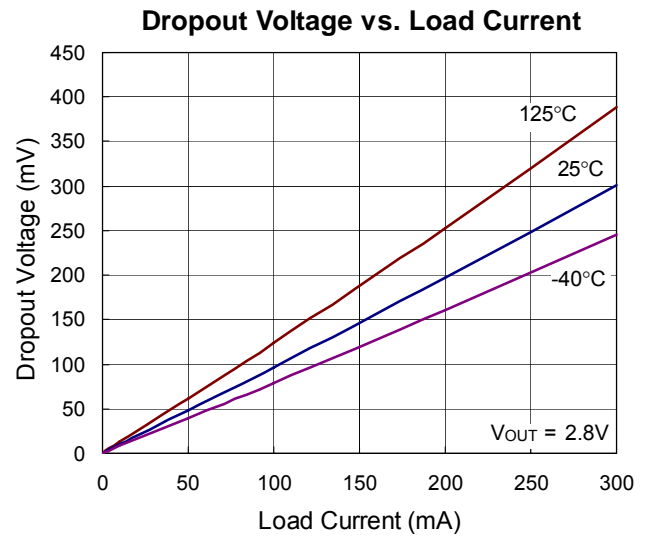
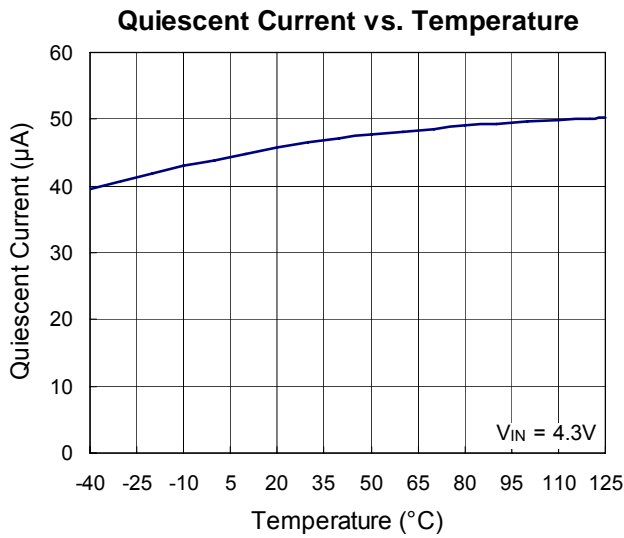
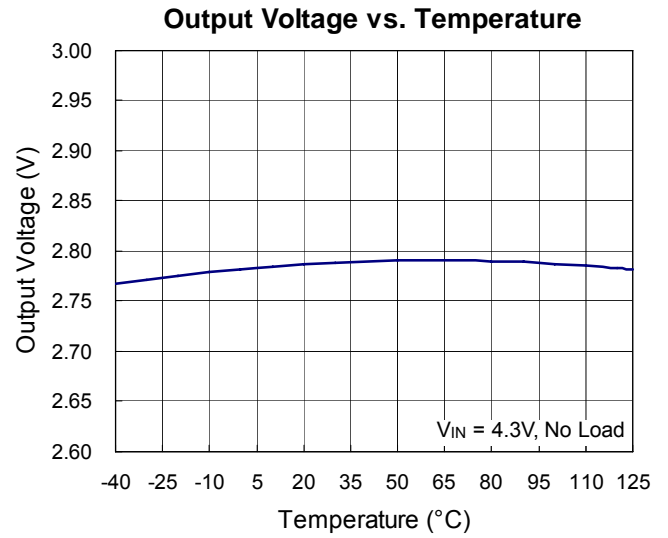
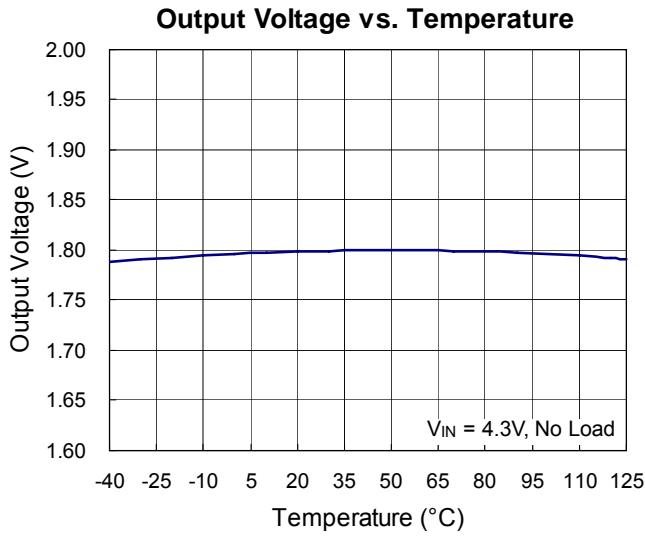
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition ($I_{OUT} = 0mA$). The total current drawn from the supply is the sum of the load current plus the ground pin current.

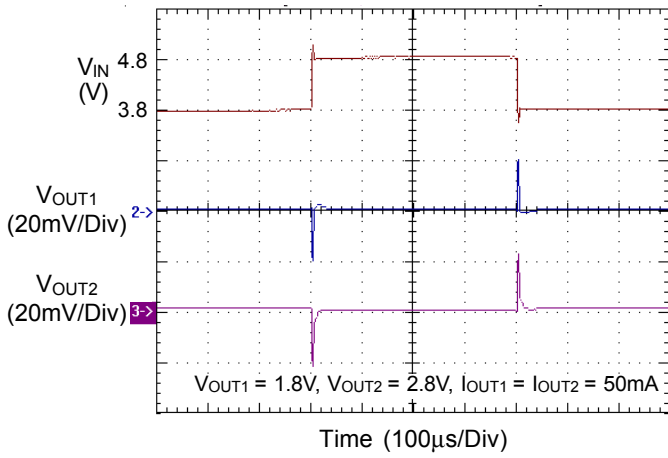
Note 6. The dropout voltage is defined as $V_{IN} - V_{OUT}$, which is measured when V_{OUT} is $V_{OUT(NORMAL)} - 100mV$.

Note 7. Output voltage V_{OUT1}/V_{OUT2} are configured by P1/P2 state when EN1 or EN2 go high. Subsequent changes to P1/P2 do not change V_{OUT1}/V_{OUT2} unless power on reset by V_{IN} or both of EN1 and EN2.

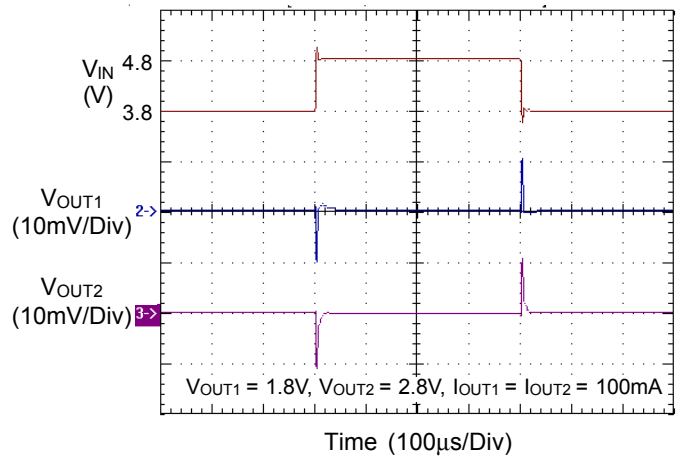
Typical Operating Characteristics



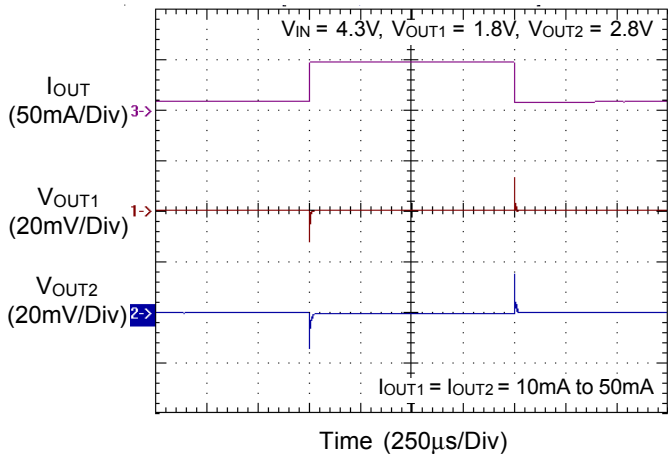
Line Transient Response



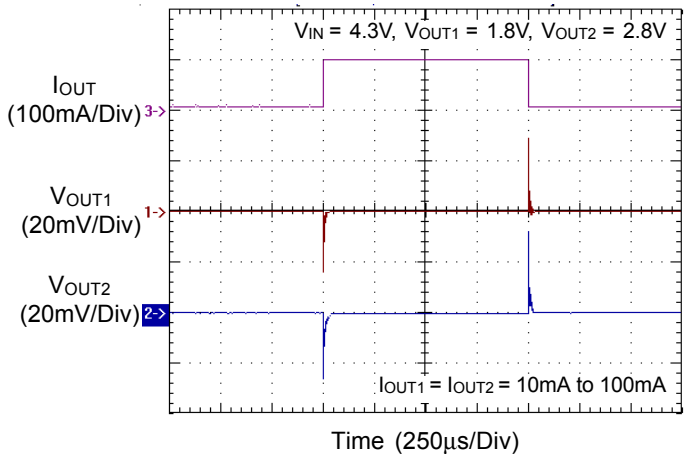
Line Transient Response



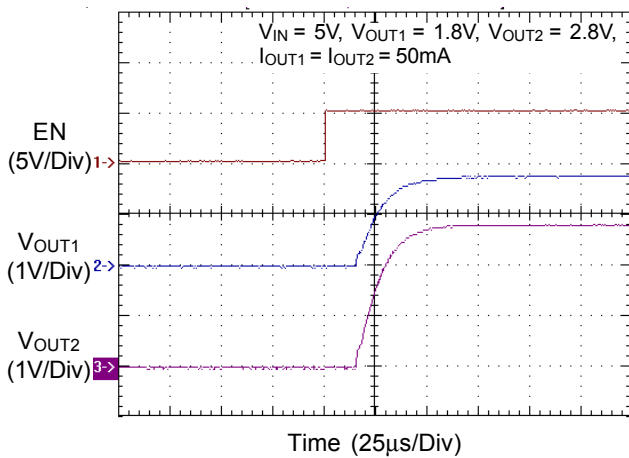
Load Transient Response



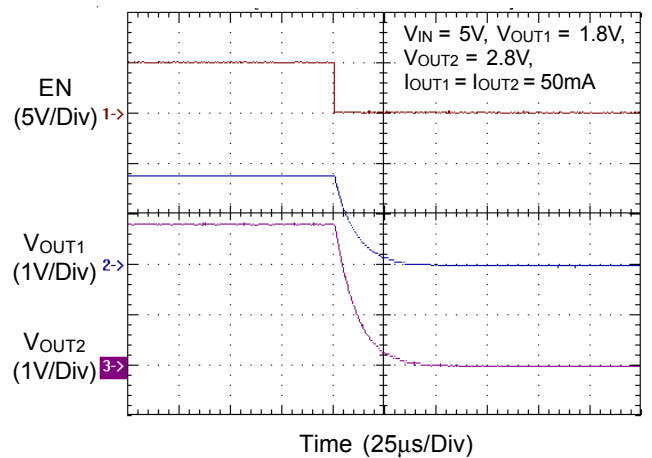
Load Transient Response



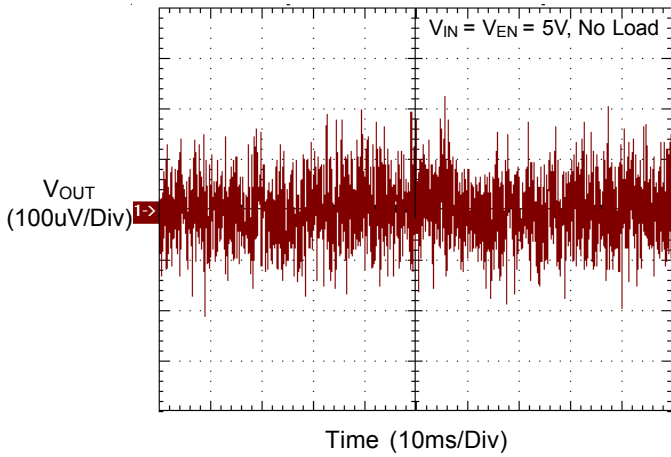
Power On from EN



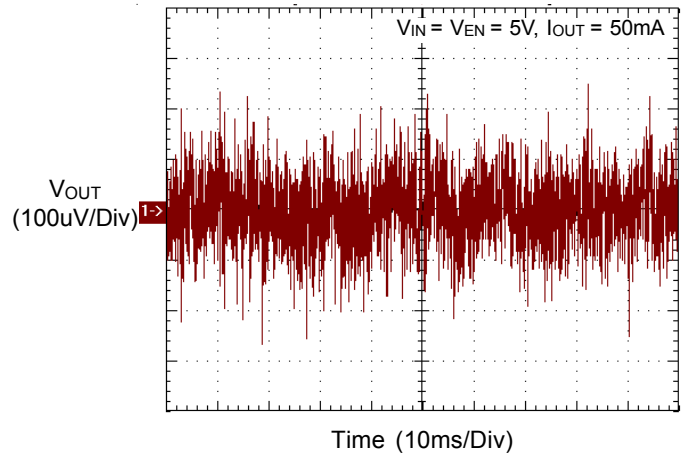
Power Off from EN



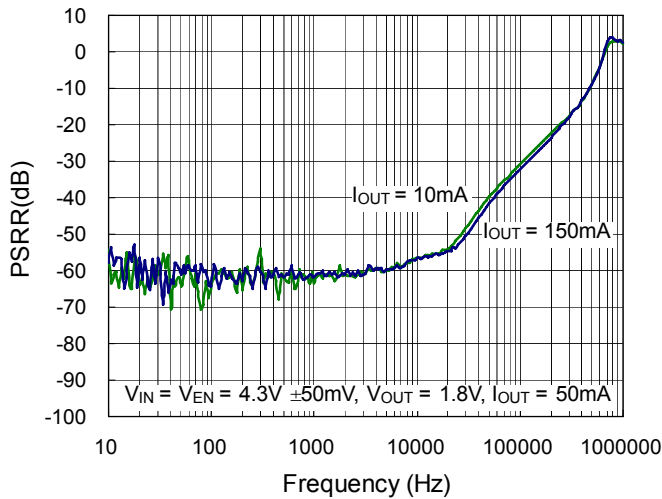
Noise



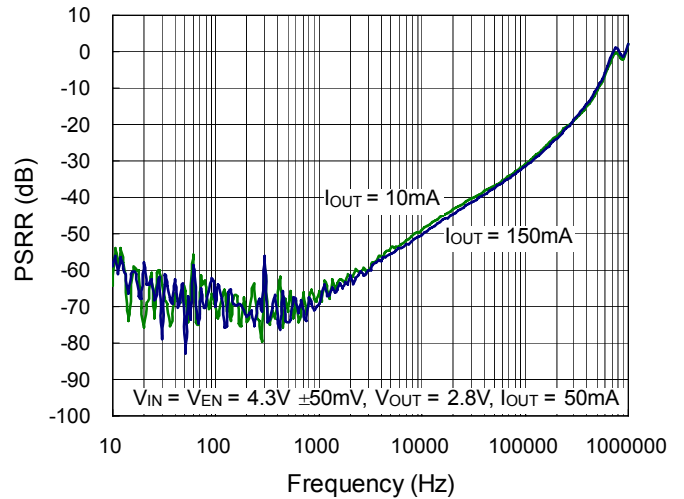
Noise



VOUT1 PSRR



VOUT2 PSRR



Application Information

Like any low-dropout regulator, the external capacitors used with the RT9032 must be carefully selected for regulator stability and performance. Using a capacitor whose value is $> 1\mu\text{F}$ on the RT9032 input and the amount of capacitance can be increased without limit. The input capacitor must be located at a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9032 is designed specifically to work with low ESR ceramic output capacitor for space-saving and performance consideration. Using a ceramic capacitor whose value is at least $1\mu\text{F}$ with ESR is $> 20\text{m}\Omega$ on the RT9032 output ensures stability. The RT9032 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1 shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located at not more than 0.5 inch from the output pin of the RT9032 and returned to a clean analog ground.

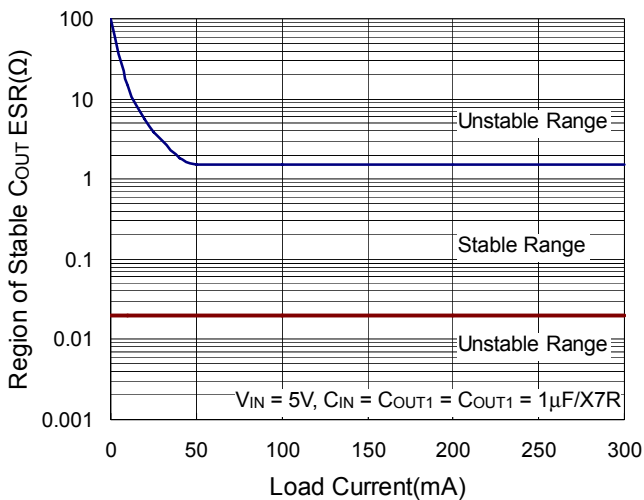


Figure 1

EN

The RT9032 goes into shutdown mode when the EN pin is in a logic low condition. During this condition, the pass transistor, error amplifier, and band gap are turned off, reducing the supply current to be lower than $1\mu\text{A}$. The EN pin can be directly tied to VIN to keep the part on.

Programmable Output Voltage Setting

There are nine sets of the VOUT1 and VOUT2 output voltages that can be achieved by setting three states (high/low/open) at the P1 and P2 pins.

The output voltage setting can be achieved by the preset of P1 and P2 states before VIN power on. However, if the P1 and P2 states are changed at the condition that only one of the EN pin is turned off-on, the VOUT1 and VOUT2 voltages will not be changed. The output voltage can be reset by turning off-on the input power (VIN) or both of EN pins (EN1 = EN2).

For the output voltage setting please refer to the "Table for Programmable Output Voltage Setting" in page 2.

Current Limit

The RT9032 contains an independent current limiter, which monitors and controls the pass transistor's gate voltage, limiting the output current to 430mA (typ.). The output can be shorted to ground indefinitely without damaging the part.

Thermal Shutdown Protection

As the die temperature is $>170^\circ\text{C}$, the chip will enter protection mode. The power MOSFET will be turned-off during the protection mode to prevent abnormal operation.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The power dissipation definition in device is :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification, the maximum junction temperature is 125°C. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for WDFN-8L 2x2 is 165°C/W and WQFN-8L 1.6x1.6 (COL) is 175°C/W on the standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (165^\circ\text{C/W}) = 0.606\text{W for WDFN-8L 2x2 packages}$$

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (175^\circ\text{C/W}) = 0.571\text{W for WQFN-8L 1.6x1.6 (COL) packages}$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA} . The Figure 2 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

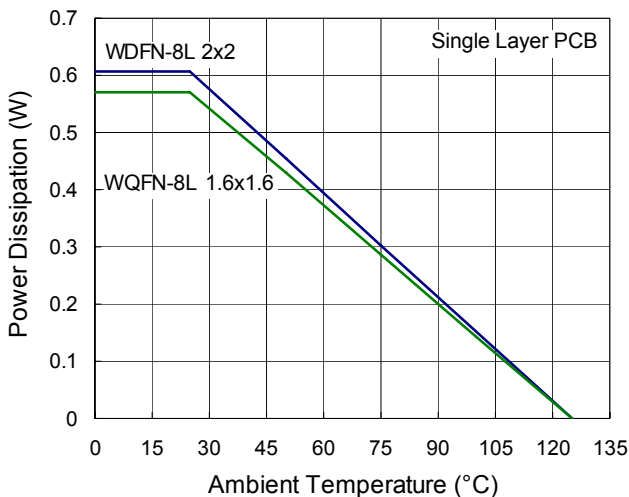


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Considerations

Careful PCB Layout is necessary for better performance. The following guidelines should be followed for good PCB layout.

- ▶ Place the input and output capacitors as close as possible to the IC.
- ▶ Keep VIN, VOUT1 and VOUT2 traces as possible as short and wide.
- ▶ Connect GND pin and Exposed Pad to a large PCB ground plane for maximum thermal dissipation.

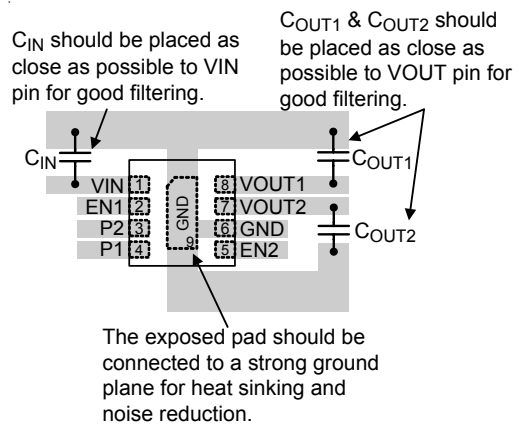


Figure 3. Layout Considerations for WDFN-8L 2x2 Packages

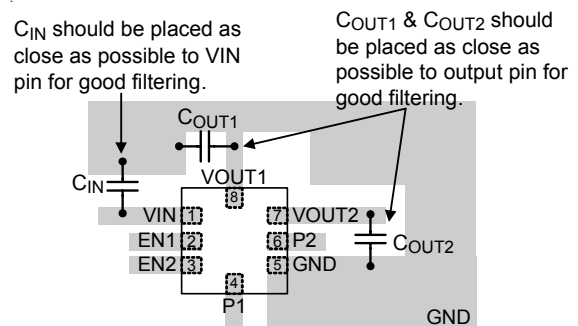
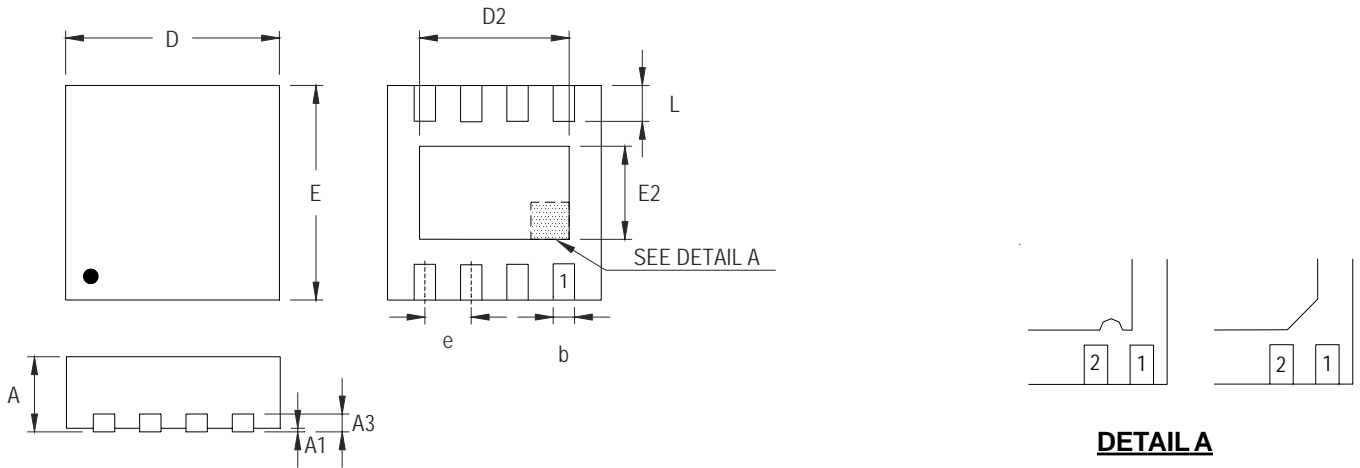


Figure 4. Layout Considerations for WQFN-8L 1.6x1.6 (COL) Packages

Outline Dimension

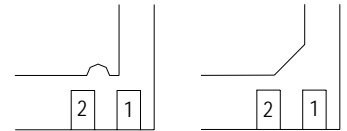
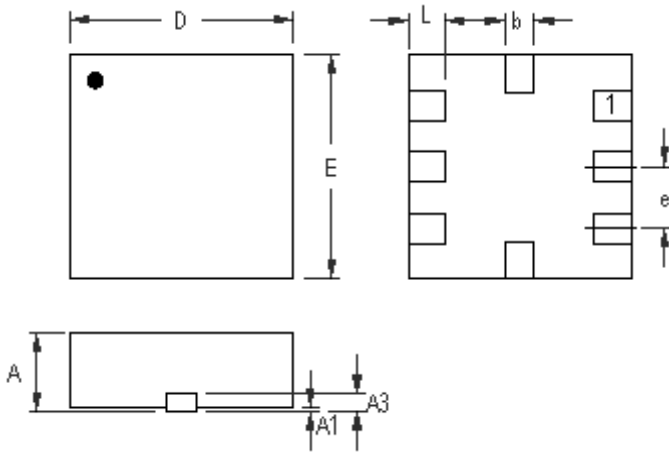


DETAILA
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| D | 1.950 | 2.050 | 0.077 | 0.081 |
| D2 | 1.000 | 1.250 | 0.039 | 0.049 |
| E | 1.950 | 2.050 | 0.077 | 0.081 |
| E2 | 0.400 | 0.650 | 0.016 | 0.026 |
| e | 0.500 | | 0.020 | |
| L | 0.300 | 0.400 | 0.012 | 0.016 |

W-Type 8L DFN 2x2 Package



DETAILA

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 1.550 | 1.650 | 0.061 | 0.065 |
| E | 1.550 | 1.650 | 0.061 | 0.065 |
| e | 0.400 | | 0.016 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

W-Type 8L QFN 1.6x1.6 (COL) Package

Richtek Technology Corporation

5F, No. 20, Taiyuen Street, Chupei City
 Hsinchu, Taiwan, R.O.C.
 Tel: (8863)5526789

Richtek products are sold by description only. Richtek reserves the right to change the circuitry and/or specifications without notice at any time. Customers should obtain the latest relevant information and data sheets before placing orders and should verify that such information is current and complete. Richtek cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Richtek product. Information furnished by Richtek is believed to be accurate and reliable. However, no responsibility is assumed by Richtek or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Richtek or its subsidiaries.