Obsolete Device

TC530/TC534

5V Precision Data Acquisition Subsystems

Features

- Precision (up to 17-Bits) A/D Converter
- 3-Wire Serial Port
- Flexible: User Can Trade Off Conversion Speed For Resolution
- Single Supply Operation
- -5V Output Pin
- 4 Input, Differential Analog MUX (TC530)
- Automatic Input Polarity and Overrange Detection
- Low Operating Current: 5mA Max
- Wide Analog Input Range: ±4.2V Max
- Cost Effective

Applications

- Precision Analog Signal Processor
- Precision Sensor Interface
- High Accuracy DC Measurements

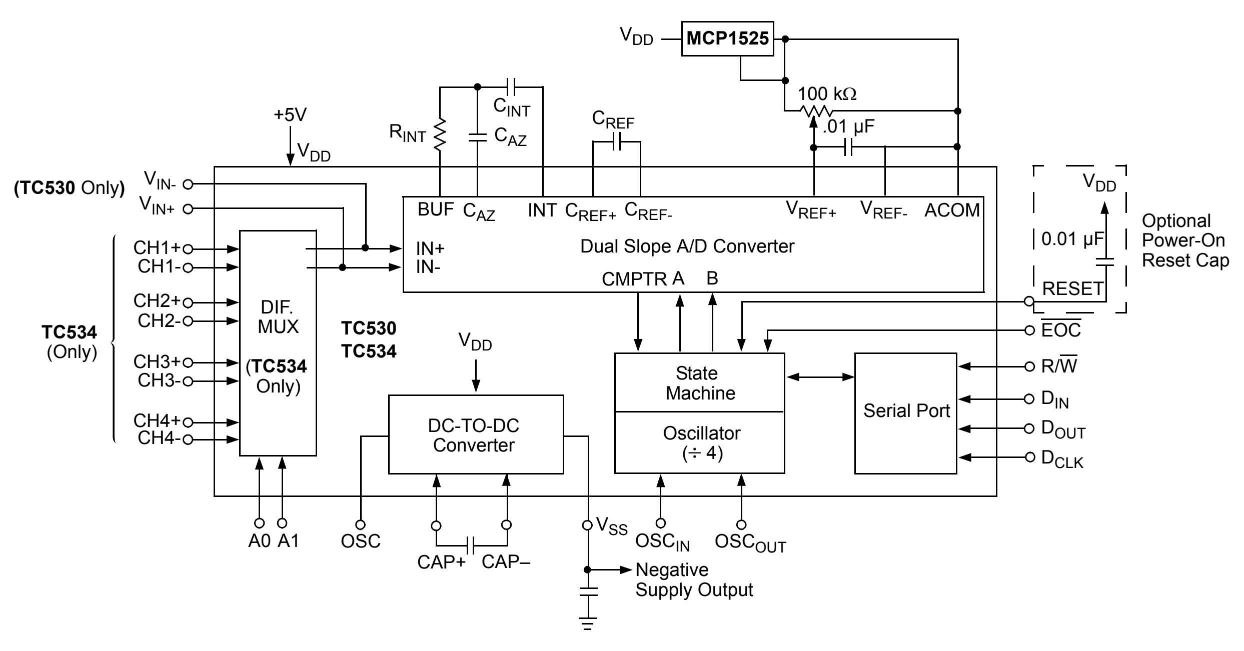
General Description

The TC530/TC534 are serial analog data acquisition subsystems ideal for high precision measurements (up to 17-bits plus sign). The TC534 consists of a dual slope integrating A/D converter, negative power supply generator and 3 wire serial interface port. The TC530 is identical to the TC534, but adds a four channel differential input multiplexer. Key A/D converter operating parameters (Auto Zero and Integration time) are programmable, allowing the user to trade conversion time for resolution.

Data conversion is initiated when the RESET input is brought low. After conversion, data is loaded into the output shift register and $\overline{\text{EOC}}$ is asserted, indicating new data is available. The converted data (plus Overrange and polarity bits) is held in the output shift register until read by the processor or until the next conversion is completed, allowing the user to access data at any time.

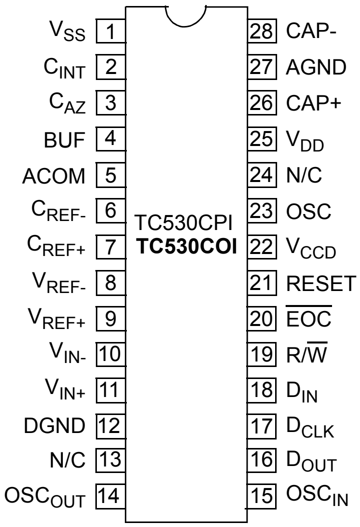
The TC530/TC534 timebase can be derived from an external crystal of 2MHz (max) or from an external frequency source. The TC530/TC534 requires a single 5V power supply and features a -5V, 10mA output which can be used to supply negative bias to other components in the system.

Typical Application

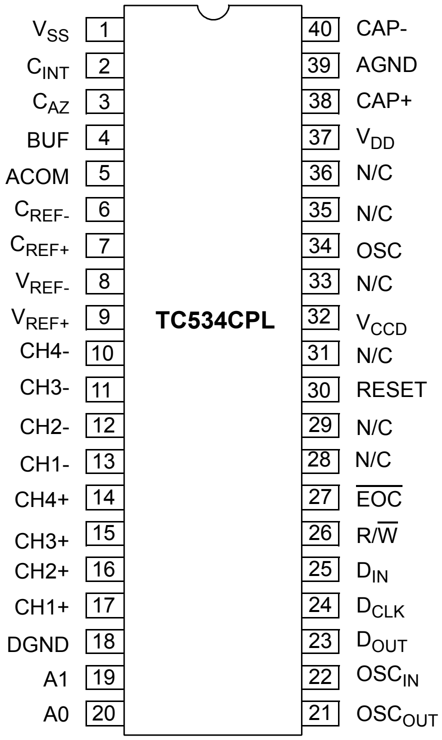


Package Types

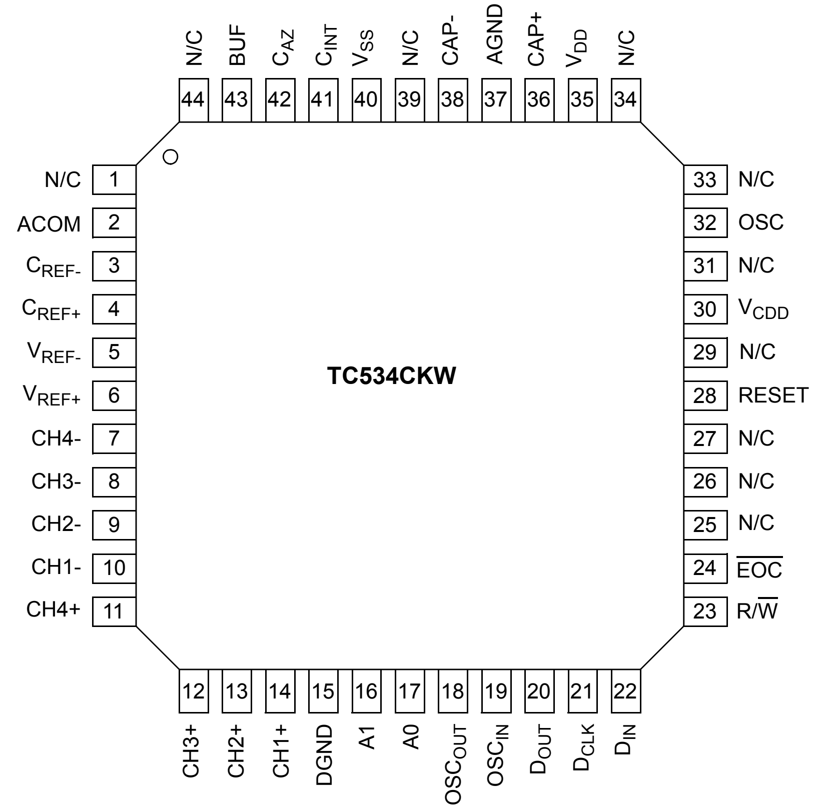
28-Pin SOIC
28-Pin PDIP



40-Pin PDIP



44-Pin MQFP



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage .... +6V

Analog Input Voltage (V_{IN}+ or V_{IN}-)............V_{DD} to V_{SS}

Logic Input Voltage......... (V_{DD} + 0.3V) to (GND - 0.3V)

Ambient Operating Temperature Range:

PDIP Package (C) .... 0°C to +70°C
SOIC Package (C)............................... 0°C to +70°C
MQFP Package (C) .... 0°C to +70°C

Storage Temperature Range.............. -65°C to +150°C

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise specifier, $V_{DD} = V_{CCD}$, $C_{AZ} = C_{REF}$ = 0.47 µF

Parameter	Symbol	T_A = +25°C			T_A = 0°C to +70°C			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max		
Analog Power Supply Voltage	V_{DD}	4.5	5.0	5.5	4.5	—	5.5	V	
Digital Power Supply Voltage	V_{CCD}	4.5	5.0	5.5	4.5	—	5.5	V	
Total Power Dissipation	P_D	—	—	25	—	—	—	mW	$V_{DD} = V_{CCD}$ = 5V
Supply Current ($V_S + P_{IN}$)	I_S	—	1.8	2.5	—	—	3.0	mA	
Supply Current (V_{CCD} P_{IN})	I_{CCD}	—	—	1.5	—	—	1.7	mA	F_{OSC} = 1 MHz
Analog									
Resolution	R	—	—	±17	—	—	±17	Bits	**Note 1**
Zero Scale Error with Auto Zero Phase	ZSE	—	—	0.5	—	0.005	0.012	% F.S.	
End Point Linearity	ENL	—	0.015	0.030	—	0.015	0.045	% F.S.	**Note 1** and **Note 2**
Max. Deviation from Best Straight Line Fit	NL	—	0.008	0.015	—	—	—	% F.S.	**Note 1** and **Note 2**
Zero Scale Temperature Coefficient	ZS_{TC}	—	—	—	—	1	2	µV/°C	
Rollover Error	SYE	—	.012	—	—	.03	—	% F.S.	**Note 3**
Full Scale Temperature Coefficient	FS_{TC}	—	—	—	—	10	—	ppm/°C	Ext. V_{REF} T.C. = 0 ppm/°C
Input Current	I_{IN}	—	6	—	—	—	—	pA	V_{IN} = 0V
Common-Mode Voltage Range	V_{CMR}	V_{SS} + 1.5	—	V_{DD} - 1.5	V_{SS} + 1.5	—	V_{DD} - 1.5	V	
Integrator Output Swing	V_{INT}	V_{SS} + 0.9	—	V_{DD} - 0.9	V_{SS} + 0.9	—	V_{DD} - 0.9	V	
Analog Input Signal Range	V_{IN}	V_{SS} + 1.5	—	V_{DD} -1.5	V_{SS} + 1.5	—	V_{DD} - 1.5	V	
Voltage Reference Range	V_{REF}	V_{SS} + 1	—	V_{DD} - 1	V_{DD} + 1	—	V_{DD} - 1	V	
Zero Crossing Comparator Delay	T_D	—	2.0	—	—	3.0	—	µs	

Note 1: Integrate time ≥ 66 ms. Auto Zero time ≥ 66 ms. V_{INT} (pk) = 4V.

2: End point linearity at ±1/4, ±1/2, and ±3/4. F.S. after full scale adjustment.

3: Rollover error is related to capacitor used for CINT. See Table 6-2, Recommended Capacitor for C_{INT}.

4: TC534 Only.

ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specifier, $V_{DD} = V_{CCD}$, $C_{AZ} = C_{REF} = 0.47\ \mu F$

Parameter	Symbol	T_A = +25°C			T_A = 0°C to +70°C			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max		
Serial Port Interface									
Input Logic HIGH Level	V_{IH}	2.5	—	—	2.5	—	—	V	
Input Logic LOW Level	V_{IL}	—	—	0.8	—	—	0.8	V	
Input Current (DI, DO, D_{CLK})	I_{IN}	—	—	10	—	—	—	µA	
Logic LOW Output Voltage ($\overline{\text{EOC}}$)	V_{OL}	—	0.2	0.3	—	—	0.35	V	I_{OUT} = 250 µA
Rise and Fall Times ($\overline{\text{EOC}}$, DI, DO)	T_R, T_F	—	—	250	—	250		ns	C_L = 10 pF
Crystal Frequency	F_{XTL}	—	—	2.0	—	—	2.0	MHz	
External Frequency on OSC_{IN}	F_{EXT}	—	—	4.0	—	—	4.0	MHz	
Read Setup Time	T_{RS}	1	—	—	—	1	—	µs	
Read Delay Time	T_{RD}	250	—	—	—	250		ns	
D_{CLK} to D_{OUT} Delay	T_{DRS}	450	—	—	—	450		ns	
D_{CLK} LOW Pulse Width	T_{PWL}	150	—	—	—	150		ns	
D_{CLK} HIGH Pulse Width	T_{PWH}	150	—	—	—	150		ns	
Data Ready Delay	T_{DR}	200	—	—	—	200		ns	
Output Resistance	R_{OUT}	—	65	85	—	—	100	Ω	I_{OUT} = 10 mA
Oscillator Frequency	F_{CLK}	—	100	—	—	—	—	kHz	C_{OSC} = 0
V_{SS} Output Current	I_{OUT}	—	—	10	—	—	10	mA	
Multiplexer									
Maximum Input Voltage	V_{IMMAX}	-2.5	—	2.5	-2.5	—	2.5	V	
Drain/Source ON Resistance	R_{DSON}	—	6	10	—	—	—	kΩ	

Note 1: Integrate time ≥ 66 ms. Auto Zero time ≥ 66 ms. V_{INT} (pk) = 4V.

2: End point linearity at ±1/4, ±1/2, and ±3/4. F.S. after full scale adjustment.

3: Rollover error is related to capacitor used for CINT. See Table 6-2, Recommended Capacitor for C_{INT}.

4: TC534 Only.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range), and therefore outside the warranted range.

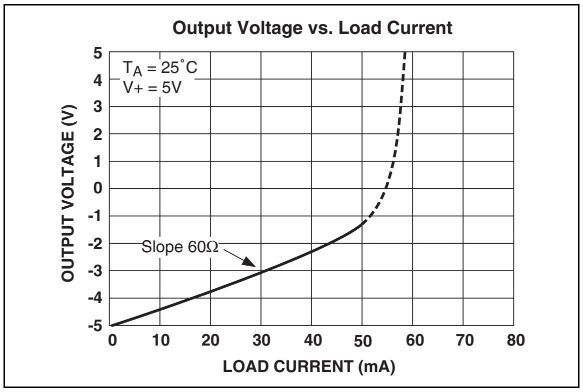


FIGURE 2-1: Output Voltage vs. Load Current.

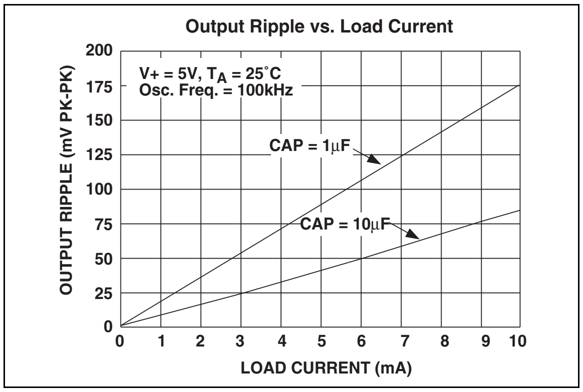


FIGURE 2-2: Output Ripple vs. Load Current.

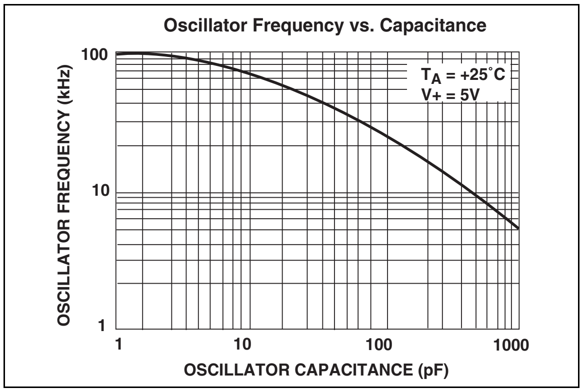


FIGURE 2-3: Oscillator Frequency vs. Capacitance.

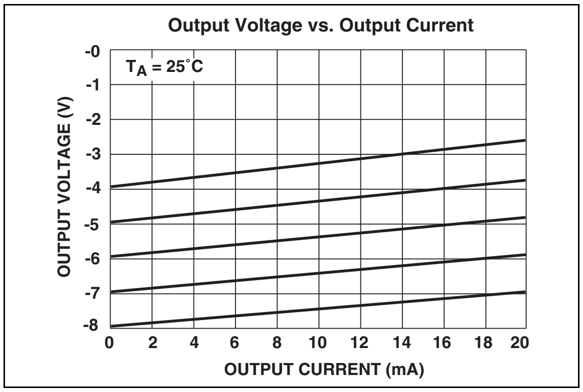


FIGURE 2-4: Output Voltage vs. Output Current.

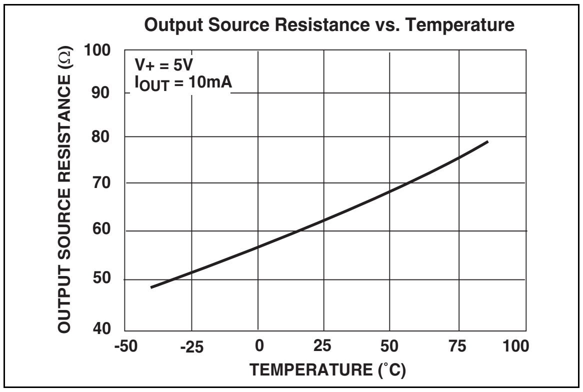


FIGURE 2-5: Output Source Resistance vs. Temperature.

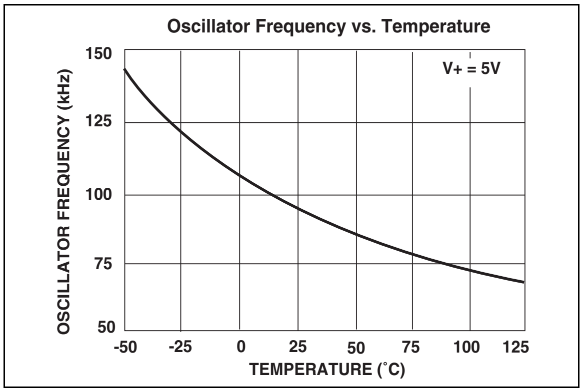


FIGURE 2-6: Oscillator Frequency vs. Temperature.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number (TC530) 28-Pin PDIP	Pin Number (TC530) 28-Pin SOIC	Pin Number (TC534) 40-Pin PDIP	Pin Number (TC534) 44-Pin MQFP	Sym	Description
1	1	1	40	V_{SS}	Analog output. Negative power supply converter output and reservoir capacitor connection. This output can be used to provide negative bias to other devices in the system.
2	2	2	41	C_{INT}	Analog output. Integrator capacitor connection and integrator output.
3	3	3	42	C_{AZ}	Analog input. Auto Zero capacitor connection.
4	4	4	43	BUF	Analog output. Integrator capacitor connection and voltage buffer output.
5	5	5	2	ACOM	Analog input. This pin is ground for all of the analog switches in the A/D converter. It is grounded for most applications. ACOM and the input common pin (V_{IN}- or CHX-) should be within the common mode range, CMR.
6	6	6	3	C_{REF}-	Analog Input. Reference cap negative connection.
7	7	7	4	C_{REF}+	Analog Input. Reference cap positive connection.
8	8	8	5	V_{REF}-	Analog Input. External voltage reference negative connection.
9	9	9	6	V_{REF}+	Analog Input. External voltage reference positive connection.
—	—	10	7	CH4-	Analog Input. Multiplexer channel 4 negative differential
—	—	11	8	CH3-	Analog Input. Multiplexer channel 3 negative differential
—	—	12	9	CH2-	Analog Input. Multiplexer channel 2 negative differential
—	—	13	10	CH1-	Analog Input. Multiplexer channel 1 negative differential
—	—	14	11	CH4+	Analog Input. Multiplexer channel 4 positive differential
—	—	15	12	CH3+	Analog Input. Multiplexer channel 3 positive differential
—	—	16	13	CH2+	Analog Input. Multiplexer channel 2 positive differential
—	—	17	14	CH1+	Analog Input. Multiplexer channel 1 positive differential
10	10	—	—	V_{N}-	Analog Input. Negative differential analog voltage input.
11	11	—	—	V_{IN}+	Analog Input. Positive differential analog voltage input.
12	12	18	15	DGND	Analog Input. Ground connection for serial port circuit.
—	—	19	16	A1	Logic Level Input. Multiplexer address MSB.
—	—	20	17	A0	Logic Level Input. Multiplexer address LSB.
14	14	21	18	OSC_{OUT}	Analog Input. Timebase for state machine. This pin connects to one side of an AT-cut crystal having an effective series resistance of 100Ω (typ) and a parallel capacitance of 20 pF. If an external frequency source is used to clock the TC530/TC534 this pin must be left floating.
15	15	22	19	OSC_{IN}	Analog Input. This pin connects to the other side of the crystal described in OSC_{OUT} above. The TC530/TC534 may also be clocked from an external frequency source connected to this pin. The external frequency source must be a pulse waveform with a minimum 30% duty cycle and rise and fall times 15nsec (Max). If an external frequency source is used, OSC_{OUT}) must be left floating. A maximum operating frequency of 2 MHz (crystal) or 4 MHz (external clock source) is permitted.

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number (TC530) 28-Pin PDIP	Pin Number (TC530) 28-Pin SOIC	Pin Number (TC534) 40-Pin PDIP	Pin Number (TC534) 44-Pin MQFP	Sym	Description
16	16	23	20	D_{OUT}	Logic Level Output. Serial port data output pin. This pin is enabled only when $R/\overline{W}$ is high.
17	17	24	21	D_{CLK}	Logic Input, Positive and Negative Edge Triggered. Serial port clock. When $R/\overline{W}$ is high, serial data is clocked out of the TC530/TC534A (on D_{OUT}) at each high-to-low transition of D_{CLK}. A/D initialization data (LOAD VALUE) is clocked into the TC530/TC534 (on D_{IN}) at each low-to-high transition of D_{CLK}. A maximum serial port D_{CLK} frequency of 3 MHz is permitted.
18	18	25	22	D_{IN}	Logic Level Input. Serial port input pin. The A/D converter integration time (T_{INT}) and Auto Zero time (T_{AZ}) values are determined by the LOAD VALUE byte clocked into this pin. This initialization must take place at power up, and can be rewritten (or modified and rewritten) at any time. The LOAD VALUE is clocked into D_{IN} MSB first.
19	19	26	23	$R/\overline{W}$	Logic Level Input. This pin must be brought low to perform a write to the serial port (e.g. initialize the A/D converter). The D_{OUT} pin of the serial port is enabled only when this pin is high.
20	20	27	24	$\overline{EOC}$	Open Drain Output. End-of-Conversion ($\overline{EOC}$) is asserted any time the TC530/TC534 is in the AZ phase of conversion. This occurs when either the TC530/TC534 initiates a normal AZ phase or when RESET is pulled high. $\overline{EOC}$ is returned high when the TC530/TC534 exits AZ. Since $\overline{EOC}$ is driven low immediately following completion of a conversion cycle, it can be used as a DATA READY processor interrupt.
21	21	30	28	RESET	Logic Level Input. It is necessary to force the TC530/TC534 into the Auto Zero phase when power is initially applied. This is accomplished by momentarily taking RESET high. Using an I/O port line from the microprocessor or by applying an external system reset signal or by connecting a 0.01 µF capacitor from the RESET input to V_{DD}. Conversions are performed continuously as long as RESET is low and conversion is halted when RESET is high. RESET may therefore be used in a complex system to momentarily suspend conversion (for example, while the address lines of an input multiplexer are changing state). In this case, RESET should be pulled high only when the $\overline{EOC}$ is LOW to avoid excessively long integrator discharge times which could result in erroneous conversion. (See *Applications* Section).
22	22	32	30	V_{CCD}	Analog Input. Power supply connection for digital logic and serial port. Proper power-up sequencing is critical, see the *Applications* section.
23	23	34	32	OSC	Input. The negative power supply converter normally runs at a frequency of 100 kHz. This frequency can be slowed down to reduce quiescent current by connecting an external capacitor between this pin and $V^+_{DD.}$ See **Section 2.0 “Typical Performance Curves”**, Typical Characteristics.
25	25	37	35	V_{DD}	Analog Input. Power supply connection for the A/D analog section and DC-DC converter. Proper power-up sequencing is critical, (See the *Applications* section).

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number (TC530) 28-Pin PDIP	Pin Number (TC530) 28-Pin SOIC	Pin Number (TC534) 40-Pin PDIP	Pin Number (TC534) 44-Pin MQFP	Sym	Description
26	26	38	36	CAP+	Analog Input. Storage capacitor positive connection for the DC/DC converter.
27	27	39	37	AGND	Analog Input. Ground connection for DC/DC converter.
28	28	40	38	CAP-	Analog Input. Storage capacitor negative connection for the DC/DC converter.
13, 24	13, 24	28, 29, 31, 33, 35, 36	1, 25, 26, 27, 29, 31, 33, 34, 39, 44	N/C	No connect. Do not connect any signal to these pins.

4.0 DETAILED DESCRIPTION

4.1 Dual Slope Integrating Converter

The TC530/TC534 dual slope converter operates by integrating the input signal for a fixed time period, then applying an opposite polarity reference voltage while timing the period (counting clocks pulses) for the integrator output to cross 0V (deintegrating). The resulting count is read as conversion data.

A simple mathematical expression that describes dual slope conversion is:

EQUATION 4-1:

Integrate Voltage = De-integrate Voltage

EQUATION 4-2:

$$\frac{1}{R_{INT}C_{INT}}\int_0^{T_{INT}} V_{IN}(T)dT = \frac{1}{R_{INT}C_{INT}}\int_0^{T_{DEINT}} V_{REF}$$

from which:

EQUATION 4-3:

$$(V_{IN})\left[\frac{(T_{INT})}{(R_{INT})(C_{INT})}\right] = (V_{REF})\left[\frac{(T_{DEINT})}{(R_{INT})(C_{INT})}\right]$$

And therefore:

EQUATION 4-4:

$$V_{IN} = V_{REF}\left[\frac{T_{DEINT}}{T_{INT}}\right]$$

Where:

V_{REF} = Reference Voltage
T_{INT} = Integrate Time
T_{DEINT} = Reference Voltage De-integrate Time

Inspection of Equation 4-4 shows dual slope converter accuracy is unrelated to integrating resistor and capacitor values, as long as they are stable throughout the measurement cycle. This measurement technique is inherently ratiometric (i.e., the ratio between the T_{INT} and T_{DEINT} times is equal to the ratio between V_{IN} and V_{REF}).

Another inherent benefit is noise immunity. Input noise spikes are integrated, or averaged to zero, during the integration period. The integrating converter has a noise immunity with an attenuation rate of at least -20 dB per decade. Interference signals with frequencies at integral multiples of the integration period are, for the most part, completely removed. For this reason, the integration period of the converter is often established to reject 50/60 Hz line noise. The ability to reject such noise is shown by the plot of Figure 4-1.

In addition to the two phases required for dual slope measurement (Integrate and De-integrate), the TC530/TC534 performs two additional adjustments to minimize measurement error due to system offset voltages. The resulting four internal operations (conversion phases) performed each measurement cycle are: Auto Zero (AZ), Integrator Output Zero (IZ), Input Integrate (INT) and Reference De-integrate (DINT). The AZ and IZ phases compensate for system offset errors and the INT and DINT phases perform the actual A/D conversion.

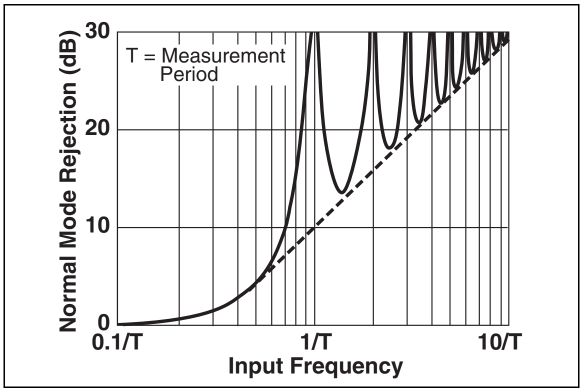
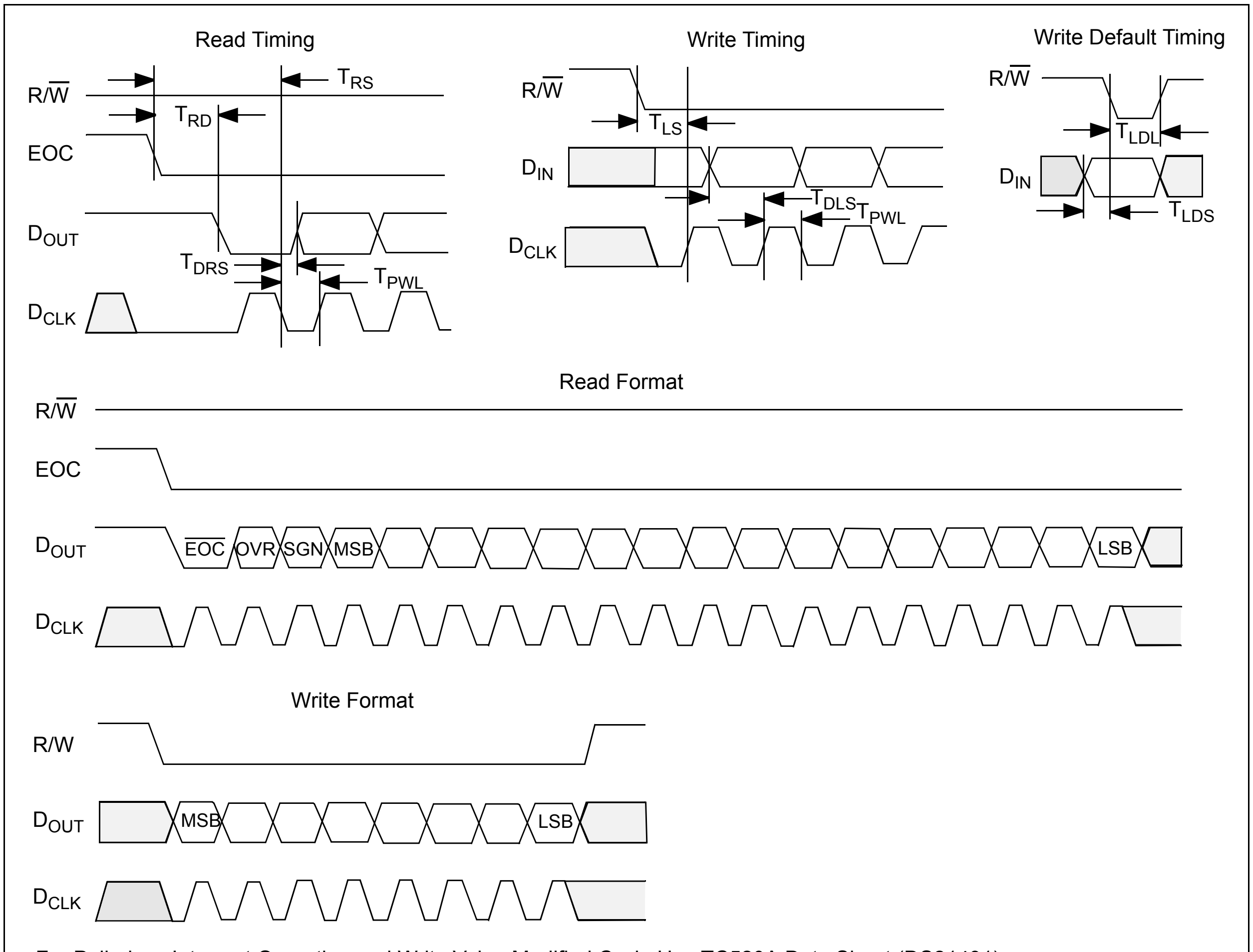


FIGURE 4-1: Integrating Converter Normal Mode Rejection.

4.2 Auto Zero Phase (AZ)

This phase compensates for errors due to buffer, integrator and comparator offset voltages. During this phase, an internal feedback loop forces a compensating error voltage on auto zero capacitor (C_{AZ}). The duration of the AZ phase is programmable via the serial port (see **Section 5.1.1 "AZ and INT Phase Duration"**, AZ and INT Phase Duration).



For Polled vs. Interrupt Operation and Write Value Modified Cycle Use TC520A Data Sheet (DS21431).

FIGURE 4-2: *Serial Port Timing.*

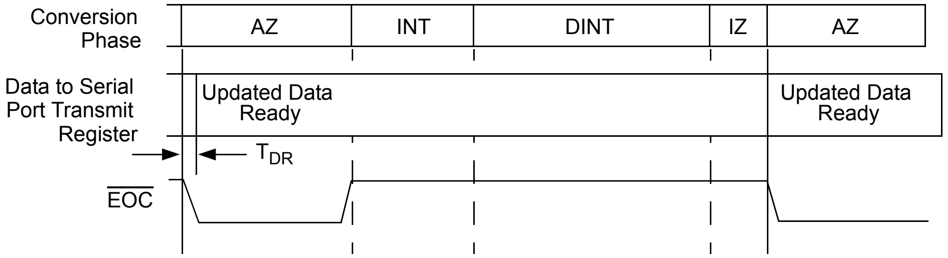


FIGURE 4-3: *A/D Converter Timing.*

4.3 Input Integrate Phase (INT)

In this phase, a current directly proportional to differential input voltage is sourced into integrating capacitor C_{INT}. The amount of voltage stored on C_{INT} at the end of the INT phase is directly proportional to the applied differential input voltage. Input signal polarity (sign bit) is determined at the end of this phase. Converter resolution and speed is a function of the duration of the INT phase, which is programmable by the user via the serial port (see **Section 5.1.1 "AZ and INT Phase Duration"**, AZ and INT Phase Duration). The shorter the integration time, the faster the speed of conversion (but the lower the resolution). Conversely, the longer the integration time, the greater the resolution (but at slower the speed of conversion).

4.4 Reference De-integrate Phase (DINT)

This phase consists of measuring the time for the integrator output to return (at a rate determined by the external reference voltage) from its initial voltage to 0V. The resulting timer data is stored in the output shift register as converted analog data.

4.5 Integrator Output Zero Phase (IZ)

This phase ensures the integrator output is at zero volts when the AZ phase is entered so that only true system offset voltages will be compensated for.

All internal converter timing is derived from the frequency source at OSC_{IN} and OSC_{OUT}. This frequency source must be either an externally provided clock signal or an external crystal. If an external clock is used, it must be connected to the OSC_{IN} pin and the OSC_{OUT} pin must remain floating. If a crystal is used, it must be connected between OSC_{IN} and OSC_{OUT} and be physically located as close to the OSC_{IN} and OSC_{OUT} pins as possible. In either case, the incoming clock frequency is divided by four, with the resulting clock serving as the internal TC530/TC534 timebase.

5.0 TYPICAL APPLICATIONS

5.1 Programming the TC530/TC534

5.1.1 AZ AND INT PHASE DURATION

These two phases have equal duration determined by the crystal (or external) frequency and the timer initialization byte (LOAD VALUE). Timing is selected as follows:

1. Select Integration Time

   Integration time must be picked as a multiple of the period of the line frequency. For example, T_{INT} times of 33 ms, 66 ms and 132 ms maximize 60 Hz line rejection.

2. Estimate Crystal Frequency

   Crystal frequencies as high as 2 MHz are allowed. Crystal frequency is estimated using:

EQUATION 5-1:

$$2(R_{ES})/T_{INT}$$

Where:

R_{ES} = Desired Converter Resolution (in counts)

F_{IN} = Input Frequency (in MHz)

INT = Integration Time (in seconds)

3. Calculate LOAD VALUE

EQUATION 5-2:

$$[LOAD\ VALUE]10 = 256 - \frac{(T_{INT})(F_{IN})}{1024}$$

F_{IN} can be adjusted to a standard value during this step. The resulting base, -10 LOAD VALUE, must be converted to a hexadecimal number and then loaded into the serial port prior to initiating A/D conversion.

5.2 D_{INT} and I_Z Phase Timing

The duration of the D_{INT} phase is a function of the amount of voltage stored on the integrator capacitor during INT and the value of V_{REF}. The D_{INT} phase is initiated immediately following INT and terminated when an integrator output zero crossing is detected. In general, the maximum number of counts chosen for D_{INT} is twice that of INT (with V_{REF} chosen at $V_{IN(MAX)}/2$).

5.3 System RESET

The TC530/TC534 must be forced into the AZ state when power is first applied. A .01 µF capacitor connected from RESET to V_{DD} (or external system reset logic signal) can be used to momentarily drive RESET high for a minimum of 100 ms.

5.4 Design Example

Figure 5-1 shows a typical TC530 interrupt-driven application. Timing and component values are calculated from equations and recommendations made in **Section 4.1 "Dual Slope Integrating Converter"** and **Section 5.1 "Programming the TC530/TC534"** of this document. The $\overline{\text{EOC}}$ connection to the processor INT input is for interrupt-driven applications only. (In polled systems, the $\overline{\text{EOC}}$ output is available on D_{OUT}).

Given:

Required Resolution (R_{ES}):	16-bits (65,536 counts.)
Maximum:	V_{IN} ±2V
Power Supply Voltage:	+5V
60Hz System	

1. Pick Integration time (T_{INT}): 66 ms.
2. Estimate crystal frequency.

EXAMPLE 5-1:

$$F_{IN} = \frac{2R_{ES}}{T_{INT}} = \frac{2 \bullet 65536}{66ms} \approx 2MHz$$

3. Calculate LOAD VALUE

EXAMPLE 5-2:

$$LOAD\ VALUE = 256 - \frac{(T_{INT})(F_{IN})}{1024} = [128]_{10}$$
$$[128]_{10} = 80\ hex$$

4. Calculate R_{INT}.

EXAMPLE 5-3:

$$R_{INT} = \frac{V_{INMAX}}{20} = \frac{2}{20} = 100k\Omega$$

5. Calculate C_{INT} for maximum (4V) integrator output swing:

EXAMPLE 5-4:

$$\begin{aligned} C_{INT} &= \frac{(T_{INT})(20 \times 10^{6})}{(V_s - 0.9)} \\ &= \frac{(.066)(20 \times 10^{-6})}{4.1} \\ &= .32\mu F (use\ closest\ value:\ 0.33\mu F) \end{aligned}$$

Note: Microchip recommended capacitor: Evox-Rifa p/n: SMR5 334K50J03L

6. Choose C_{REF} and C_{AZ} based on conversion rate:

EXAMPLE 5-5:

Conversions/sec $= 1/(T_{AZ} + T_{INT} + 2T_{INT} + 2ms)$

$= 1/(66ms + 66ms + 132ms + 2ms)$

= 3.7 conversions/sec

from which $C_{AZ} = C_{REF} = \underline{0.22\mu F}$ (*Table 6-1*)

Note: Microchip recommended capacitor: Evox-Rifa p/n: SMR5 224K50J02L4.

7. Calculate V_{REF}.

EXAMPLE 5-1:

$$\begin{aligned} V_{REF} &= \frac{(V_S - 0.9)(C_{INT})(R_{INT})}{2(T_{INT})} \\ &= \frac{(4.1)(0.33 \times 1^{-6})(10^{5})}{2(.\dddot{0}66)} \\ &= 1.025V \end{aligned}$$

5.5 Power Supply Sequencing

Improper sequencing of the power supply inputs (V_{DD} vs. V_{CCD}) can potentially cause an improper power-up sequence to occur. See **Section 5.6 "Circuit Design/Layout Considerations"**, Circuit Design/Layout Considerations. Failing to insure a proper power-up sequence can cause spurious operation.

5.6 Circuit Design/Layout Considerations

1. Separate ground return paths should be used for the analog and digital circuitry. Use of ground planes and trace fill on analog circuit sections is highly recommended EXCEPT for in and around the integrator section and C_{REF}, C_{AZ} (C_{INT}, C_{REF}, C_{AZ}, R_{INT}). Stray capacitance between these nodes and ground appears in parallel with the components themselves and can affect measurement accuracy.
2. Improper sequencing of the power supply inputs (V_{DD} vs. V_{CCD}) can potentially cause an improper power-up sequence to occur in the internal state machines. It is recommended that the digital supply, V_{CCD}, be powered up first. One method of insuring the correct power-up sequence is to delay the analog supply using a series resistor and a capacitor. See Figure 5-1, TC530/TC534 Typical Application.
3. Decoupling capacitors, preferably a higher value electrolytic or tantulum in parallel with a small ceramic or tantalum, should be used liberally. This includes bypassing the supply connections of all active components and the voltage reference.
4. Critical components should be chosen for stability and low noise. The use of a metal-film resistor for R_{INT} and Polypropylene or Polyphenelyne Sulfide (PPS) capacitors for C_{INT}, C_{AZ} and C_{REF} is highly recommended.
5. The inputs and integrator section are very high impedance nodes. Leakage to or from these critical nodes can contribute measurement error. A guard-ring should be used to protect the integrator section from stray leakage.
6. Circuit assemblies should be exceptionally clean to prevent the presence of contamination from assembly, handling or the cleaning itself. Minute conductive trace contaminates, easily ignored in most applications, can adversely affect the performance of high impedance circuits. The input and integrator sections should be made as compact and close to the TC53X as possible.
7. Digital and other dynamic signal conductors should be kept as far from the TC53X's analog section as possible. The microcontroller or other host logic should be kept quiet during a measurement cycle. Background activities such as keypad scanning, display refreshing and power switching can introduce noise.

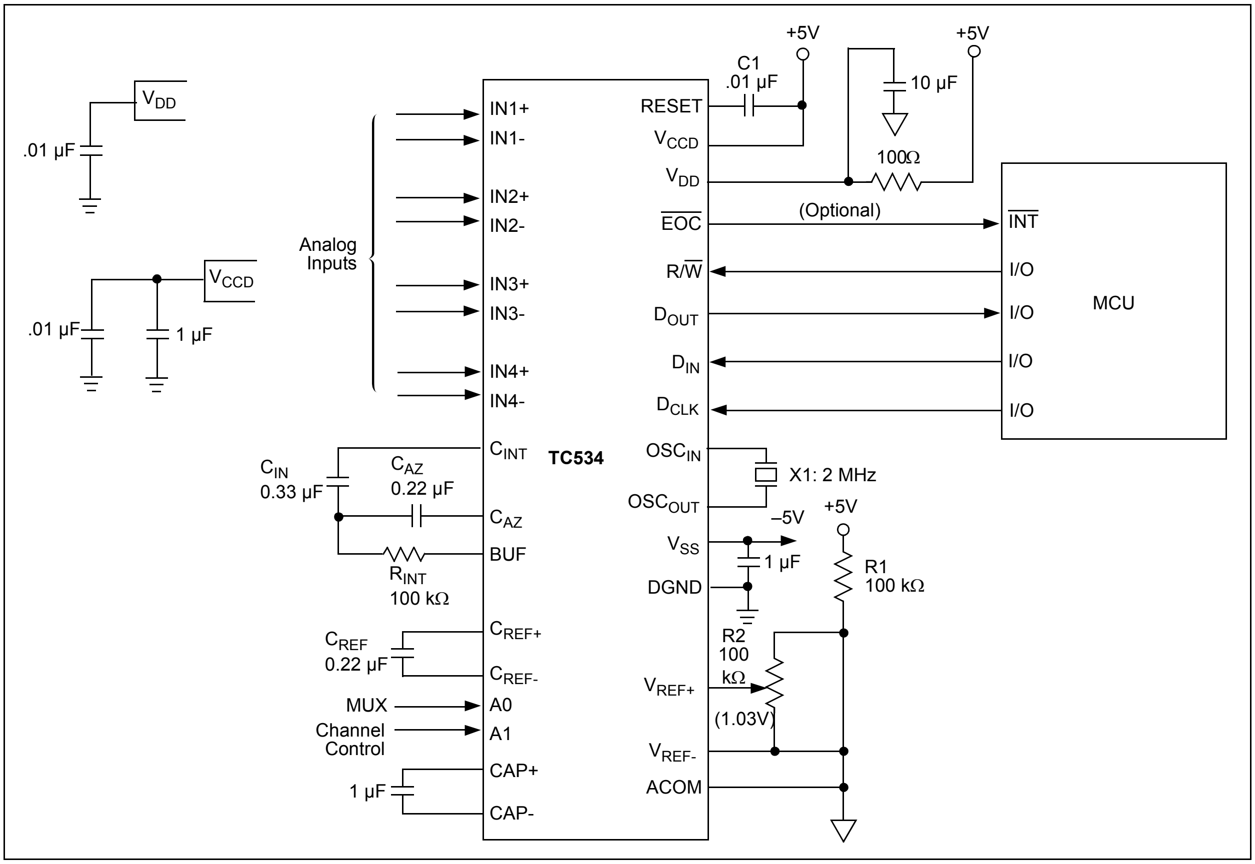


FIGURE 5-1: *Typical Application.*

6.0 SELECTING COMPONENT VALUES FOR THE TC530/TC534

1. Calculate Integrating Resistor (R_{INT})

   The desired full scale input voltage and amplifier output current capability determine the value of R_{INT}. The buffer and integrator amplifiers each have a full scale current of 20 µA. The value of R_{INT} is therefore directly calculated as follows:

EQUATION 6-1:

$$R_{INT}(M\Omega) = \frac{V_{INMAX}}{20}$$

Where:

$V_{IN(MAX)}$ = Maximum Input Voltage (full count voltage)

R_{INT} = Integrating Resistor (in MΩ)

For loop stability, R_{INT} should be ≥ 50 kΩ.

2. Select Reference (C_{REF}) and Auto Zero (C_{AZ}) Capacitors.

   C_{REF} and C_{AZ} must be low leakage capacitors (such as polypropylene). The slower the conversion rate, the larger the value C_{REF} must be. Recommended capacitors for C_{REF} and C_{AZ} are shown in Table 6-1. Larger values for C_{AZ} and C_{REF} may also be used to limit rollover errors.

TABLE 6-1: C_{REF} AND C_{AZ} SELECTION

Conversion Per Second	Typical Value of C_{REF}, C_{AZ} (µF)	Suggested [(1)] Part Number
>7	0.1	SMR5 104K50J0IL
2 to 7	0.22	SMR5 224K50J2L
2 or less	0.47	SMR5 474K50J04L

Note 1: Manufactured by Evox-Rifa, Inc.

6.1 Calculate Integrating Capacitor (C_{INT})

The integrating capacitor must be selected to maximize integrator output voltage swing. The integrator output voltage swing is defined as the absolute value of V_{DD} (or V_{SS}) less 0.9V (i.e.,$|V_{DD} - 0.9V|$ or $|V_{SS} + 0.9V|$). Using the 20 µA buffer maximum output current, the value of the integrating capacitor is calculated using Equation 6-2.

EQUATION 6-2:

$$C_{INT}(\mu F) = \frac{(T_{INT})(20 \times 10^{-6})}{(V_S - 0.9)}$$

Where:

T_{INT} = Integration Period

V_S = $|V_{DD}|$

C_{INT} = Integrated Capacitor Value (µF)

It is critical that the integrating capacitor have a very low dielectric absorption. PPS capacitors are an example of one such dielectric. Table 6-2 summarizes various capacitors suitable for C_{INT}.

TABLE 6-2: RECOMMENDED CAPACITOR FOR C_{INT}

Value (µF)	Suggested Part Number[(1)]
0.1	SMR5 104K50J0IL
0.22	SMR5 224K50J2L
0.33	SMR5 334K50J03L4
0.47	SMR5 474K50J04L

Note 1: Manufactured by Evox-Rifa, Inc.

6.2 Calculate V_{REF}

The reference de-integration voltage is calculated using the following equaton:

EQUATION 6-3:

$$V_{REF} = \frac{(V_S - 0.9)(C_{INT})(R_{INT})}{2(R_{INT})} V$$

6.3 Serial Port

Communication with the TC530/TC534 is accomplished over a 3-wire serial port. Data is clocked into D_{IN} on the rising edge of D_{CLK} and clocked out of D_{OUT} on the falling edge of D_{CLK}. $R/\overline{W}$ must be HIGH to read converted data from the serial port and LOW to write the LOAD VALUE to the TC530/TC534.

6.4 Data Read Cycle

Data is shifted out of the serial port in the following order: End of Conversion ($\overline{EOC}$), Overrange (OVR), Polarity (POL), conversion data (MSB first). When R/$\overline{W}$ is high, the state of the $\overline{EOC}$ bit can be polled by simply reading the state of D_{OUT}. This allows the processor to determine if new data is available without connecting an additional wire to the $\overline{EOC}$ output pin (this is especially useful in a polled environment). Refer to Figure 6-1.

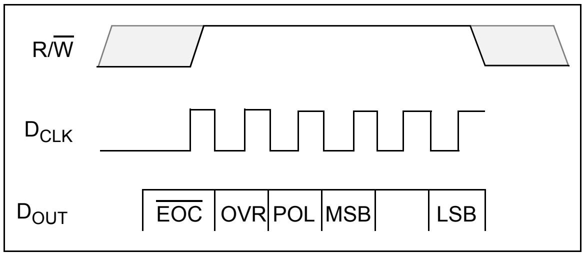


FIGURE 6-1: *Serial Port Data Read Cycle.*

6.5 Load Value Write Cycle

Following the power-up reset pulse, the LOAD VALUE (which sets the duration of AZ and INT) must next be transmitted to the serial port. To accomplish this, the processor monitors the state of EOC (which is available as a hardware output or at D_{OUT}). R/$\overline{W}$ is taken low to initiate the write cycle only when $\overline{EOC}$ is low (during the AZ phase). (Failure to observe $\overline{EOC}$ low may cause an offset voltage to be developed across C_{INT}, resulting in erroneous readings). The 8-bit LOAD VALUE data on D_{IN} is clocked in by D_{CLK}. The processor then terminates the write cycle by taking R/$\overline{W}$ high. (Data is transferred from the serial input shift register to the time base counter on the rising edge of R/$\overline{W}$ and data conversion is initiated). See Figure 6-2.

6.6 Input Multiplexer (TC534 Only)

A 4-input, differential multiplexer is included in the TC534. The states of channel address lines A0 and A1 determine which differential V_{IN} pair is routed to the converter input. A0 is the least significant address bit (i.e., channel 1 is selected when A0 = `0` and A1 = `0`). The multiplexer is designed to be operated in a differential mode. For single-ended inputs, the CHx- input for the channel under selection must be connected to the ground reference associated with the input signal.

6.7 DC/DC Converter

An on-board, TC7660H-type charge pump supplies negative bias to the converter circuitry, as well as to external devices. The charge pump develops a negative output voltage by moving charge from the power supply to the reservoir capacitor at V_{SS} by way of the commutating capacitor connected to the CAP+ and CAP- inputs.

The charge pump clock operates at a typical frequency of 100 kHz. If lower quiescent current is desired, the charge pump clock can be slowed by connecting an external capacitor from the OSC pin to V_{DD}. Reference typical characteristics curves.

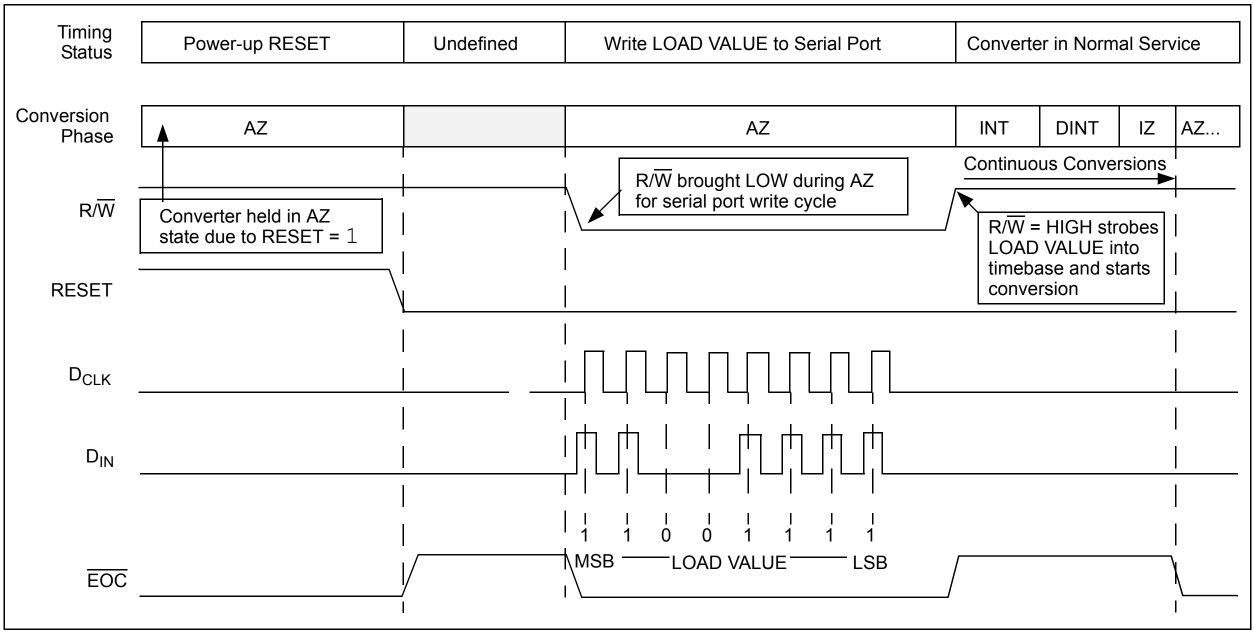
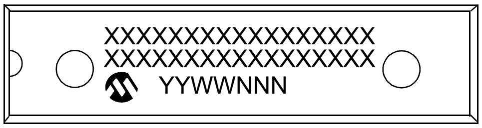


FIGURE 6-2: *TC530/TC534 Initialization and Load Value Write Cycle.*

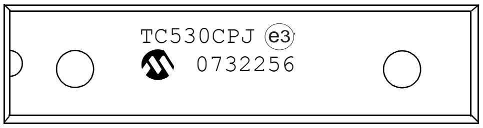
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

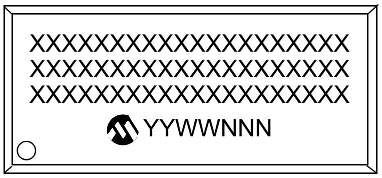
28-Lead SPDIP



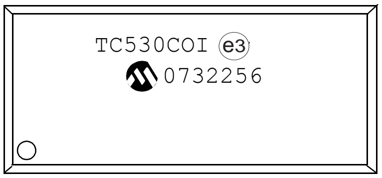
Example



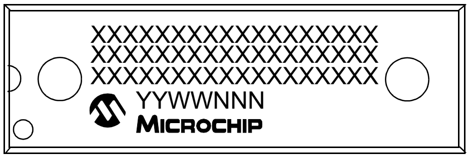
28-Lead SOIC (.300”)



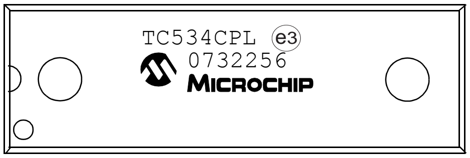
Example



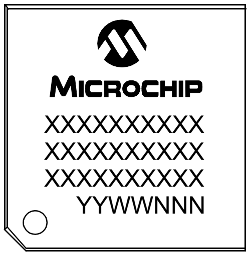
40-Lead PDIP



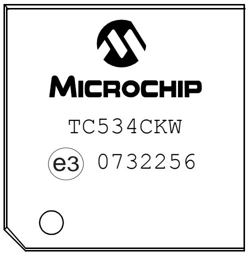
Example



44-Lead MQFP



Example

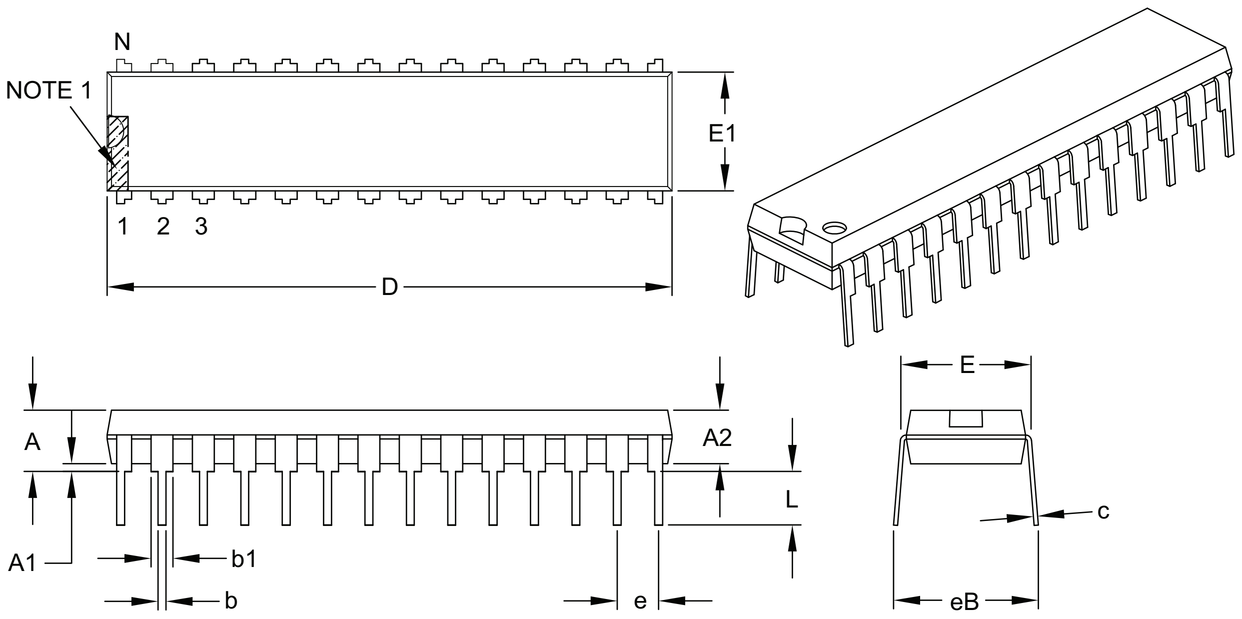


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

28-Lead Skinny Plastic Dual In-Line (PJ) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

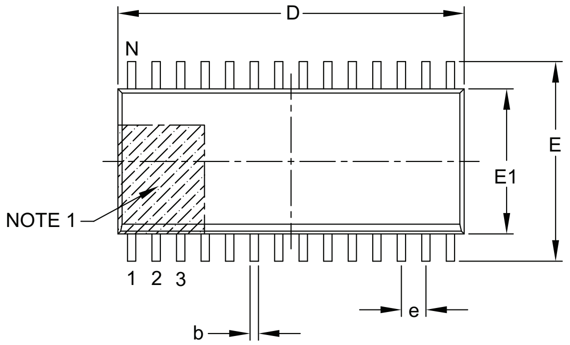
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

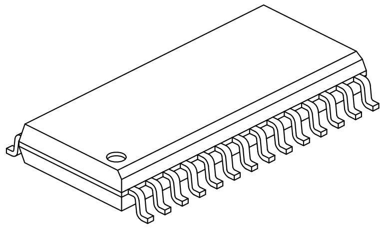
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

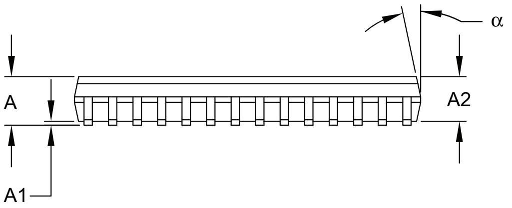
Microchip Technology Drawing C04-070B

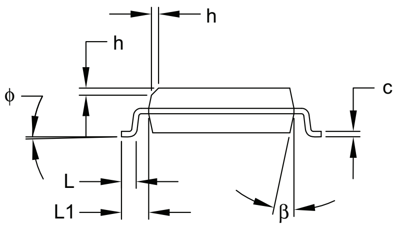
28-Lead Plastic Small Outline (OI) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1	1.40 REF		
Foot Angle Top	ϕ	0°	–	8°
Lead Thickness	c	0.18	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

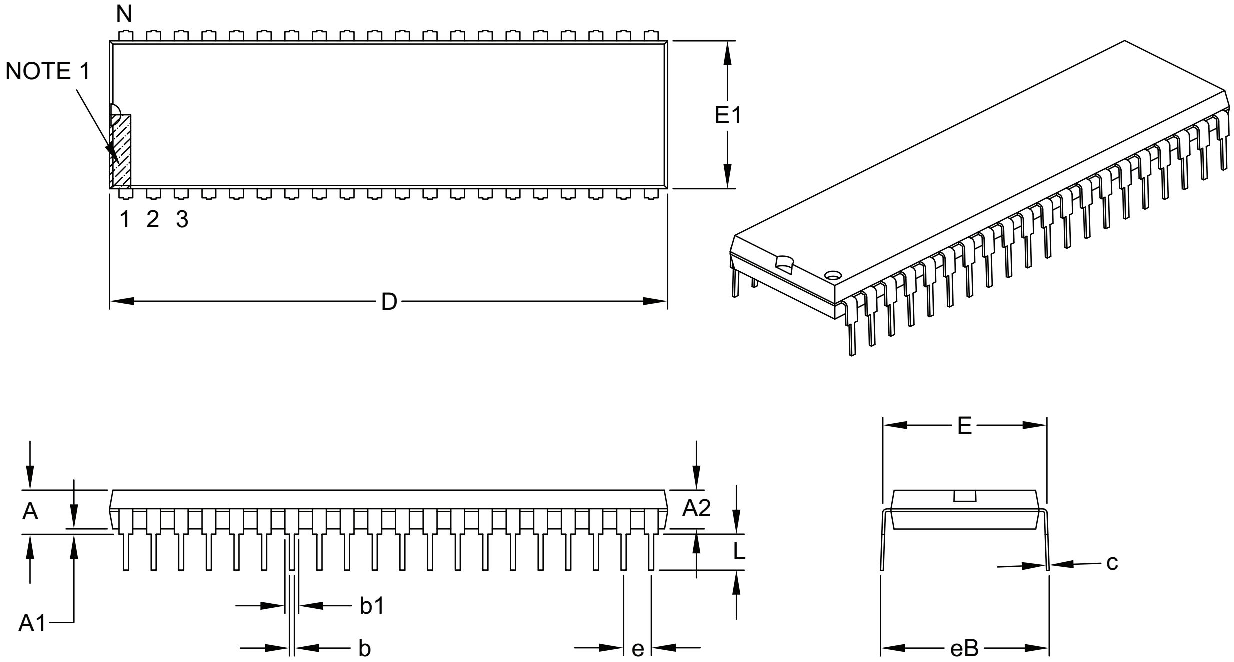
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B

40-Lead Plastic Dual In-Line (PL) – 600 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	40		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.250
Molded Package Thickness	A2	.125	–	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.590	–	.625
Molded Package Width	E1	.485	–	.580
Overall Length	D	1.980	–	2.095
Tip to Seating Plane	L	.115	–	.200
Lead Thickness	c	.008	–	.015
Upper Lead Width	b1	.030	–	.070
Lower Lead Width	b	.014	–	.023
Overall Row Spacing §	eB	–	–	.700

Notes:

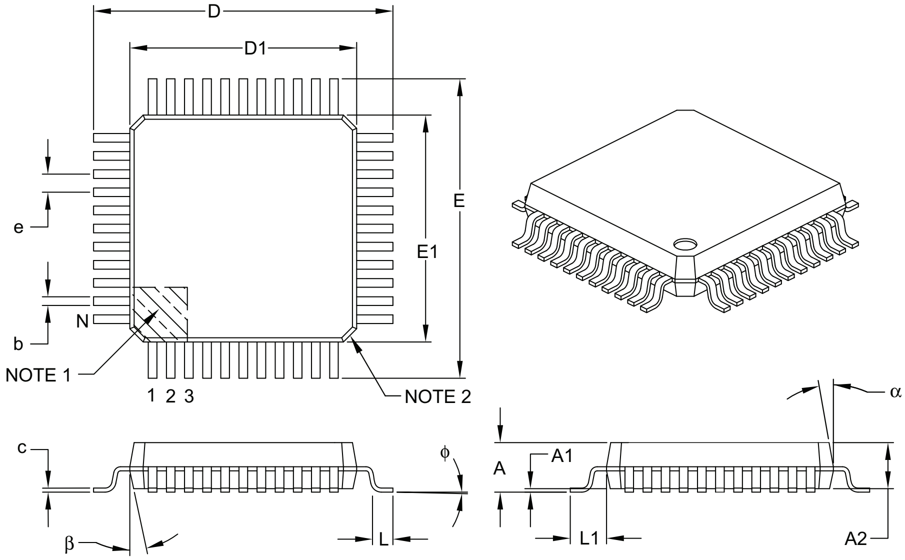
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-016B

44-Lead Plastic Metric Quad Flatpack (KW) – 10x10x2 mm Body, 3.20 mm Footprint [MQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	44		
Lead Pitch	e	0.80 BSC		
Overall Height	A	–	–	2.45
Molded Package Thickness	A2	1.80	2.00	2.20
Standoff §	A1	0.00	–	0.25
Foot Length	L	0.73	0.88	1.03
Footprint	L1	1.60 REF		
Foot Angle	φ	0°	–	7°
Overall Width	E	13.20 BSC		
Overall Length	D	13.20 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.11	–	0.23
Lead Width	b	0.29	–	0.45
Mold Draft Angle Top	α	5°	–	16°
Mold Draft Angle Bottom	β	5°	–	16°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. § Significant Characteristic.

Microchip Technology Drawing C04-071B

NOTES:

APPENDIX A: REVISION HISTORY

Revision C (September 2007)

- Change status from active to end-of-life (EOL).

Revision B (May 2002)

- Changes not documented.

Revision A (April 2002)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	**Temperature Range**	**Package**

Device	TC530:	Precision Data Acquisition Subsystem
	TC534:	Precision Data Acquisition Subsystem
Temperature Range	C =	0°C to +70°C (Commercial)
Package	KW =	Plastic Metric Quad Flatpack (10x10x2 mm), 44-lead
	PJ =	Skinny Plastic Dual In-Line (300 mil), 28-lead
	PL =	Plastic Dual In-Line (600 mil), 40-lead
	OI =	Plastic Small Outline (wide, 7.50 mm), 28-lead

Examples:

a)	TC530CPJ:	0°C to +70°C, 28LD SPDIP pkg
b)	TC530COI:	0°C to +70°C, 28LD SOIC pkg
a)	TC534CPL:	0°C to +70°C, 40LD PDIP pkg
b)	TC534CKW:	0°C to +70°C, 44LD MQFP pkg

NOTES:

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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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